Design Report for ECE 3020

Jack Adams

Abstract:

This project explores how inverter type, feedback, and reactive components influence amplifier behavior across DC, AC, and transient domains. Using LTspice simulations, I compared NMOS and BJT inverter circuits to see how their device physics impact switching behavior and frequency response. The results show that BJTs switch more sharply due to their exponential current behavior, while both devices respond almost identically when driven by large pulse inputs. I then introduced negative feedback and observed how it smooths transitions and improves stability, but at the cost of earlier gain roll-off. Adding an inductor in parallel with the load resistor created resonant behavior, where the sharpness of the resonance depended on the load resistance and inductance value. Finally, I simulated a MOS differential pair and analyzed its S-shaped transfer curve, highlighting the narrow transition region around 0V where small input changes cause large output shifts.

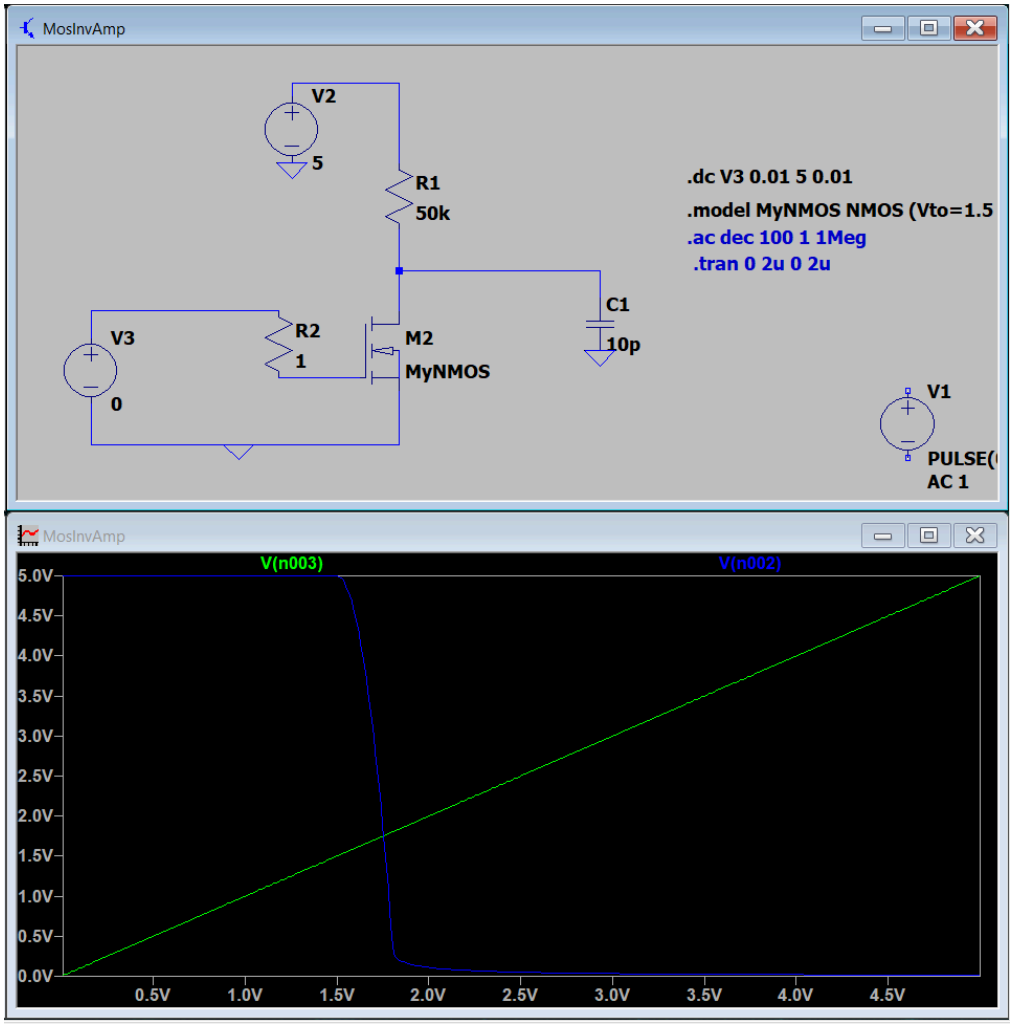
Introduction:

This study focuses on understanding how different inverting amplifier topologies behave across DC, AC, and transient domains. I specifically compared an NMOS inverter and a BJT inverter to see how their internal device physics influence switching behavior, gain response, and frequency limitations. In addition to comparing device types, I investigated how negative feedback alters circuit stability and response characteristics, and how adding reactive components such as inductors changes both frequency and time-domain behavior. The goal was not just to observe simulation results, but to understand why the circuit responds the way it does under different conditions. All analysis was performed using LTspice simulations along with hand calculations to verify key behaviors.

Results:

To begin the analysis, I built two common inverting amplifier circuits. Both circuits were configured the same, with the only difference being the active device: one used an NMOS transistor and the other used an NPN BJT.

The first comparison focused on how the DC sweep behavior changes when switching between these two inverter types.

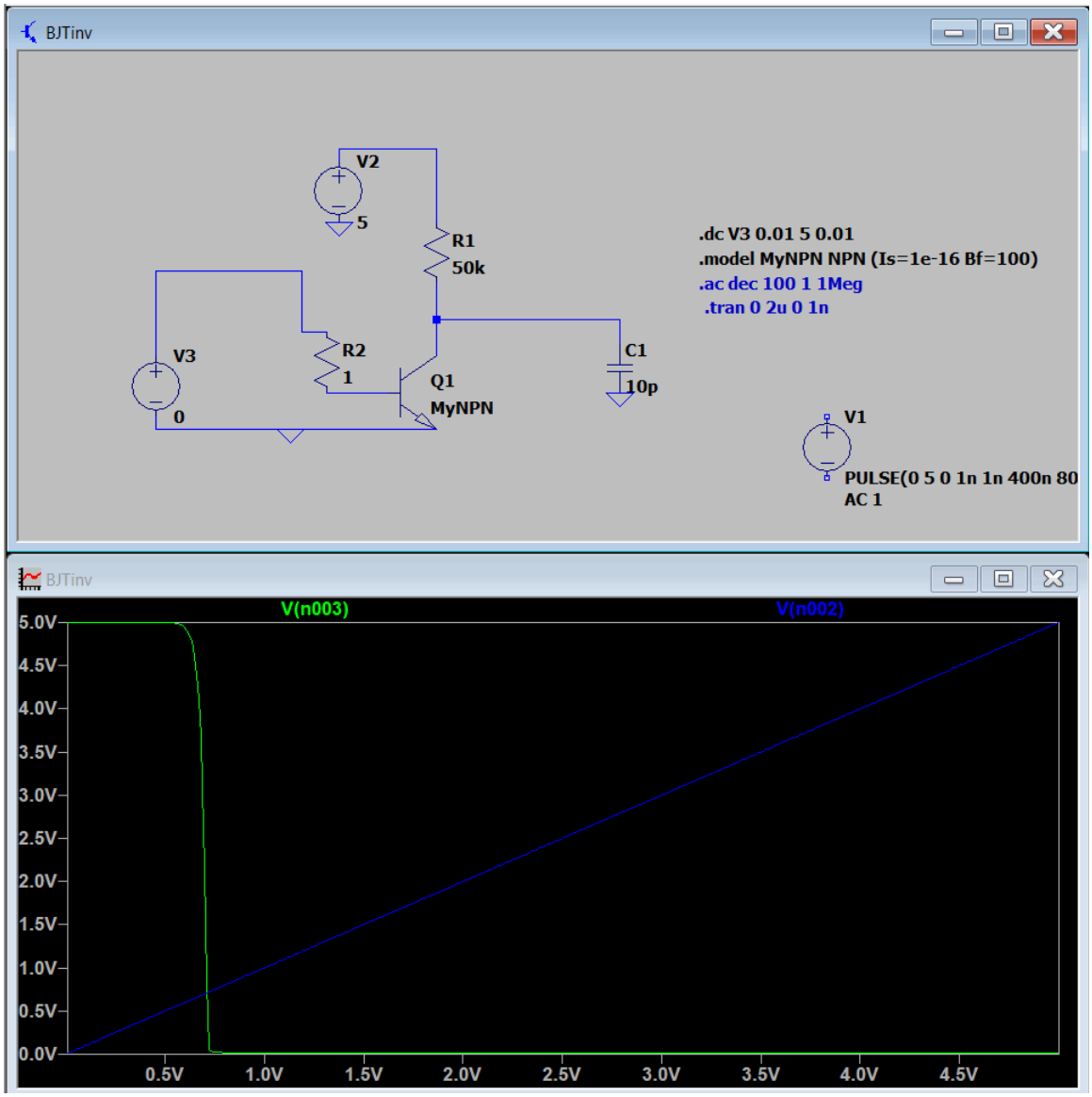


For the NMOS inverter, I performed a DC sweep from 0.01V to 5V in 0.01V increments to observe how the output responds as the input increases. The plot clearly shows the inverting behavior of the amplifier.

At low input voltages, the output remains high. This is because the NMOS transistor is off, so there is no conductive path to ground. The output node is therefore pulled up to 5V through the load resistor connected to VCC.

As the input voltage increases and approaches approximately 1.5V, the output begins to drop rapidly. This happens because the gate-to-source voltage exceeds the threshold voltage of the NMOS, allowing the transistor to turn on. Once the transistor conducts, it creates a path to ground and pulls the output node downward toward 0V. This behavior matches expectations, since the NMOS was modeled with a threshold voltage of 1.5V.

This sharp drop in output voltage marks the switching point of the inverter. With that established, I then compared this behavior to the DC sweep of the BJT inverter.



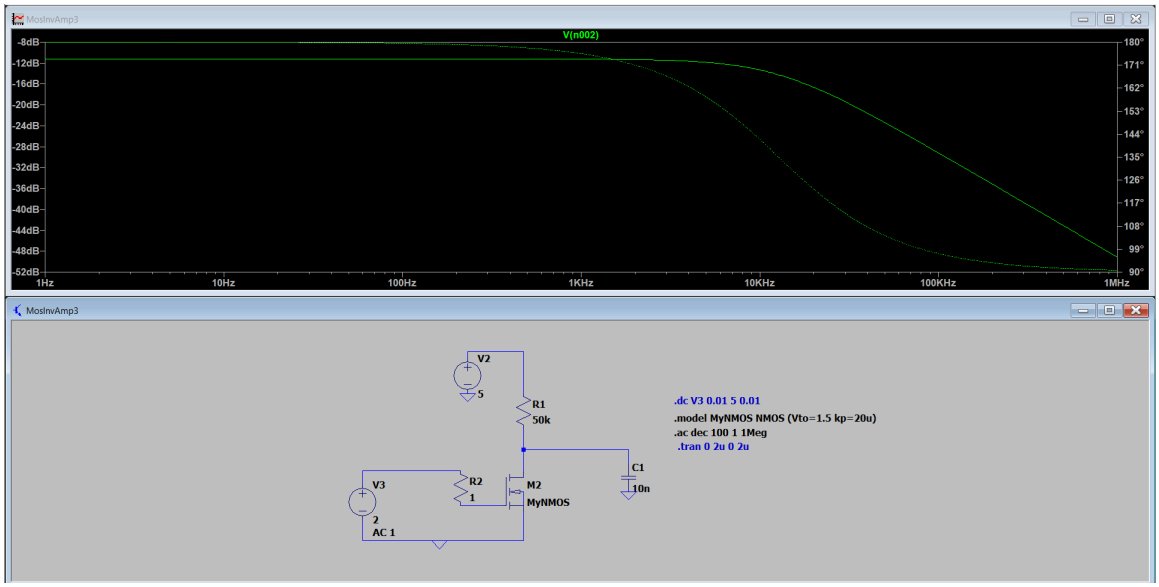
The BJT inverter shows similar overall behavior in the DC sweep. The output begins high and is pulled low once the transistor turns on, just like in the NMOS case. When the BJT is off, there is no path to ground and the output node is pulled up to 5V through the load resistor. Once the transistor conducts, it creates a path to ground and the output drops toward 0V.

The key difference is the switching point. The BJT begins turning on at approximately 0.7V instead of 1.5V. This is because the base-emitter junction is a PN junction, and it requires about 0.7V to become forward biased. Once this voltage is reached, collector current increases rapidly and the transistor enters conduction.

Another noticeable difference is the steepness of the transition. The BJT pull-down is sharper than the NMOS case. This comes directly from the device physics. In a BJT,

collector current increases exponentially with base-emitter voltage (Vbe), so small changes in input voltage produce large changes in collector current. In contrast, the drain current of a MOSFET increases approximately quadratically with gate-to-source voltage (Vgs). Because of this, the BJT transitions more abruptly, while the NMOS shows a slightly more gradual output fall.

The next analysis focused on the AC frequency response.



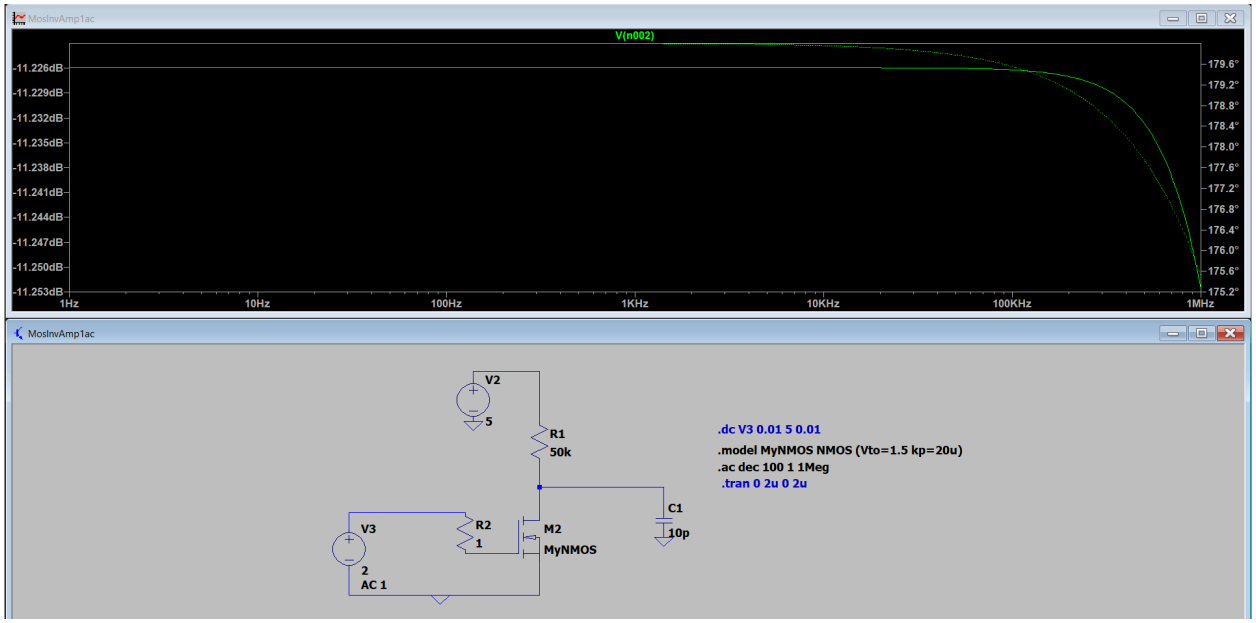
For the NMOS inverter, I ran an AC sweep from 1 Hz to 1 MHz. The plot shows both the gain in dB and the phase in degrees. I chose this range intentionally. Starting at 1 Hz allows the true low-frequency behavior of the amplifier to be observed, while extending to 1 MHz ensures that the high-frequency roll-off is clearly captured. From initial tests, I noticed that the amplifier begins losing gain around 10 kHz, so sweeping well beyond that point made the trend easier to see.

At low frequencies, the gain starts at approximately –12 dB, which corresponds to about 25% of the input amplitude. This slight attenuation is expected due to the small-signal limitations of the NMOS device. The finite transconductance (gm) of the MOSFET, along with the resistive divider formed by the drain load resistor and the transistor's output impedance, limits the achievable gain.

As the frequency increases beyond roughly 1 kHz, the gain begins to roll off. This drop is caused by capacitive loading effects at the output node. The capacitor plays a major role in shaping the high-frequency response. In fact, I initially made an error when setting up the simulation by using a 10 pF capacitor instead of 10 nF. With the smaller capacitance, the impedance $Zc=1/(2\pi fC)$ remained much higher across the frequency

range, so very little signal was shunted to ground. As a result, the gain roll-off was much less noticeable, even near 1 MHz.

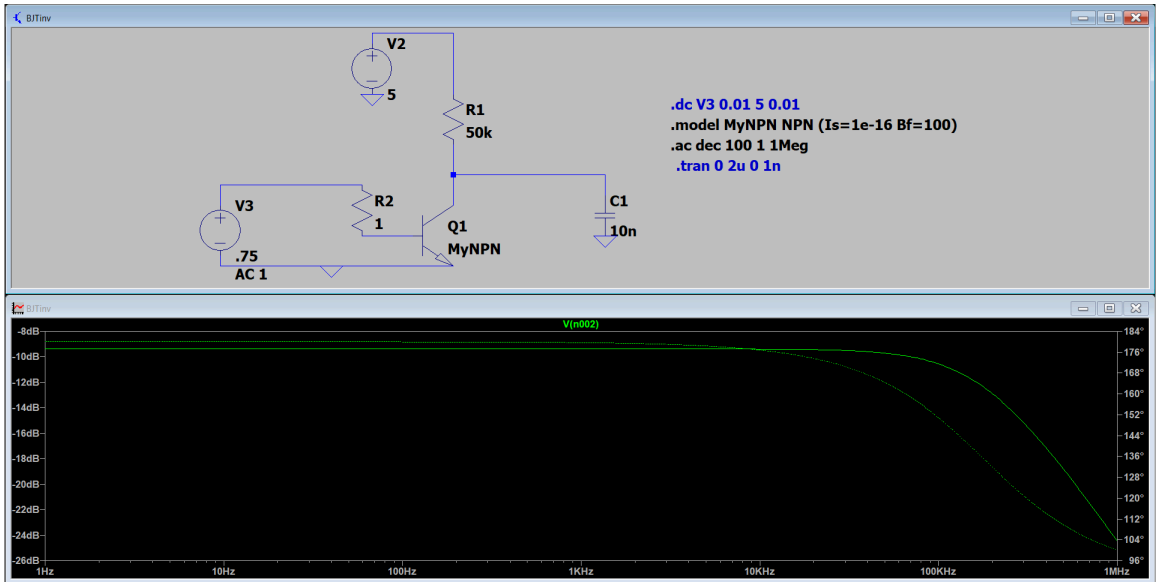
Correcting the capacitor value to 10 nF produced the expected high-frequency attenuation and clearly demonstrated how strongly reactive elements influence bandwidth.



With the smaller 10 pF capacitor, the magnitude change is much less noticeable. This makes sense because the impedance of a capacitor is given byZc=1/(2πfC)

Reducing the capacitance increases the impedance across the entire frequency range. As a result, much less signal is shunted to ground, and the amplifier maintains its gain even at higher frequencies. Even near 1 MHz, the attenuation is minimal compared to the 10 nF case.

With that behavior understood, I then compared the AC response of the NMOS inverter to the BJT inverter.



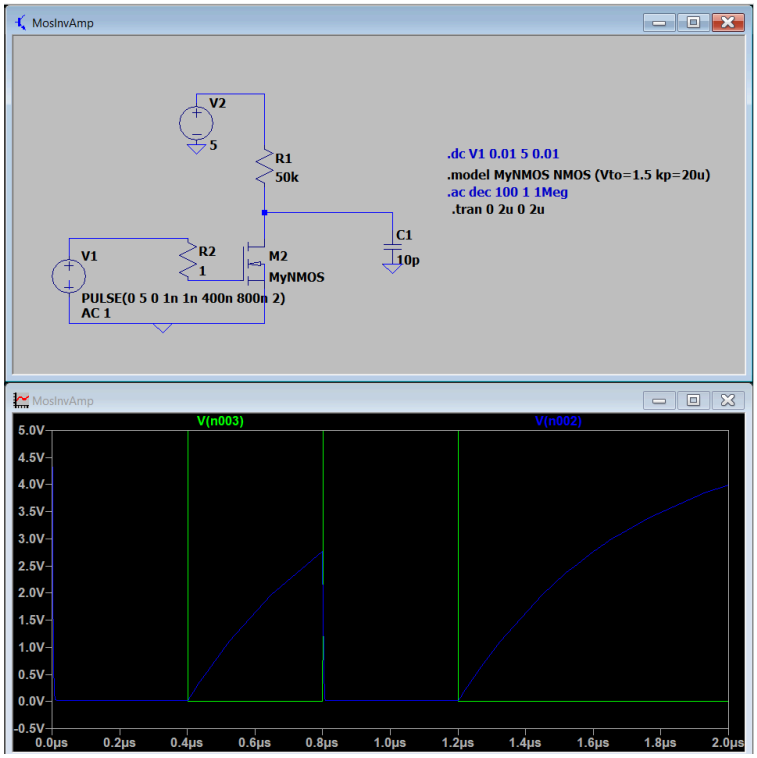
For the BJT inverter, both the magnitude and phase begin to roll off at a higher frequency compared to the NMOS inverter. This difference comes from the device characteristics of the BJT. BJTs generally have higher transconductance (gm), meaning they can drive current more effectively for a given input signal. In addition, the BJT has lower output impedance than the MOSFET. Because of this, the BJT amplifier is able to maintain its resistive behavior longer before capacitive effects begin to dominate.

The steeper falloff in the BJT response is also related to its higher gain and stronger ability to drive the load before the capacitor begins significantly affecting the output.

It is also important to note that for both inverters, the phase starts near 180 degrees at low frequencies. This is expected because both circuits operate as inverting amplifiers in this region. An ideal inverting amplifier produces an output that is 180 degrees out of phase with the input. For a sinusoidal input, this simply means the output is inverted, or shifted by half a period.

As the frequency increases, capacitive loading begins to dominate the response. The phase then shifts downward as the circuit transitions from primarily resistive behavior to increasingly reactive behavior. At sufficiently high frequencies, the capacitor begins to behave more like an integrator, which explains the continued phase shift.

With the AC behavior understood, I then moved on to analyzing the transient response of the inverter circuits.



For the transient simulation, I used a pulse input that swings from 0V to 5V with a 1 ns rise and fall time and a 400 ns pulse width.

When the input is at 0V, the NMOS transistor is off. With no conductive path to ground, the output node is pulled up to 5V through the pull-up resistor. When the input rises to 5V, the gate-to-source voltage exceeds the 1.5V threshold, turning the NMOS on. Once conducting, the transistor provides a path to ground and pulls the output rapidly toward 0V. The inverting behavior is clearly visible in the transient response.

One important observation is that the output rise is not instantaneous. Instead, the rising edge follows an exponential curve. This behavior is caused by the RC time constant formed by the pull-up resistor and the load capacitor. In this case:

$\tau = R1C1 = 50k\Omega \times 10pF = 500ns$

This time constant determines how quickly the output can charge toward 5V. The exponential rise matches the expected RC charging behavior.

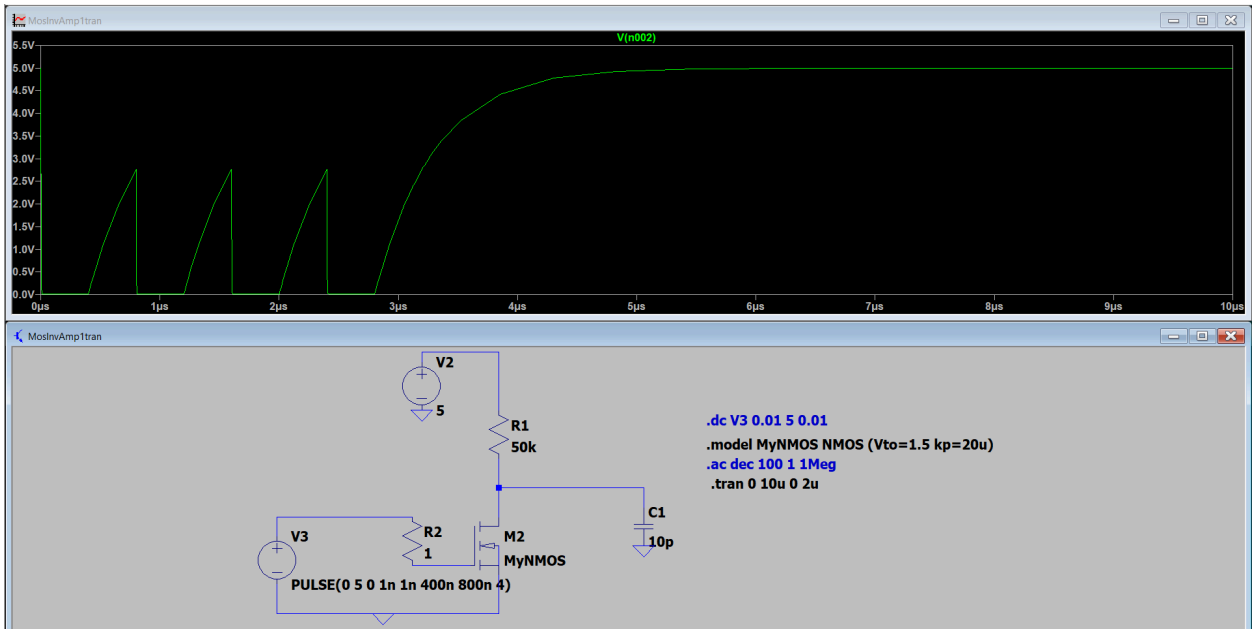
While setting up the simulation, I initially made an error by using a 10 nF capacitor instead of 10 pF. With 10 nF, the time constant becomes:

$\tau = 50k\Omega \times 10nF = 500\mu s$

which is 1000 times slower. At that value, the circuit responded far too slowly to the input pulse. Correcting the capacitor made the transient response behave as expected. This highlighted how strongly the RC time constant controls switching speed in time-domain behavior.

Another important observation is that the falling edge appears almost instantaneous. This is because when the NMOS turns on, it connects the output node to ground through a very small drain-to-source resistance RDS(on). Since this resistance is much smaller than the pull-up resistor, the output discharges much faster than it charges.

At first glance, it also appears that the output rises higher after the second pulse compared to the first. To verify whether this was actually happening or just a limited-time-window effect, I extended the simulation time to observe multiple switching cycles.



With the extended simulation window, it becomes clear that the output does not continue increasing with each pulse. Instead, after each switching cycle, the output rises to approximately the same peak value. In this case, there are four pulses, and we see three identical peaks followed by one longer rise at the end.

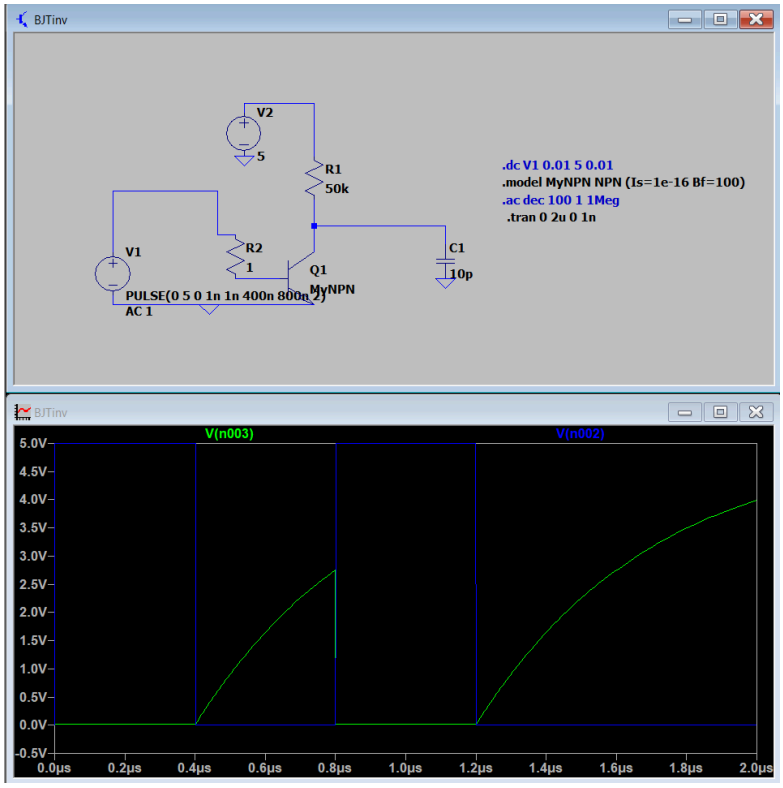
This behavior can be understood by looking at the RC charging process. After each falling edge, the output begins charging from 0V through the pull-up resistor R1. Since the pulse width and period are the same for each cycle, and the RC time constant remains constant, the output is allowed to charge for the same amount of time during each cycle before being pulled back down. Because of this, each rising segment follows the same exponential curve for the same duration, resulting in identical peak values.

This matches the expected RC charging equation:

$V(t)=Vf(1-e^{(-t/\tau)})$

where Vf is the final voltage (5V), τ is the time constant (500 ns), and t is the time allowed for charging. As long as t is limited by the pulse period, the peak voltage will remain the same for each cycle. On the final pulse, however, the input remains low afterward, allowing more time for charging. As a result, the output continues rising toward 5V and eventually settles there.

With the NMOS transient behavior understood, I then compared it to the BJT inverter.



The transient response of the BJT inverter looks almost identical to that of the NMOS inverter, even though their DC and AC responses showed noticeable differences. At first this might seem surprising, but it becomes clear when considering what the transient simulation is actually testing.

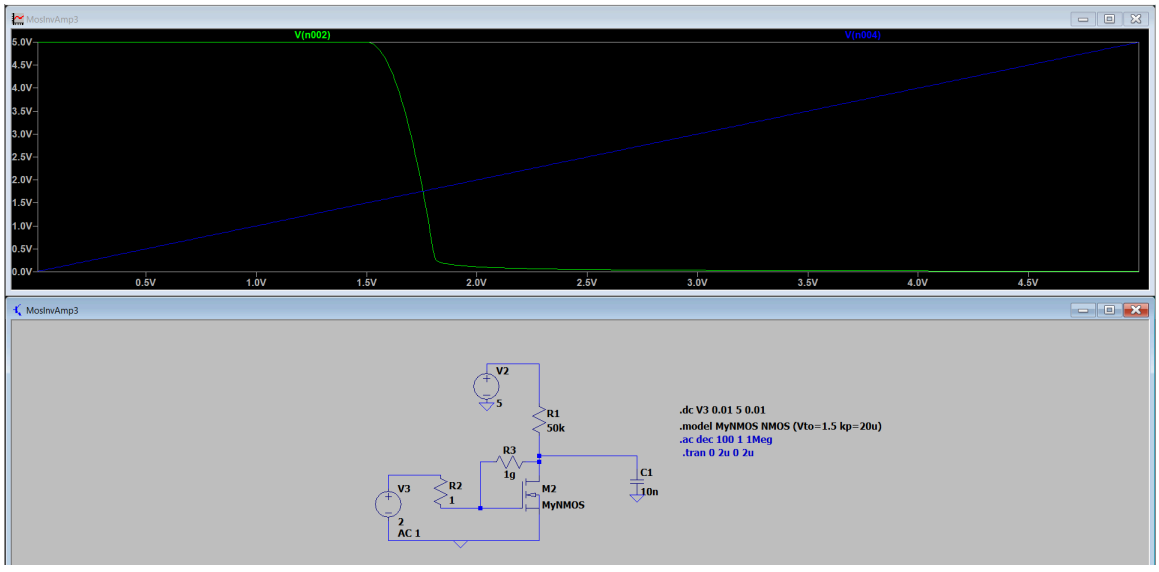
In this case, both devices are being driven with a large pulse input from 0V to 5V. Under these conditions, each transistor is operating primarily as a switch rather than as a small-signal amplifier. When the input is low, both devices are fully off. When the input rises to 5V, both devices are driven well beyond their turn-on thresholds and become fully conducting. Because the pulse amplitude is large compared to both threshold

voltages (0.7V for the BJT and 1.5V for the NMOS), the two circuits behave very similarly in time-domain switching.

To observe a difference in their transient behavior, the input swing would need to be closer to the devices' turn-on voltages. For example, if the pulse ranged from 0V to 1V, the BJT would turn on around 0.7V, while the NMOS would remain off because its threshold voltage would not be reached. In that case, their responses would diverge significantly.

This highlights an important design concept: when input signals are large enough to fully drive a device into saturation or cutoff, differences in device physics become less noticeable. However, when signals operate closer to the threshold region, internal characteristics such as threshold voltage, transconductance, and conduction behavior play a much larger role in shaping the output. In practical amplifier design, choosing device type and input signal range directly determines how the output is constructed.

With the switching behavior understood, I then investigated how adding negative feedback affects the DC, AC, and transient responses. To do this, I modified the NMOS inverter by adding a resistor from the output node back to the input, introducing controlled negative feedback. The first comparison focused on the DC sweep behavior.

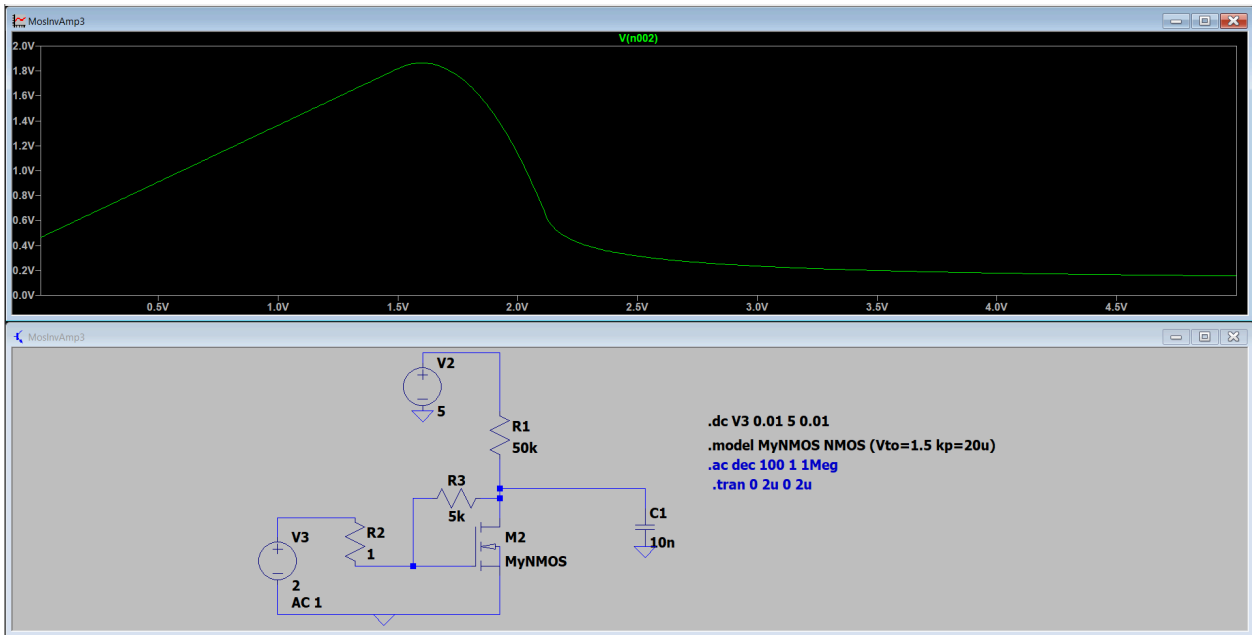


With a feedback resistor of 1 GΩ, the negative feedback is extremely weak. Because the resistance is so large, very little current flows from the output back to the input node. As a result, the DC sweep looks almost identical to the case without feedback.

This behavior makes sense when considering how negative feedback operates. Feedback is most effective when the amplifier is functioning in its active region, where small changes in input produce small, controlled changes in output. However, in this inverter configuration, the NMOS transitions very abruptly once the input crosses the threshold voltage. The device moves quickly from cutoff to conduction, leaving very little gradual region for feedback to influence.

Since the switching behavior is so sharp, the weak feedback resistor does not meaningfully alter the transition. There is simply not enough feedback current to soften or reshape the response.

To observe a noticeable effect, the feedback must be strengthened by lowering the resistance. Reducing the feedback resistor allows more current to flow from the output back to the input, increasing the influence of the feedback network. When the resistor is decreased to 5 kΩ, the DC sweep changes more noticeably.

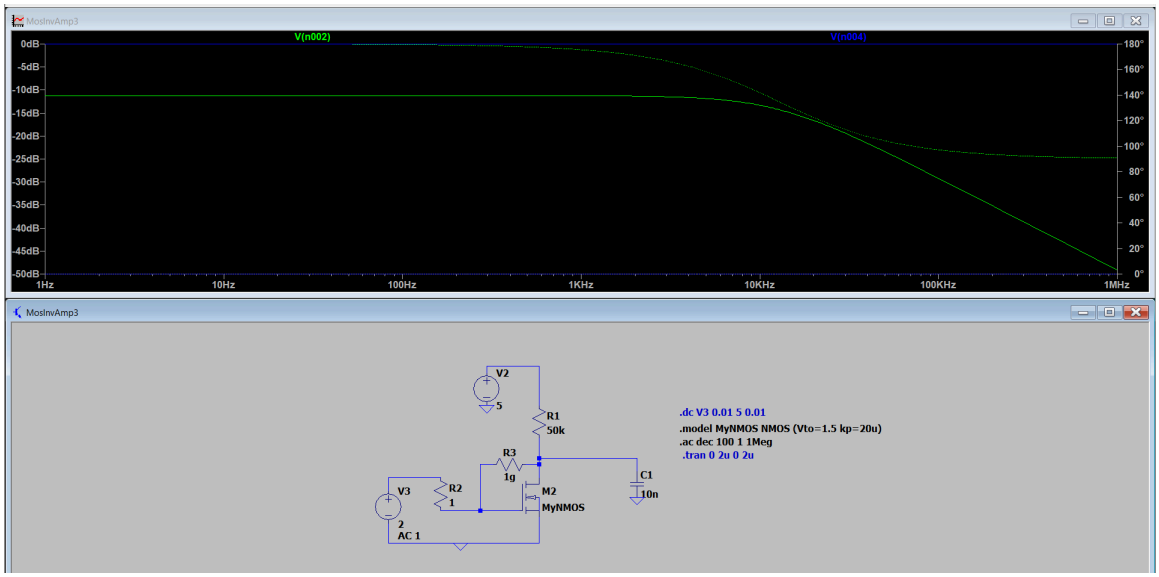


With the feedback resistor reduced to 5 kΩ, the effect of negative feedback becomes much more noticeable. The inverter still switches near the same input voltage (around 1.5V), but the output transition becomes significantly more gradual.

This happens because stronger negative feedback forces the circuit to respond more linearly. As the NMOS begins to turn on and pull current, part of the output voltage is fed back to the input node through the resistor. This feedback partially counteracts the input signal, reducing the effective gate-to-source voltage and slowing the rate at which the transistor turns on.

Instead of a sharp transition from high to low, the switching action is stretched over a wider input range. The result is a smoother and more controlled output fall compared to the abrupt drop seen without feedback. In other words, the feedback softens the switching behavior by opposing rapid changes in the output.

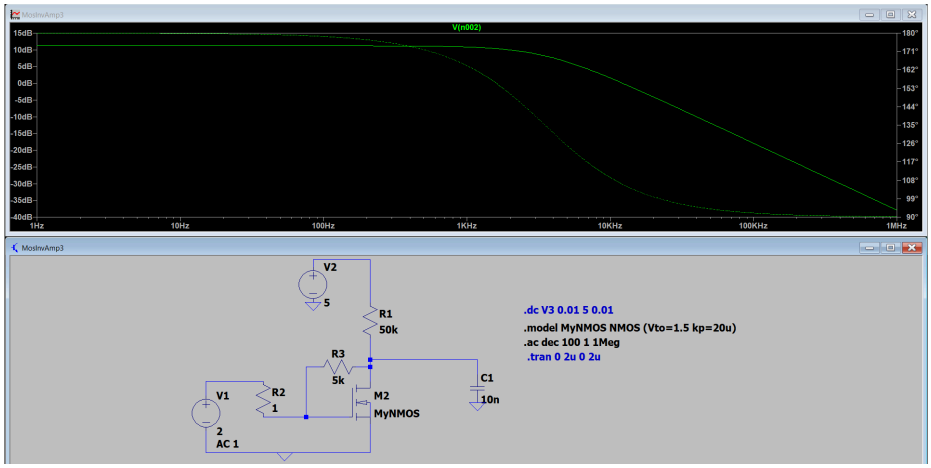
With the DC behavior understood, I then analyzed how the same feedback configuration affects the AC response.



At first glance, the AC sweep with the 1 GΩ feedback resistor appears different from the no-feedback case. However, the behavior is essentially unchanged. The apparent difference comes mainly from the scaling of the phase axis rather than an actual shift in the circuit's response.

This result is consistent with what was observed in the DC sweep. Because the feedback resistance is so large, very little current flows from the output back to the input. As a result, the feedback network has minimal influence on the frequency response.

To see a meaningful change in the AC behavior, the feedback must be strengthened. Reducing the feedback resistor to 5 kΩ allows more feedback current to interact with the input node, increasing its effect on the overall response.



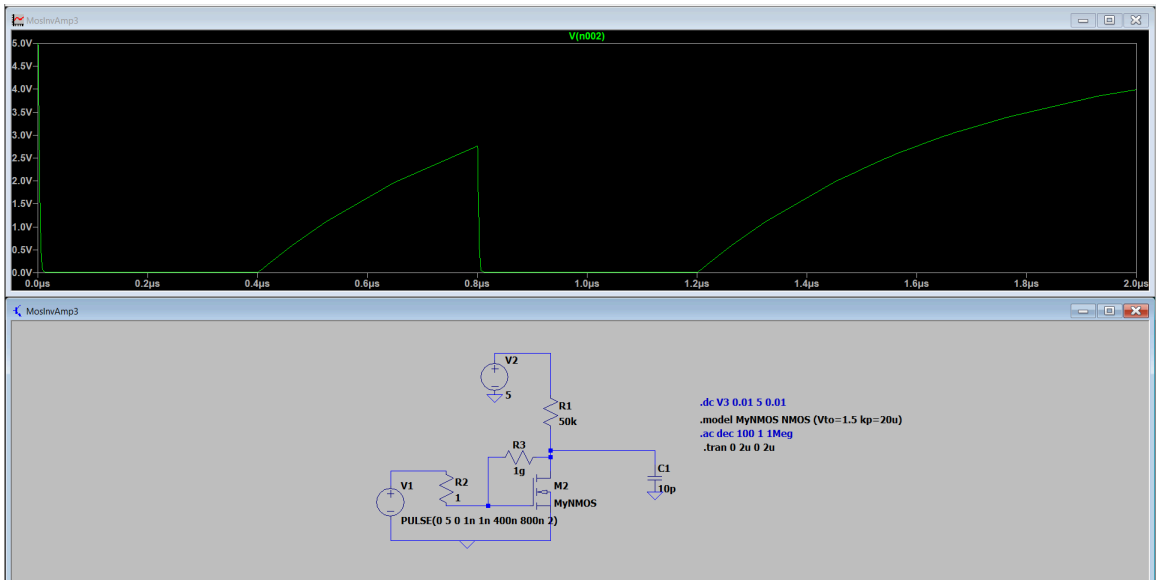
With the feedback resistor reduced to 5 kΩ, more current flows from the output back to the input, and the effect of negative feedback becomes clearly visible in the AC response.

The phase shift now begins earlier, around 100 Hz instead of 1 kHz. Similarly, the magnitude begins rolling off sooner, shifting from roughly 9 kHz in the no-feedback case to about 2 kHz with strong feedback. This demonstrates the classic tradeoff introduced by negative feedback: reduced gain in exchange for improved stability and controlled behavior.

Although the gain begins to drop at a lower frequency, the overall response becomes smoother. Strong feedback forces the output to more closely track the input, flattening the midband response and preventing abrupt changes in magnitude. Instead of a sharp collapse at higher frequencies, the gain decreases more gradually.

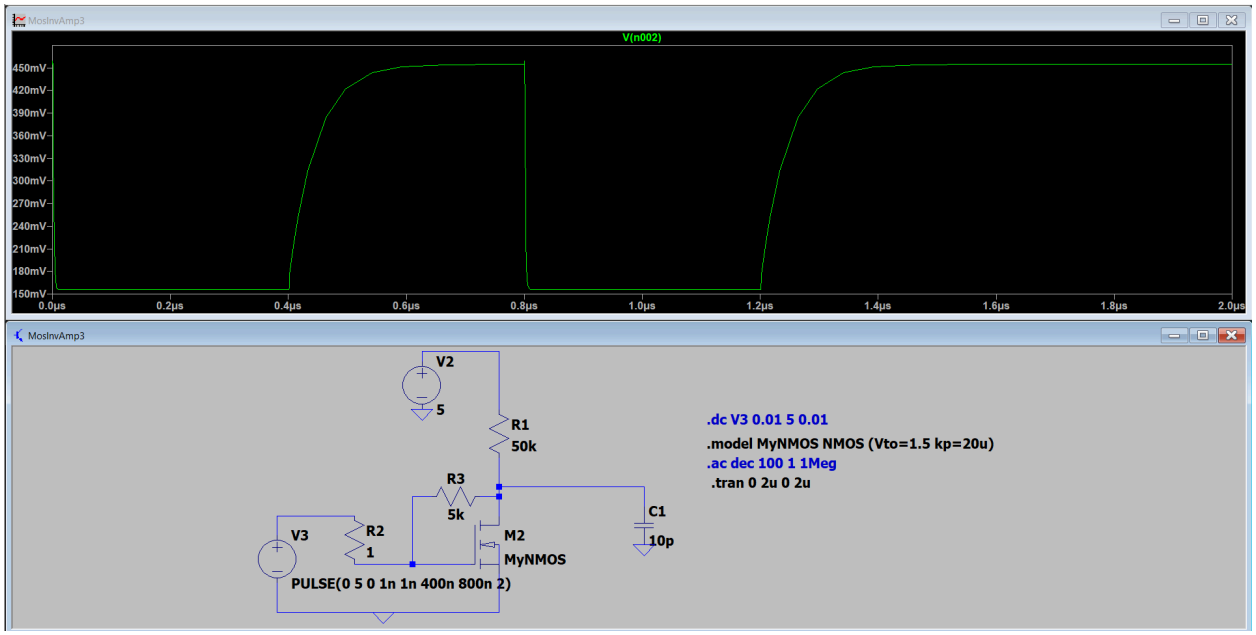
In other words, negative feedback reshapes the entire frequency response. It does not simply reduce gain; it changes the slope and consistency of the response curve, producing a more stable and predictable system.

Next, I analyzed how negative feedback influences the transient response.



With the 1 GΩ feedback resistor, the transient behavior looks almost identical to the case without feedback. This is expected, since the feedback resistance is so large that very little current flows from the output back to the input node. As a result, the feedback network has minimal influence on the switching behavior.

To observe a noticeable change in the transient response, the feedback must be strengthened by lowering the resistance. Increasing the feedback current allows the output to more directly influence the input node. When the resistor is reduced to 5 kΩ, the transient response changes significantly.



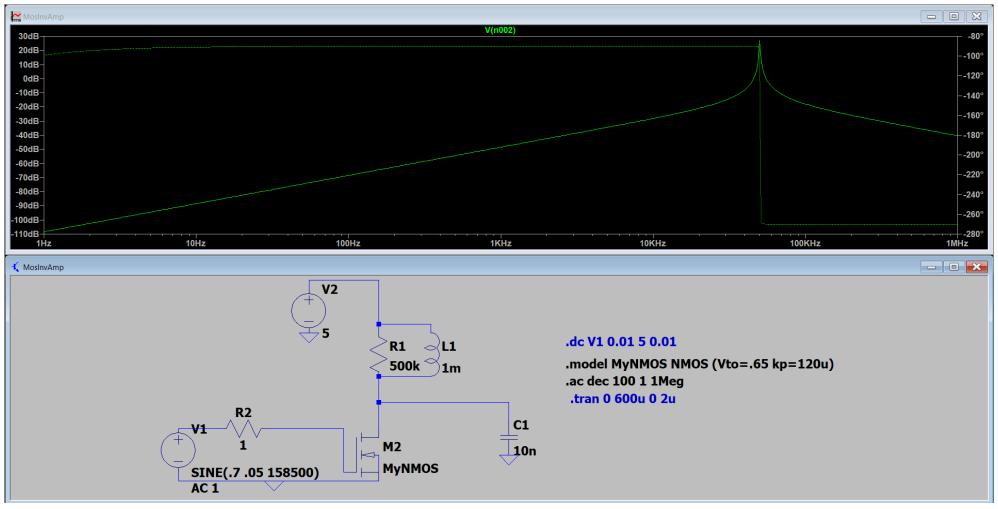
With strong negative feedback, the transient response changes significantly. The output rise becomes much slower and only reaches about 450 mV, compared to approximately 2.7 V without feedback.

This behavior occurs because strong feedback forces the output to closely track the input. As the output begins to rise, part of that voltage is fed back to the input node through the feedback resistor. This reduces the effective gate-to-source voltage of the NMOS transistor. Even while the input pulse is high, the transistor is partially turned on due to this feedback interaction, providing a resistive path to ground.

Because of this partial conduction, the output can no longer freely charge toward the full 5 V supply. Instead, it stabilizes at a much lower voltage. The rise is also slower because the pull-up resistor must charge the output node while simultaneously opposing the current flowing through the partially conducting NMOS.

This demonstrates how strong negative feedback not only smooths transitions but can fundamentally limit output amplitude by dynamically opposing changes in voltage.

Next, I investigated how adding an inductor in parallel with the load resistor affects the frequency response.

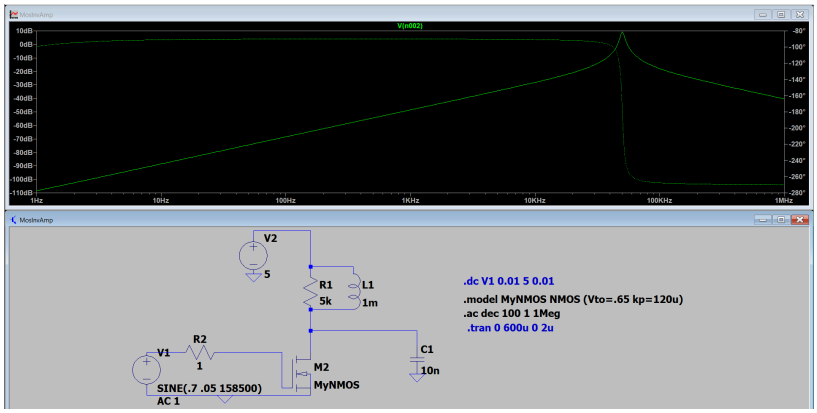


With a 500 kΩ load resistor and a 1 mH inductor in parallel, the AC sweep shows a sharp magnitude peak near 70 kHz, along with a rapid phase shift from approximately –90° to –270°. This behavior indicates resonant behavior in the output network.

At low frequencies, the inductor behaves almost like a short circuit because its reactance XL=2πfL is small. As frequency increases, the inductive reactance increases as well. At a certain frequency, the interaction between the inductor and the circuit capacitance produces a resonance, causing the output magnitude to peak sharply.

Beyond the resonant frequency, the circuit becomes increasingly reactive, and the phase shifts rapidly as inductive effects begin to dominate. The sharpness of the magnitude peak is due to the very large load resistance. With 500 kΩ, there is minimal damping in the network, allowing energy to build up and produce a pronounced resonance.

To better understand how the load resistor influences the resonance, I reduced the parallel resistance to allow more current to flow through the resistor rather than the inductor. The results are shown below.

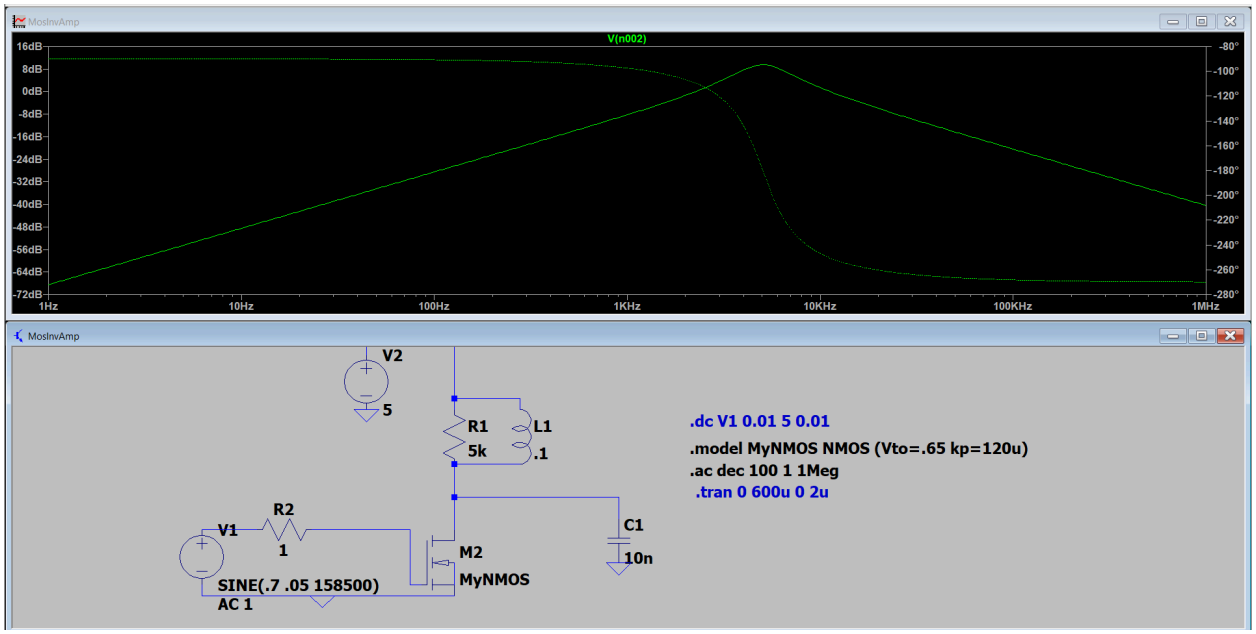


When the load resistor is reduced to 5 kΩ while keeping the same 1 mH inductor, the magnitude peak becomes much less sharp and pronounced. This occurs because a smaller resistor introduces stronger damping into the parallel network.

With a lower resistance, energy stored in the inductor dissipates more quickly through the resistor. As a result, the circuit cannot sustain the sharp buildup of voltage at resonance. The peak flattens, and the gain enhancement at the resonant frequency is reduced. The phase shift around resonance is also less extreme compared to the high-resistance case.

Overall, decreasing the parallel resistance increases damping, smooths the magnitude response, and reduces the severity of the phase transition at resonance.

To further explore how the inductor influences the AC behavior, I then increased the inductance value to observe how shifting the reactive element affects the resonance.



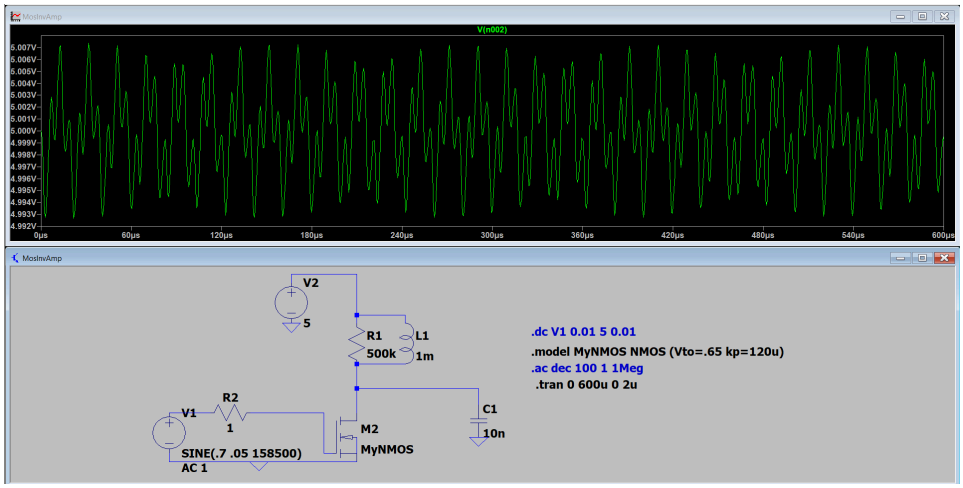
When the inductance is reduced, the resonance becomes much smoother and less pronounced. The magnitude peak flattens, and the phase transition becomes more gradual instead of dropping sharply.

This occurs because a smaller inductor provides less reactive impedance at the frequencies of interest. Since inductive reactance is given by XL=2πfL, reducing L lowers the reactance across the frequency range. As a result, the reactive energy exchange that produces strong resonance is weakened.

With less stored magnetic energy in the inductor, the circuit behaves more like a damped resistive network. The AC response becomes smoother overall, without a sharp gain peak or steep phase shift.

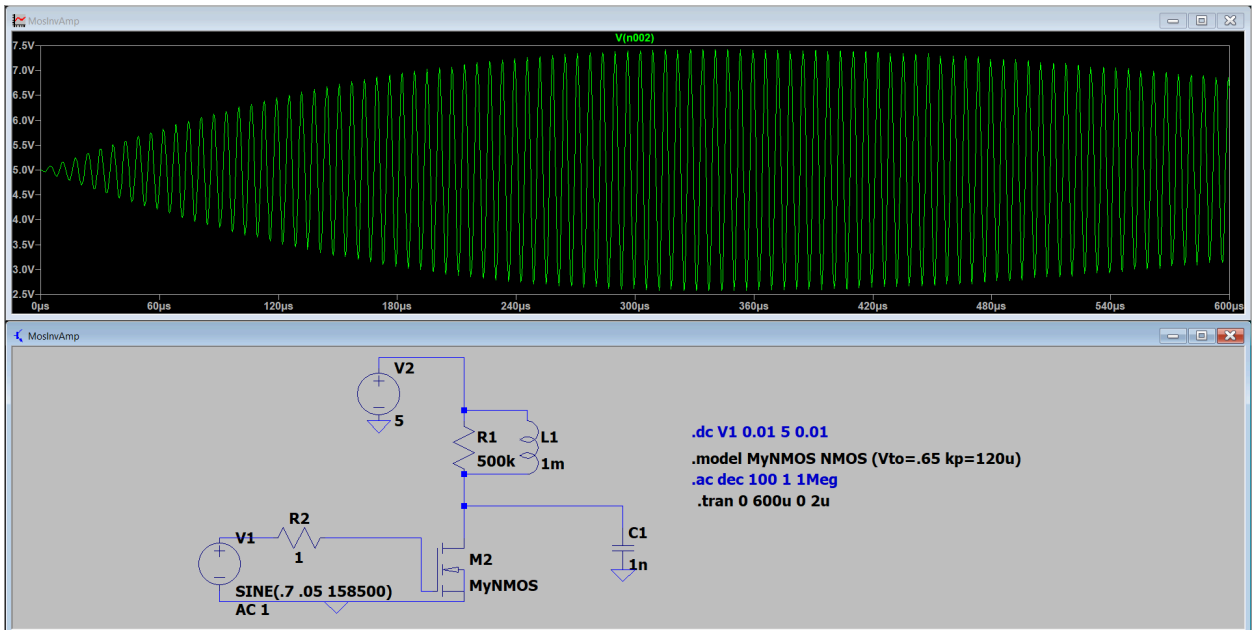
This demonstrates that the inductance value directly controls how strong and how sharp the resonance appears in the frequency response.

After analyzing the AC sweep with the inductor in parallel with the load resistor, I then examined how this configuration affects the transient response. With the load resistor set to 500 kΩ, the circuit exhibited oscillatory behavior, but the magnitude of the oscillations was relatively small.



To better observe the resonance, I reduced the capacitor value from 10 nF to 1 nF. With the original 10 nF capacitor, the RC time constant was large enough that the circuit responded slowly, heavily damping the oscillations. By reducing the capacitance to 1 nF, the time constant decreased, allowing the node to charge and discharge more quickly.

This adjustment made the oscillations more visible and better aligned with the driving input signal. Additionally, a smaller capacitor reduces the amount of capacitive loading at higher frequencies, allowing the LC resonance to dominate more clearly in the transient response.



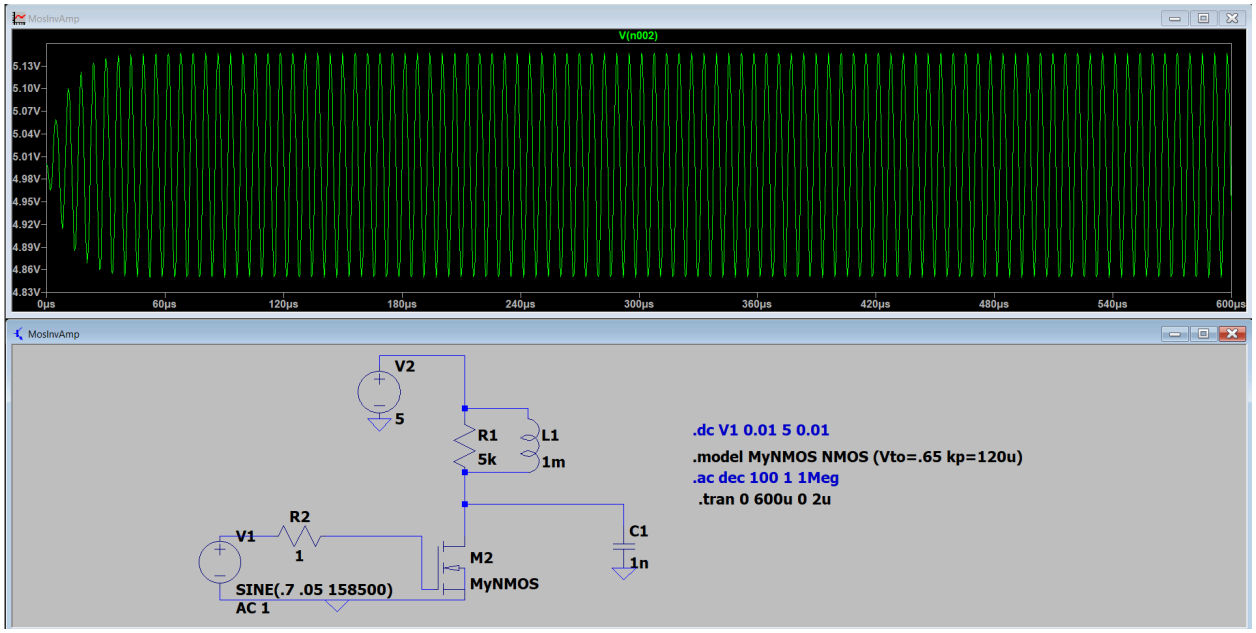
With the capacitor properly sized, the expected resonant transient behavior becomes clearly visible. Using a 500 kΩ load resistor and a 1 mH inductor, the output begins with small oscillations that grow larger with each cycle of the sinusoidal input.

Initially, the amplitude increases because energy is gradually being stored in the LC tank formed by the inductor and capacitor. As the driving frequency approaches the natural resonant frequency of the LC network, energy adds constructively each cycle, causing the oscillations to build.

Around 300 µs, the oscillations reach a peak amplitude, swinging approximately from 2.5 V to 7 V. After reaching this maximum, the amplitude stabilizes briefly (between roughly 300 µs and 400 µs) and then begins to slowly decrease.

This behavior shows that while the LC circuit resonates strongly, it is not lossless. The 500 kΩ load resistor introduces light damping, allowing some energy to dissipate over time. Because the resistance is large, the damping is weak, so it takes many cycles for the energy to build up and many cycles for it to decay once steady-state oscillations are reached.

To observe how damping changes this behavior, I then reduced the load resistance from 500 kΩ to 5 kΩ.



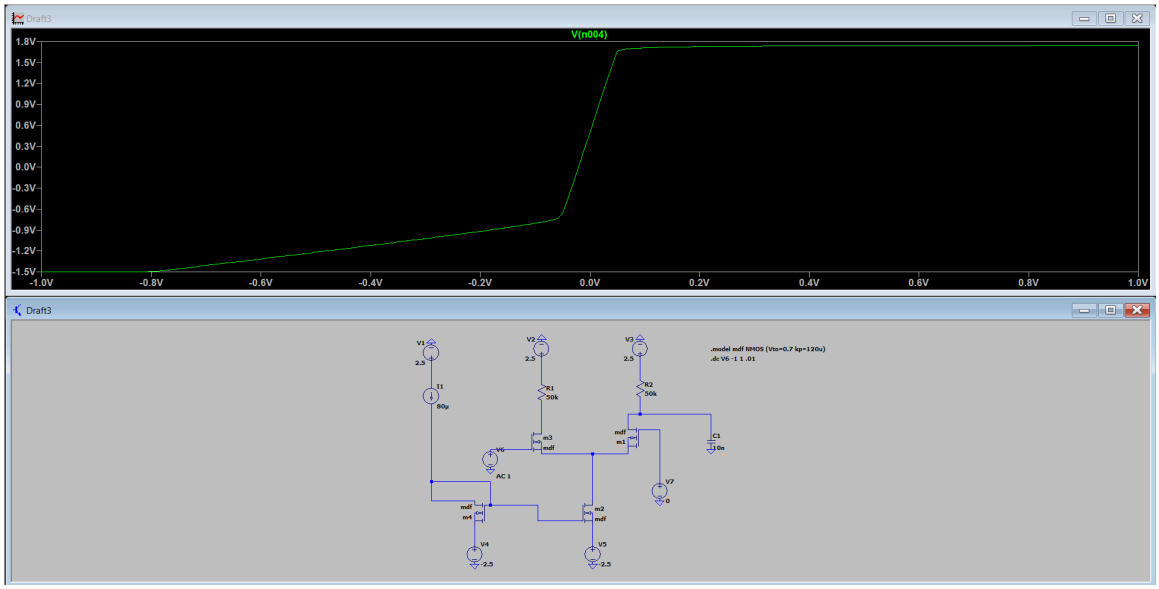
When the load resistor is reduced to 5 kΩ, the transient response changes noticeably. The output reaches steady-state oscillations much more quickly, and the amplitude of the swings is significantly smaller — approximately from 4.85 V to 5.15 V.

After steady state is reached, the amplitude remains very consistent with no noticeable long-term decay. This behavior occurs because the smaller load resistor introduces much stronger damping into the circuit. With lower resistance, energy stored in the LC tank is dissipated more rapidly through the resistor.

As a result, the oscillations build up faster but cannot reach the same large amplitudes seen in the lightly damped case. The circuit is unable to store and sustain as much energy. The stronger damping also prevents long-term ringing, so once steady state is reached, the system settles into a stable and consistent oscillation.

This demonstrates how reducing the load resistance increases damping, tightens the transient response, and limits the peak oscillation amplitude.

After building the MOS differential pair amplifier and running a DC sweep, the output produced the expected S-shaped transfer curve. This characteristic response is typical of a differential pair.



The curve shows a flat region at strongly negative differential voltages, followed by a gradual increase beginning around –0.8 V. Near –0.075 V, the slope increases sharply, and then after crossing 0 V, the curve levels off again more gradually.

This behavior comes from how a differential pair steers bias current between its two transistors depending on the differential input voltage. When the differential input is strongly negative, nearly all of the tail current flows through one transistor, keeping the output relatively flat. As the differential input approaches zero, the current begins transferring more rapidly between the two devices.

The steep transition region near the center of the curve represents the point where the differential pair becomes highly sensitive to small input differences. In this region, small changes in differential voltage produce large changes in output voltage. This narrow transition area is often referred to as the “forbidden zone,” since the circuit quickly shifts from favoring one transistor to the other.

In this simulation, the forbidden zone is centered around 0 V and is relatively sharp rather than wide, indicating strong switching behavior between the two branches of the differential pair.

Conclusion:

Through this project, I explored how inverter-based amplifiers behave across DC, AC, and transient domains. By comparing an NMOS inverter to a BJT inverter, I observed how device physics directly influence switching behavior, gain response, and frequency limitations.

Introducing negative feedback demonstrated how feedback reshapes system behavior; smoothing transitions, improving stability, and trading gain for bandwidth. Adding an inductor in parallel with the load resistor revealed how resonance, damping, and energy storage interact, and how tuning parameters such as inductance and resistance can significantly alter both frequency and time-domain responses.

Finally, simulating a MOS differential pair provided insight into current steering behavior and the sharp transition region near zero differential input. This highlighted why differential pairs are fundamental building blocks in analog amplifier design.

Overall, this study strengthened my understanding of how circuit topology, device characteristics, and reactive components interact to shape amplifier behavior under varying conditions.