Potential Enhancement of f_T and $g_m f_T/I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics

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***Abstract*—The potential for negative-capacitance field-effect transistors (NCFETs) to enhance the unity-current-gain cutoff frequency f_T and $g_m f_T/I_D$ ratio through a technique that mitigates the impacts of extrinsic parasitic capacitances is investigated, where g_m is the transconductance and I_D is the dc drain current, and where "extrinsic" refers to elements arising outside an "intrinsic" or core transistor structure. We explain the technique and show that NCFETs can provide significant gains in extrinsic f_T and $g_m f_T/I_D$ from this mitigation effect. However, an inherent degradation of intrinsic f_T needs to be addressed to maximize these benefits, and this degradation can be alleviated through channel-length scaling as well as supply- and threshold-voltage tuning. The relative influences of different extrinsic parasitic elements are also evaluated, and it is found that improvements to f_T and $g_m f_T/I_D$ increase as extrinsic parasitic capacitance increases and decrease as extrinsic parasitic resistance increases. Overall, this work finds NCFET structures are promising candidates to mitigate the impacts of extrinsic parasitics in aggressively scaled transistors for next-generation RF applications.**

***Index Terms*— Ferroelectric, modeling, negative-capacitance field-effect transistors (NCFETs), scaling, RF.**

I. Introduction

NEGATIVE-capacitance field-effect transistors (NCFETs) are seen as promising next-generation devices because of their abilities to alleviate undesired short-channel effects and decrease subthreshold slope (SS) [1], [2]. Recently, numerous studies have investigated various aspects, including dc, digital, and radio-frequency (RF) performance, of these novel devices. In addition to theoretical studies, promising results of NCFET performance have also been reported experimentally [3], [4].

A major area of interest for NCFETs is their performance potential for RF applications. Towards this end, previous works have extensively examined key small-signal parameters, circuit performance, as well as device-level RF figures-of-merit. In terms of small-signal parameters, NCFETs were found to have higher transconductance g_m [5]–[14], higher gate capacitance C_{gg} [3], [5], [6], [11], [14]–[17], and higher or negative output resistance r_o [6], [7], [8], [12], [15], [17]–[19]. An improved performance in linearity metrics [6], and in various analog circuits has also been found [11], [13], [15], [20]–[23].

At the device level, the unity-current-gain cutoff frequency (f_T), the maximum oscillation frequency (f_{max}), and the $g_m f_T$-to-current ratio ($g_m f_T/I_D$) have been examined [5]–[8], [11], [13], [24]. Specifically, NCFETs were found to have similar f_T compared to baseline MOSFETs due to a simultaneous increase in g_m and C_{gg} [5]–[8], [11], [13], [24], a substantial improvement in $g_m f_T/I_D$ due to higher g_m [5], [6], and a lower f_{max} due to the impacts of the ferroelectric damping parameter ρ [5], [6], [24].

Through these investigations of small-signal parameters and key RF figures-of-merit, one feature that emerged was the simultaneous increase of g_m and C_{gg} compared to baseline MOSFETs, defined in this context as parameters obtained for the device *without* extrinsic parasitic elements, i.e., for an intrinsic or core transistor structure. This allows NCFETs to maintain a similar *intrinsic* cutoff frequency ($f_{T,i}$) compared to MOSFETs, calculated via $f_{T,i} = g_m/2\pi C_{gg}$ [25, Ch. 8], despite having a higher C_{gg} [5], [6], [13].

As we will detail in Section II and as suggested by [14, Fig. 19(a)], the ability to maintain a similar $f_{T,i}$ while simultaneously having a higher C_{gg} enables NCFETs to potentially achieve a higher *extrinsic* cutoff frequency ($f_{T,e}$), i.e., the cutoff frequency found with the effect of all extrinsic parasitic elements included[1], when compared to traditional MOSFETs. As extrinsic parasitic capacitances become increasingly dominant in aggressively scaled nodes [26], [27], the $f_{T,e}$ of traditional MOSFETs will continue to be degraded. Therefore, technologies that can increase resiliency to this degradation by improving $f_{T,e}$ will be important for future RF transistors.

To date, most studies of f_T in NCFETs have focused on the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [7], [11], [13], [24], which is undesirable for circuit applications due to dc leakage currents destabilizing the ferroelectric negative capacitance [2], [28]. Studies using the

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[1]In this study, "f_T" will be used as a synonym for "cutoff frequency," and used when distinction between intrinsic and extrinsic versions of the quantity is not required. In cases where a distinction between intrinsic and extrinsic quantities is important, $f_{T,i}$ and $f_{T,e}$ will be used.

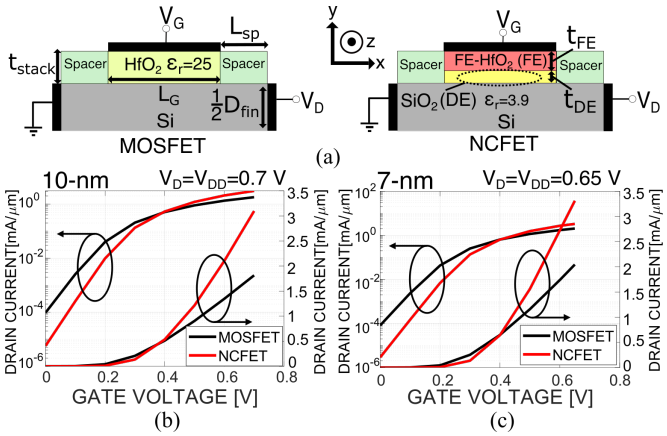


Fig. 1. (a) Schematic diagram of the intrinsic MOSFET and NCFET, where the fin height extends into the z-direction. Only half of the devices are shown, as all device structures are symmetrical. All labels are shared between devices. (b) I_D- V_G results for the 10-nm intrinsic NCFET and MOSFET. (c) I_D-V_G results for the 7-nm intrinsic NCFET and MOSFET.

TABLE I
DEVICE PARAMETERS

Parameter	10-nm node	7-nm node
Gate Length (L_G)	20 nm	16 nm
Fin Width (D_{fin})	7 nm	5.5 nm
Fin Height (H_{fin})	46 nm	50 nm
Spacer Length (L_{sp})	8 nm	6.5 nm
Stack Thickness (t_{stack})	5 nm	4 nm
Effective Oxide Thickness	0.78 nm	0.62 nm
Spacer Permittivity	4.5	4.0
Source and Drain Doping Concentration ($N_{\text{S/D}}$)	10^{20} cm^{-3}	10^{20} cm^{-3}
Channel Doping Concentration (N_{ch})	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}
Low-Field Mobility (μ_{n})	300 cm^2/Vs	340 cm^2/Vs
Velocity Saturation Exponent (β)	2 (electron) / 1 (hole)	2 (electron) / 1 (hole)
Saturation Velocity (v_{sat})	2.1 x 10^7 cm/s	2.1 x 10^7 cm/s
Metal Work Function (ϕ_m)	4.328 eV	4.325 eV
Supply Voltage (V_{DD})	0.7 V	0.65 V
Remnant Polarization (P_r)	0.14 C/m^2	0.14 C/m^2
Coercive Field (E_c)	2×10^8 V/m	2×10^8 V/m
Multidomain Parameter k	10^{-8} m^3/F	10^{-8} m^3/F
NCFET Dielectric Thickness (t_{DE})	0.78 nm	0.62 nm
NCFET Ferroelectric Thickness (t_{FE})	4.22 nm	3.38 nm

more preferrable metal-ferroelectric-insulator-semiconductor (MFIS) structure have examined f_T through simulations [5], [6], [8] and experiments [10], [14], [29] but have not focused on the use of an NCFET to mitigate the impacts of extrinsic parasitics.

Motivated by the opportunity of improving $f_{\text{T,e}}$ for scaled nodes, and the lack of examinations thus far on this promising effect, this study uses physics-based simulations in conjunction with small-signal circuits to understand the limit to which $f_{\text{T,e}}$ can be improved using NCFETs.

We will examine both f_T, as well as $g_m f_T/I_D$, which has recently become prominent as an RF metric [26], [30], especially for analog/RF circuits [26].

This paper is organized into five sections. Section II will lay out a simple analytical view of the mitigation effect. Section III will summarize the methods used for the construction of the NCFET and MOSFET models, including details of the intrinsic models, ferroelectric electrostatics, and extrinsic models. Results with regards to f_T and $g_m f_T/I_D$ will be presented in Section IV, and the conclusions will be stated in Section V.

II. ANALYTICAL MOTIVATION

One intuitive way to understand the extrinsic parasitic mitigation effect is through the analytical formula for $f_{\text{T,e}}$ [31]:

$$f_{\text{T,e}} \approx \frac{1}{2\pi} \frac{g_m}{C_{\text{gg}}+C'_{\text{gg}}+\left[\frac{1}{r_o}\left(C_{\text{gg}}+C'_{\text{gg}}\right)+g_m\left(C_{\text{gd}}+C'_{\text{gd}}\right)\right](R_s+R_d)} \quad (1)$$

where g_m, C_{gg}, and r_o represent the transconductance, gate capacitance, and output resistance taken at the intrinsic terminals (without extrinsic parasitic resistance or capacitances) of the device, C'_{gg} and C'_{gd} represent the extrinsic parasitic capacitances, and R_s and R_d represent the extrinsic parasitic resistances.

Ignoring the effects of the term multiplied by the sum of R_s and R_d, which is typically small compared to the C'_{gg} term, and rearranging the formula, the following result can be obtained:

$$f_{\text{T,e}} \approx f_{\text{T,i}} \frac{1}{1+\frac{C'_{\text{gg}}}{C_{\text{gg}}}}. \quad (2)$$

Since NCFETs can follow the same fabrication procedures as standard MOSFETs, a similar device and layout structure can be used, and the extrinsic parasitic element C'_{gg} can be assumed to be similar between the devices. As seen directly from (2), a form of which first appeared in [14, Fig. 19(a)], the higher intrinsic gate capacitance C_{gg} in NCFETs [5], [6], [11], [14]–[16] will lead to a higher $f_{\text{T,e}}$, since they are expected to have a similar $f_{\text{T,i}}$ to MOSFETs [5]–[8], [11], [13], [24], but the second term in the denominator of (2) will be smaller.

III. METHODOLOGY

A. Intrinsic Device Modeling

1) MOSFET Design and Modeling: MOSFET devices based on the IRDS 10-nm and 7-nm node have been modeled with key parameters picked based on literature values [32]–[39]. A schematic of the intrinsic device can be found on the left side of Fig. 1(a). Simulation of devices have been conducted in the same manner as our previous work, which was calibrated to an experimental device [5]. For this work, the intrinsic MOSFET devices have been calibrated by matching the on-current (I_{on}) and off-current (I_{off}) to high-performance devices in the literature [34], [35], [40] through the adjustment of the low-field mobility μ_n, saturation velocity v_{sat}, and metal work function ϕ_m. Specifically, the 10-nm device has an I_{on} of 1.81 mA/μm, and the 7-nm device has an I_{on} of 2.05 mA/μm. The I_{off} of both MOSFET devices have been set to 100 nA/μm. The drain current (I_D) to gate voltage (V_G) characteristic of the 10-nm and 7-nm device can be found in Figs. 1(b) and (c), respectively, and important simulation parameters for both the 10-nm and the 7-nm device can be found in Table I.

2) NCFET Design: A schematic of the intrinsic NCFET device can be seen on the right side of Fig. 1(a). The NCFET devices have been designed with the same oxide stack height t_{stack} of the reference MOSFETs, because t_{stack} will be limited by the amount of space between fins in advanced nodes [3], [5].

For these NCFETs ferroelectric HfO_2 and SiO_2 have been chosen as the ferroelectric and dielectric layers [4], [41],

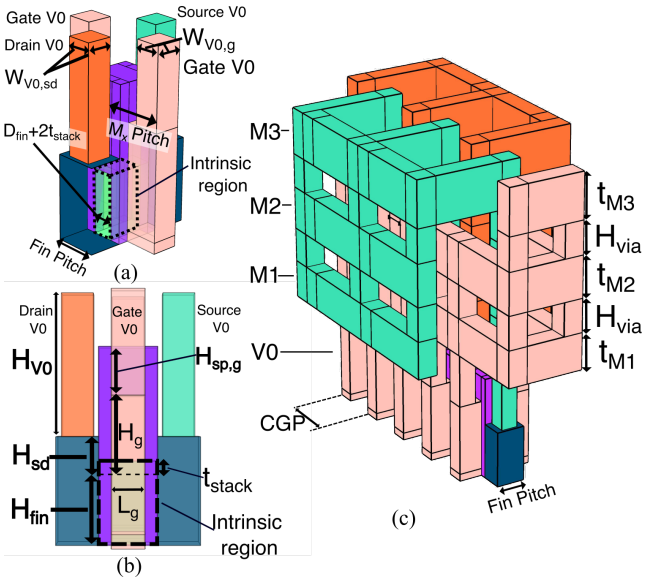


Fig. 2. (a) Perspective view and (b) side view of one fin of the extrinsic structure. (c) 3-D view of the extrinsic structure with interconnects up to M3.

TABLE II
EXTRINSIC STRUCTURE PARAMETERS

Parameter	10-nm node	7-nm node
Fin Pitch	34 nm	27 nm
Contacted Gate Pitch (CGP)	62 nm	51 nm
Gate Height (H_g)	40 nm	40 nm
Source and Drain Height (H_{sd})	20 nm	20 nm
Spacer Height Above Gate ($H_{sp,g}$)	30 nm	30 nm
M_x Pitch	35 nm	28 nm
M_x Width	23 nm	18 nm
V0 Height (H_{V0})	88 nm	88 nm
Source Drain V0 Width ($W_{V0,SD}$)	19.5 nm	16.5 nm
Gate V0 Width ($W_{V0,G}$)	20 nm	16 nm
M1/M2/M3 Thickness (t_{M1}, t_{M2}, t_{M3})	44 nm/50 nm/ 55nm	44 nm/50 nm/ 55nm
Interlayer Via Height (H_{via})	40 nm	40 nm
Interlayer Dielectric Constant	2.5	2.5

respectively. Leakage current through the ferroelectric layer has not been modeled, because it would not destabilize an MFIS NCFET [2], [28], and the magnitude of the leakage current is also shown to be negligible compared to the drain current [4], [9]. The capacitance of the combined ferroelectric-dielectric stack has been selected such that the series combination of the linear ferroelectric negative capacitance [1] and the dielectric layer capacitance is nominally a factor of 3.3 × higher than that of the MOSFET oxide capacitance. This ratio is picked as a compromise between maximizing $f_{T,e}$ and avoiding hysteresis. To clarify, maximizing the ratio, and thus maximizing C_{gg} [5], would maximize $f_{T,e}$ as seen from (2), but a ratio that is too large would require too close a match between the ferroelectric and dielectric capacitances, making the match vulnerable to variations during fabrication, which may inadvertently violate the matching condition [1], [28] required to avoid hysteresis.

While a variety of layer thicknesses, t_{DE} and t_{FE}, and material combinations can be used for the oxide stack [5], it is expected that the results will be the same to first order if the choice made is within the constraints of attaining the nominal capacitance increase of 3.3 × and with realistic materials. This outcome is based on the observation that f_T and $g_m f_T / I_D$ are primarily governed by the final series capacitance combination

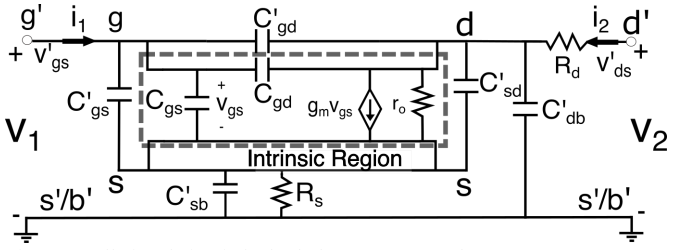


Fig. 3. Small-signal circuit for both the MOSFET and NCFET.

of the ferroelectric and dielectric layers, rather than individual layer thicknesses [5] or specific materials yielding the capacitances. In our case, the value of t_{DE} is chosen to match the SiO_2-normalized effective oxide thickness of the MOSFET.

3) Ferroelectric Modeling and Parameters: The ferroelectric HfO_2 layer in NCFETs has been modeled using the multi-domain Landau-Khalatnikov equation [5], [19], [42], [43], implemented in the same manner as [5]. Ferroelectric parameters α and β have been picked to attain the nominal capacitance ratio as discussed in Section III-A-2, and their values have been calculated using the remnant polarization P_r and coercive voltage E_c of the ferroelectric layer [44]. Out of a variety of possible E_c and P_r value pairs that are consistent with literature ranges [45] and that satisfy the nominal capacitance ratio, the pair that maximizes the width of the negative capacitance region is picked in order to maximize bias ranges in which the device is operating in the negative capacitance region. In addition, these specific values for E_c and P_r are consistent (within 10%) with those obtained experimentally for Sr-doped HfO_2 [46] and are shown in Table I. It is expected that the trends would not qualitatively change provided the *ratio* of E_c to P_r, which dictates the nominal capacitance ratio by dictating the ferroelectric parameter α [44], is similar. Multidomain effects in the form of coupling between adjacent dipoles are modeled using the k parameter [5], [19], [43], [47], picked to be consistent with literature ranges [5], [19], [43], [47], and also shown in Table I.

B. Extrinsic Structure

To model parasitic capacitance and resistance outside of the intrinsic FET region, a representative multi-finger extrinsic structure [48, Ch. 4] comprised of interconnects up to the M3 metal level has been modeled. In the immediate area surrounding the intrinsic region, a raised source and drain structure has been chosen, with parameters obtained from [49]. A schematic diagram of the structure can be seen in Fig. 2, where the intrinsic regions depicted in Fig. 1(a) correspond to a top view of the dashed box in Fig. 2(a).

By connecting five units of the structure depicted in Figs. 2(a) and 2(b) in a row, and building metal lines around them, five gate fingers with one row of fins have been modeled, as shown in Fig. 2(c). Here, two gate contacts have been utilized, and metal lines for each contact have been stacked to minimize resistance. Important parameter values for this overall structure are listed in Table II [32], [33], [35]–[37], [39], [40], [49], [50].

C. Small-Signal Circuits

To find f_T, a small-signal circuit simulation approach is used. The MOSFET and NCFET small-signal circuits follow from [5], and the same methods have been used to extract intrinsic

TABLE III
WIDTH NORMALIZED PARASITIC VALUES

Parameter	10-nm node	7-nm node
$C'_{\rm gs}$	338.24 aF/μm	290.44 aF/μm
$C'_{\rm gd}$	296.95 aF/μm	255.09 aF/μm
$C'_{\rm sd}$	73.81 aF/μm	64.04 aF/μm
$C'_{\rm sb}$	11.33 aF/μm	7.13 aF/μm
$C'_{\rm db}$ ($V_D = V_{\rm DD}$)	8.77 aF/μm	5.60 aF/μm
R_s	96.4 Ωμm	84.0 Ωμm
R_d	96.4 Ωμm	84.0 Ωμm

circuit elements. A diagram of the circuit can be found in Fig. 3. The effects of all important device physics are reflected in the values of the small-signal circuit parameters, e.g., the effects of drain-induced barrier raising in NCFETs is reflected via values of r_o. Note that for this study, the ferroelectric damping resistor and the gate resistance, which have previously been modeled [5], have been omitted. This is done to simplify the simulation procedure, and will not at all alter the results, as it is well-known that the gate resistance does not change f_T [51]. We have also verified through simulations in [5] that a change in the ferroelectric damping parameter ρ does not change f_T.

The extrinsic parasitic capacitances, $C_{\rm gs}^{'}$, $C_{\rm gd}^{'}$, $C_{\rm sd}^{'}$, $C_{\rm db}^{'}$, and $C_{\rm sb}^{'}$ have been obtained in the same way as [5]. The R_s and R_d of 10-nm devices have been obtained by a microscopic Ohm's law [52] simulation of the structure shown in Fig. 2(c), with literature values for resistivities [32], [39], [53], [54]. Specifically, the line resistances for M1, M2 and M3 metal lines are 130 Ω/μm, normalized to the line cross section, and all via resistances are 30 Ω/via [32], [39]. The material of via layer V0 is assumed to be tungsten, and its resistivity taken to be $3 \times 10^{-7} \Omega \cdot \rm cm$ [53]. The contact resistivity between V0 and silicon is set to $10^{-9}\ \Omega \cdot \rm cm^2$, and the epitaxial silicon resistance of the source and drain extension region is set to 20% of the channel resistance, both of which are consistent with literature values [54]. R_s and R_d of the 7-nm devices are obtained by reducing the width-normalized R_s and R_d of the 10-nm devices by 15%, following IRDS predictions [32], [39]. Width-normalized values of the parasitics are listed in Table III.

IV. RESULTS

A. Baseline Results

The f_T of all devices have been extracted through simulation of the small-signal circuit in Fig. 3 and extrapolation of the resulting two-port h_{21} parameter in the range of 100 kHz to 5 GHz. For the discussion of this section, the focus will be on the 10-nm MOSFET and NCFET devices, which suffice to make the initial observations.

The f_T values are plotted versus I_D at a fixed drain voltage of $V_D = V_{\rm DD}$ to allow comparison under the same power consumption, calculated as $P = I_D \times V_{\rm DD}$. This iso-power condition will be used as the basis for comparison throughout this study, as power consumption is equally as important as performance metrics. The I_D values of the MOSFET and NCFET devices are matched by tuning the gate voltage V_G of the NCFET until its I_D matches with that of the MOSFET.

The $f_{\rm T}$ values of the NCFET and MOSFET are shown in Fig. 4(a), with both $f_{\rm T,i}$ (upper two solid lines) and $f_{\rm T,e}$ (lower two dashed lines) displayed. Here, the right-most points for both

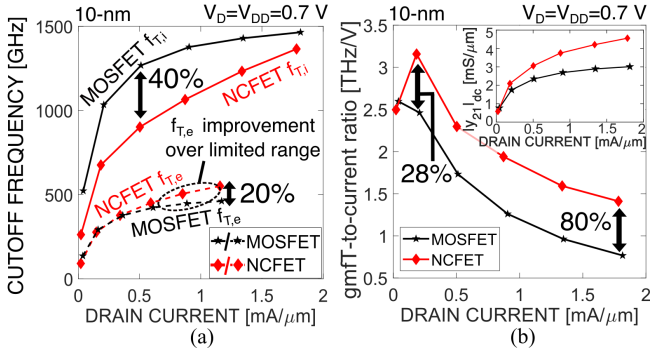


Fig. 4. (a) $f_{\rm T,e}$ and $f_{\rm T,i}$ of the 10-nm MOSFET and NCFET. (b) $g_m f_T/I_D$ for the 10-nm MOSFET and NCFET. Inset: $|y_{21}|_{\rm dc}$ of devices.

sets of lines correspond to the maximum possible V_G, i.e., $V_G = V_D = V_{\rm DD}$, and hence the $f_{\rm T,e}$ lines do not extend as far as the $f_{\rm T,i}$ lines because R_s and R_d limits I_D at maximum V_G and V_D. As seen from the dashed lines, the peak $f_{\rm T,e}$ of the 10-nm NCFET is 20% higher than that of the MOSFET, demonstrating the ability for NCFETs to improve $f_{\rm T,e}$ by mitigating the effects of parasitic capacitances, following the basic premise from (2), i.e., with the NCFET sustaining $f_{\rm T,i}$ but with its higher intrinsic gate capacitance $C_{\rm gg}$ used to mitigate the usual degradation of $f_{\rm T,e}$ from $f_{\rm T,i}$ due to $C_{\rm gg}^{'}$. We will explore this outcome in detail, but first note that this 20% improvement is comparable to the improvement in peak $f_{\rm T,e}$ when technology advances to the next node in planar technologies [27]. For FinFETs, excessive parasitic capacitance causes peak $f_{\rm T,e}$ to degrade as nodes advance, and 20% improvement would be sufficient to bring the peak $f_{\rm T,e}$ back to similar levels of a prior node [27]. We also note that in many prior simulation works [5]–[8], [11], this type of increase in $f_{\rm T,e}$ was not prominently observed because there were only small amounts of parasitic capacitances included outside of the intrinsic device. However, this type of improvement in $f_{\rm T,e}$ *was* observed in [10], where measurements were done on an experimental structure, which would include numerous parasitic components.

Comparison of $g_m f_T/I_D$ can be seen in Fig. 4(b). Here, $g_m f_T/I_D$ is calculated via $|y_{21}|_{\rm dc} \times f_{\rm T,e}/I_D$, where $|y_{21}|_{\rm dc}$ is the transconductance including parasitic elements and is found via the magnitude of the y_{21} parameter of Fig. 3 at dc. As seen from Fig. 4(b), the NCFET displays a significant improvement of $g_m f_T/I_D$ of up to 80%, owing to both the improvements in $f_{\rm T,e}$ and in $|y_{21}|_{\rm dc}$, the latter of which is directly related to the well-known improvements of g_m in NCFETs.

One undesirable feature apparent from Fig. 4(a) is a general reduction of $f_{\rm T,i}$ in NCFETs; from (2), even if NCFETs offer a decrease in the $C_{\rm gg}^{'}/C_{\rm gg}$ ratio, improvement in $f_{\rm T,e}$ is diminished if $f_{\rm T,i}$ decreases. As seen from the solid curves in Fig. 4(a), the $f_{\rm T,i}$ of the 10-nm NCFET is 40% lower than that of the reference MOSFET at $I_D = 0.5\ \rm mA/\mu m$, and this disparity in $f_{\rm T,i}$ continues to increase for lower bias currents. This reduction limits performance potential by limiting the bias ranges in which the NCFETs would display an improved $f_{\rm T,e}$, as seen in the dotted lines of Fig. 4(a). Stemming from the reduction in $f_{\rm T,i}$, the $g_m f_T/I_D$ of the NCFETs is also hindered

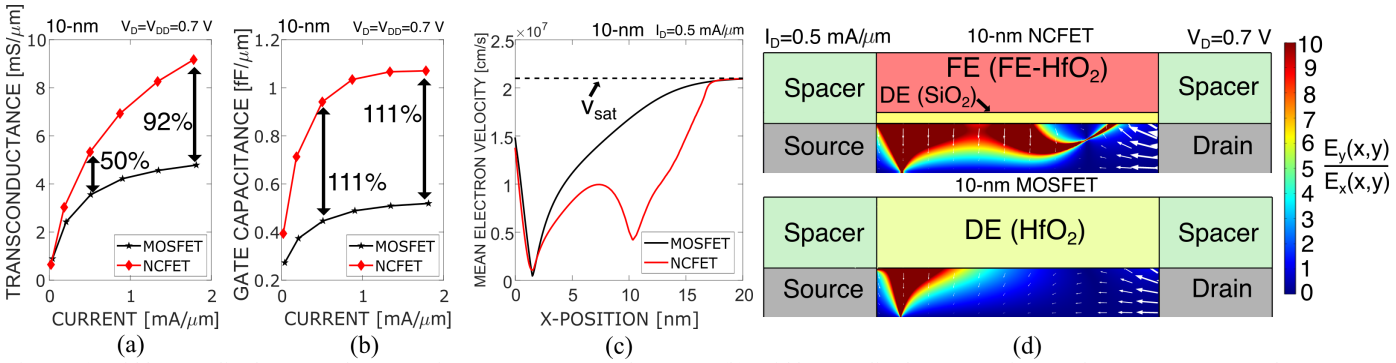


Fig. 5. (a) Width-normalized transconductance of 10-nm MOSFET and NCFET. (b) Width-normalized gate capacitance of 10-nm MOSFET and NCFET. (c) Average electron velocity of 10-nm MOSFET and NCFET, at $I_D = 0.5$ mA/μm. (d) Electric-field ratio of 10-nm MOSFET and NCFET, at $I_D = 0.5$ mA/μm. Arrows represent electric-field lines. Only the top half of each device is shown; the bottom half is symmetrical to that of the top half.

at lower currents. As seen from Fig. 4(b), the NCFET $g_m f_T / I_D$ is only 28% higher than the MOSFET when comparing at the low current corresponding to the peak values, and the NCFET $g_m f_T / I_D$ drops below the MOSFET at ultra-low currents. Overall, this reduction of $f_{T,i}$ is caused by the unique electrostatics of the NCFET, which will be further discussed in the next section.

B. Intrinsic Analysis

1) $f_{T,i}$ Degradation: The reduction of $f_{T,i}$ observed in Fig. 4(a) is echoed in the behavior of the g_m and C_{gg} of the intrinsic NCFET and the MOSFET. As seen in Figs. 5(a) and (b), at low bias ($I_D = 0.5$ mA/μm), g_m is only increased by 50% in the NCFET, whereas C_{gg} is increased by 111%; for higher biases ($I_D = 1.8$ mA/μm), this situation improves, and the g_m increase of 92% is close to the C_{gg} increase of 111%. Since $f_{T,i}$ is calculated via a ratio between g_m and C_{gg} [25, Ch. 8], this results in a large reduction of the NCFET $f_{T,i}$ at low biases, and a smaller reduction at high biases, as seen in Fig. 4(a).

This phenomenon can be explained by the unconventional electrostatics of the NCFET, which has been examined in numerous studies in terms of improvement of drain-induced barrier lowering (DIBL) and r_o, e.g., [3], [4], [12], [18], [47], [55], [56], and which originates from the *de*-amplification of channel potential near the drain side of the channel [18] due to a combination of fringing field from the drain and the negative capacitance of the ferroelectric.

This electrostatic effect can be considered as causing the NCFET to *electrically behave* like a longer channel device compared to a reference MOSFET, with the NCFET electrostatics *effectively* increasing the channel length, despite both devices having the same *physical* channel length.

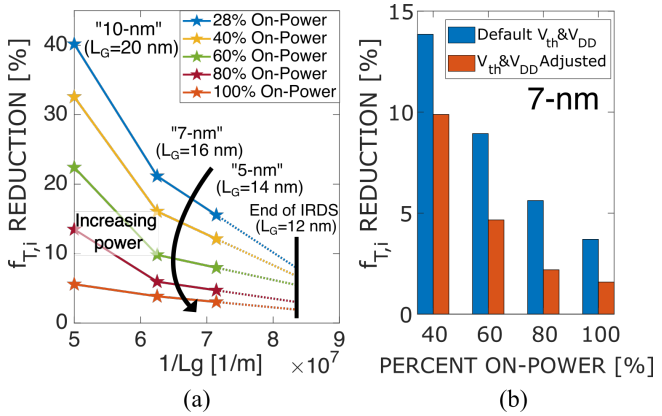
Device characteristics, such as electron velocity and electric field distribution, support this concept of a higher effective channel length. As seen in Fig. 5(c), the NCFET has a lower electron velocity compared to the MOSFET, which has also been previously observed in [8]. Further, as seen in Fig. 5(d), the gate-direction (vertical in the figure) electric field is more dominant across a larger portion of the channel in the NCFET. Both these characteristics are consistent with the notion of an effectively longer channel. Overall, this effective increase in channel length from NCFET electrostatics can be used to intuitively explain the degradation of $f_{T,i}$ in NCFETs, analogous to the well-known effect where a longer physical channel leads to a decrease of $f_{T,i}$.

To explain the bias dependence of the degradation of $f_{T,i}$, the concept of gate control versus drain control can be utilized. At lower currents, and hence lower V_G, the drain dominates channel electrostatics. Since $f_{T,i}$ degrades due to the unconventional drain electrostatics explained earlier, the disparity between $f_{T,i}$ value is high in this region of operation. As current increases, the gate starts to control channel electrostatics, and the two $f_{T,i}$ values start to converge.

2) Strategies for Overcoming the $f_{T,i}$ Discrepancy: To overcome the undesirable $f_{T,i}$ degradation in NCFETs, which limits the $f_{T,e}$ performance benefits, two strategies will be discussed here, which will be tested via simulations in subsequent subsections. While we will only discuss two potential strategies here, we note there may be other device tuning strategies (e.g., tuning of channel mobility [14]).

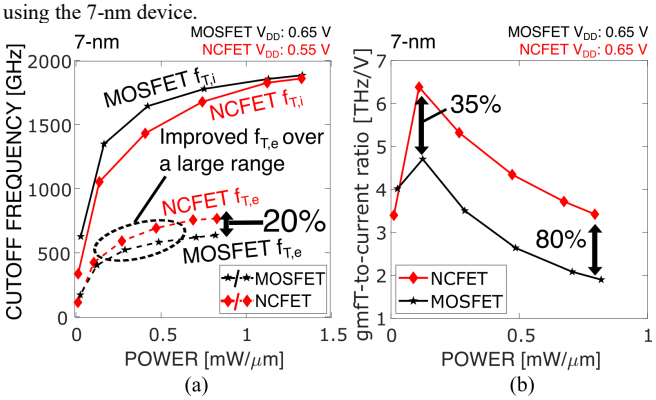
First, consider downscaling of the physical channel length L_G, which will decrease the disparity in $f_{T,i}$ between the NCFET and MOSFET. In previous studies [4], [55]–[57], it was observed that both DIBL and SS of NCFETs, while improved over MOSFETs, will still increase as L_G decreases at very short channel lengths, i.e., that short-channel effects affect NCFETs in a similar way compared to standard MOSFETs. Therefore, as L_G decreases, a larger proportion of the channel will become velocity saturated for both the MOSFET and the NCFET, and the electron velocities of both devices will eventually converge towards the limit of a fully velocity-saturated channel. This convergence of velocities will in turn decrease the difference in $f_{T,i}$ between the devices, with the $f_{T,i}$ values both approaching the fully velocity-saturated limit of $1.5 \times v_{sat}/2\pi L_G$ [25, Ch. 8].

Second, as seen from Fig. 4(a), $f_{T,i}$ is higher for devices operating at higher I_D, which can also be exploited to alleviate the degradation of $f_{T,i}$ in NCFETs. Since NCFETs have a much lower I_{off} than that of the baseline MOSFET, as seen in Fig. 1, their threshold voltage V_{th} can be lowered without compromising standby power versus MOSFETs, which will allow for an increase in I_D for a given V_G. This increase in current will in turn increase $f_{T,i}$, as seen from Fig. 4(a). However, lowering V_{th} alone will not be sufficient, as a higher I_D at the same V_{DD} will increase the power consumption of the NCFET above the MOSFET, which will violate the basis of iso-power comparison as discussed in Section IV-A. Hence, it is also necessary to simultaneously decrease V_{DD} in the NCFETs along with their V_{th}.



(a) (b)

Fig. 6. (a) Changes in $f_{T,i}$ reduction in the intrinsic NCFET vs. the MOSFET as channel length scales down for different levels of operating power, extrapolated linearly to the end of the IRDS. (b) Differences in $f_{T,i}$ reduction between default NCFET and NCFET with adjusted V_{th} and V_{DD}, demonstrated using the 7-nm device.



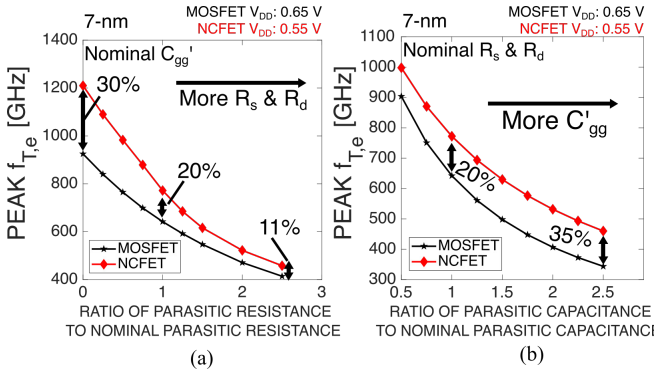
(a) (b)

Fig. 7. (a) $f_{T,e}$ and $f_{T,i}$ for 7-nm device with adjusted V_{th} and V_{DD} for the NCFET; a much greater range of improvement in $f_{T,e}$ can be observed compared to Fig. 4(a). (b) $g_m f_T/I_D$ for 7-nm device with normal V_{th} and V_{DD}.

3) Scaling Effects: To investigate the first of the above two strategies, i.e., how L_G scaling affects $f_{T,i}$, an intrinsic device at the 5-nm node is simulated in addition to the 10- and 7-nm devices. Since dimensions for the 5-nm node are scarce, a representative 5-nm device was built with parameters derived from the 7-nm parameters in Table I, by scaling each dimension by 0.87× to 0.9×, consistent with trends in the IRDS [32], [39].

To visualize the effects of L_G scaling, the reduction of $f_{T,i}$ in NCFETs for various operating powers as a function of gate length is plotted in Fig. 6(a), with the top-left point corresponding to the 40% seen in Fig. 4(a). As seen from the figure, as L_G scales down, the disparity in $f_{T,i}$ decreases, and this effect is especially prominent for devices operating at low powers. Therefore, aggressive L_G scaling will be beneficial in maximizing the $f_{T,e}$ benefits of NCFETs, as it alleviates the undesirable effects from the reduction of $f_{T,i}$.

4) V_{th} and V_{DD} Adjustment: As discussed in the Section IV-B-2, another strategy of decreasing the disparity in $f_{T,i}$ between the NCFET and MOSFET is to simultaneously decrease the V_{DD} and V_{th}. To investigate this approach, we have adjusted the V_{th} of the 7-nm NCFET device in Fig. 1(c) such that I_{off} of the NCFET matches up with the MOSFET, and have lowered V_{DD} from 0.65 V to 0.55 V, corresponding to the predicted value for the end of the IRDS [32], [39]. The result of this adjustment can be seen in Fig. 6(b), where the V_{th} and V_{DD} adjusted devices have attained minor improvements of $f_{T,i}$, primarily for devices operating at high operating power. Overall, this is an additional strategy that can maximize the $f_{T,e}$ benefits of the NCFET. However, since the improvement to $f_{T,i}$ is small, this adjustment will not maximize $g_m f_T/I_D$, as the detriment of the increase in I_D will outweigh the benefits of the increase in $f_{T,e}$.



(a) (b)

Fig. 8. Peak $f_{T,e}$ for 7-nm devices with adjusted V_{th} and V_{DD} for various (a) R_s and R_d, and (b) C'_{gs} and C'_{gd}, normalized to the nominal values seen in Table III.

C. Extrinsic Analysis

1) Nominal Parasitic Results: To examine the effects of extrinsic parasitic elements on the potential for NCFETs to provide enhancements of $f_{T,e}$, 7-nm devices with nominal extrinsic elements will be used as the baseline for comparison. The 7-nm devices are used because as discussed in Section IV-B, the NCFETs will have less degradation in $f_{T,i}$, which will lead to more pronounced performance benefits for $f_{T,e}$. To further maximize the performance of NCFETs, V_{DD} and V_{th} adjustment according to Section IV-B-4 will also be applied to devices that are used for the comparison of f_T, but not to devices that are used for the comparison of $g_m f_T/I_D$. This approach will demonstrate the best-case performance potential for each figure-of-merit.

The f_T and $g_m f_T/I_D$ of these 7-nm devices can be seen in Fig. 7. Since some comparisons are done for devices operating at different V_{DD}, the x-axis has been changed from current to power. As seen in Fig. 7(a), the improvement of $f_{T,e}$ for NCFETs occurs across a larger bias range compared to the 10-nm devices in Fig. 4(a) due to less disparity in $f_{T,i}$ between the devices. Similarly, as seen in Fig. 7(b), the $g_m f_T/I_D$ performance is also better for the 7-nm devices at lower power, and the improvement in $g_m f_T/I_D$ increased from 28% to 35% at the peak value.

2) Effect of Extrinsic Parasitic Resistances: As downscaling of devices continue, one of the most important engineering challenges is the reduction of the extrinsic parasitic resistances of the source and drain, R_s and R_d. To investigate the effect of these extrinsic parasitic resistances on the degree of advantage NCFETs can provide, we have varied the values of R_s and R_d between the ideal value of 0 Ω and 2.5 × the nominal value shown in Table III. Throughout this test, the extrinsic parasitic capacitances C'_{gs} and C'_{gd} have been kept at their nominal values, and the results of peak $f_{T,e}$ can be found in Fig. 8(a). As seen in the figure, the extrinsic parasitic resistances can hinder the improvement of $f_{T,e}$ offered by NCFETs, with a 30% improvement of peak $f_{T,e}$ in the ideal case decreasing to 20% at the nominal extrinsic parasitic resistances, and 11% at 2.5 × the nominal value. Similarly, we found the maximum improvement in $g_m f_T/I_D$ is reduced from 144% in the ideal case to 80% in the nominal case, and 60% at 2.5 × the nominal value. These

reductions occur because higher R_s and R_d lower the peak operating current of both devices, which in turn lowers peak power. Since the $f_{\mathrm{T,i}}$ of NCFETs suffer a greater degradation at lower powers as seen from Fig. 7(a), the peak $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ boost degrades as R_s and R_d increases.

3) Effect of Parasitic Capacitances: Another important extrinsic factor to consider is capacitance, which is highly layout dependent. To investigate the effects of extrinsic parasitic capacitances on the potential benefits of the NCFET, we have swept the values of C'_{gs} and C'_{gd}, the dominant extrinsic parasitic capacitances, between 0.5× and 2.5 × of the nominal values shown in Table III. The result for the peak $f_{\mathrm{T,e}}$ of the 7-nm V_{th} and V_{DD} adjusted device can be seen in Fig. 8(b), where the *x*-axis is the ratio between a potentially achieved extrinsic parasitic gate capacitance C'_{gg} and the nominal value calculated using the sum of C'_{gs} and C'_{gd} in Table III. As seen from the figure, benefits of the NCFET from mitigating the effects of parasitic capacitances will be more pronounced if the extrinsic parasitic capacitance is large, a result consistent with [14, Fig. 19(b)]. In our tests, NCFETs can provide up to 35% of peak $f_{\mathrm{T,e}}$ improvement if extrinsic parasitic capacitance is high and the extrinsic parasitic resistances are kept at nominal values. In this case, up to 98% of $g_m f_T/I_D$ improvement can also be observed. These enhancements of peak $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ show that an NCFET structure will be more beneficial in mitigating extrinsic parasitics for RF performance as scaling continues, where extrinsic capacitance from high-density interconnects is expected to increase [27].

V. Conclusion

With our key results in Figs. 4 – 8, the following conclusions can be drawn from this study that investigates the potential for NCFETs to offer improvements to f_T and $g_m f_T/I_D$ by mitigating extrinsic parasitic capacitances:

1) The basic idea of mitigation is to achieve a similar intrinsic cutoff frequency $f_{\mathrm{T,i}}$ with the NCFET, but a higher extrinsic cutoff frequency $f_{\mathrm{T,e}}$, by leveraging a higher intrinsic gate capacitance C_{gg} to mitigate the extrinsic gate capacitance $C_{\mathrm{gg}}^{'}$, as shown via (2).
2) The $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ of an NCFET can be improved by up to 20% for $f_{\mathrm{T,e}}$ and up to 80% for $g_m f_T/I_D$ for our 10-nm devices, as shown in Fig. 4.
3) The increases of $f_{\mathrm{T,e}}$ in NCFETs is accompanied by a decrease of $f_{\mathrm{T,i}}$, shown in Fig. 4, which is a result of the ferroelectric electrostatics near the drain that effectively increases the channel length of NCFETs, as shown in Fig. 5. Two ways of alleviating this reduction of $f_{\mathrm{T,i}}$, via channel length scaling, and via adjustments to V_{th} and V_{DD} of the NCFET, were discussed, with results shown in Fig. 6.
4) Utilizing 7-nm devices with nominal characteristics shown in Fig. 7, we find that higher extrinsic parasitic resistances may decrease the benefits provided by NCFETs, as shown in Fig. 8(a), emphasizing the importance of keeping these resistances as low as possible.
5) The performance gain seen in NCFETs is more pronounced as extrinsic parasitic capacitances increase, as shown in Fig. 8(b). Hence, the benefits of using NCFETs to increase $f_{\mathrm{T,e}}$ will increase as scaling continues, due to increases in extrinsic parasitic capacitances [27].

Overall, this study demonstrates the potential for NCFETs to bring substantive gain in f_T and $g_m f_T/I_D$ from mitigating the effects of extrinsic parasitic capacitances. As the transistors for RF applications continue to advance, the use of smaller nodes will naturally help to alleviate the issue of $f_{\mathrm{T,i}}$ degradation in NCFETs that might otherwise limit the mitigation. Further, as the field of NCFETs advance, other methods of alleviating the $f_{\mathrm{T,i}}$ reduction (e.g., mobility enhancement [14]) may also emerge. Finally, the expected increase of extrinsic parasitic capacitances for future nodes [27] will also enhance the benefits of NCFETs. Given the encouraging experimental work done on NCFETs thus far [3], [4], this work thus finds promise for NCFET structures in significantly reducing the impact of extrinsic parasitics for next-generation RF applications.

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