RF Performance Projections of Negative-Capacitance FETs: f_T, $f_{\max}$, and $g_m f_T / I_D$

Ji Kai Wang, *Student Member, IEEE*, Prasad S. Gudem, *Senior Member, IEEE*, Thomas Cam, Zhi Cheng Yuan, Michael Wong, Kyle D. Holland, *Member, IEEE*, Diego Kienle, and Mani Vaidyanathan, *Senior Member, IEEE*

***Abstract* — As continuous development and optimization of negative-capacitance field-effect transistors (NCFETs) are pursued for digital applications, it is desirable also to examine the radio-frequency (RF) performance of these devices, especially devices with the metal-ferroelectric-insulator-semiconductor (MFIS) structure. In this paper, we use a combination of physics-based modeling and small-signal circuits to investigate the RF performance of MFIS NCFETs using three key device figures of merit: the well-known unity-current-gain (cut-off) frequency f_T and the well-known maximum oscillation frequency $f_{\max}$, and another important metric specified by $g_m f_T / I_D$, where g_m is the transconductance and I_D is the dc drain current. We find that MFIS NCFETs achieve similar f_T and $f_{\max}$ performance to conventional MOSFETs, but offer a significant advantage in $g_m f_T / I_D$.**

***Index Terms*—Ferroelectric, modeling, negative-capacitance field-effect transistors (NCFETs), scaling, RF.**

I. Introduction

Ferroelectric negative-capacitance field-effect transistors (NCFETs) have been proposed as candidates for future low-power nanoelectronics since 2008 [1], based on their potential of continuing supply-voltage scaling via amplification of the applied gate voltage. Recently [2], the integration of NCFETs into an advanced industrial node, and the demonstration of performance improvements of ring oscillators employing them over conventional FinFETs, points to the continuing promise of NCFET technology for digital circuit applications.

While demonstrations and investigations of the dc and digital behavior of NCFETs are abundant in the literature, the radio-frequency (RF) potential of NCFETs has not yet been thoroughly investigated. Investigation into this direction is important for future RF applications of NCFET technology.

Thus far, numerous studies [2]-[22] have made observations on a number of individual small-signal quantities for NCFETs that could impact their overall RF performance. Specifically, increases in the input capacitance C_{gg} [2]-[10], transconductance g_m [5], [8], [10]-[17], and output resistance r_o [8]-[9], [12], [14], [18]-[22] have been observed. Furthermore, numerous studies [6], [8]-[9], [11], [14], [20]-[23] have noted the possibility of negative differential resistance (NDR) in NCFET output characteristics. Temperature-dependent effects of these parameters have also been examined in the context of self-heating [23] and temperature-dependent parasitic capacitances [11]. A possibility of improved RF performance by controlling NDR through asymmetrical parasitic capacitances has also been proposed [14].

Beyond individual small-signal parameters, a few papers have also examined the overall RF potential of NCFETs through simulations [10]-[11], [16], [20], [23]-[26], and experiments [12]. For device-level figures of merit, similar or superior values of the unity-current-gain (cut-off) frequency f_T have been observed [10]-[12], [16], [23], and in terms of the maximum oscillation frequency $f_{\max}$, there has been a single report of a decrease in $f_{\max}$ when the ferroelectric is integrated into the NCFET [23]. For circuit-level figures of merit, investigations have shown that NCFETs can perform better for comparators [20], [26], sample-and-hold circuits [24], analog switches [16], [25], differential amplifiers [16], voltage-to-time converters [26], and current mirrors [16], [20], [25].

Although these advancements show great promise for NCFETs in RF applications, most of the studies thus far have considered a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [10]-[11], [16], [20], [23]. While the MFMIS structure simplifies modeling due to the uniform potential at the ferroelectric-insulator surface, dc leakage currents would make the ferroelectric negative capacitance unstable [27]. This instability makes biasing of MFMIS devices and circuits difficult, and hence makes the MFMIS structure undesirable for RF applications. Furthermore, due to multidomain effects, an additional restriction on the length of the ferroelectric to avoid hysteresis in an MFMIS structure has been reported in the literature, further limiting the usefulness of this structure [28].

By contrast, a metal-ferroelectric-insulator-semiconductor (MFIS) structure mitigates these problems [27], [28], and yields different overall device characteristics arising from a spatially varying ferroelectric potential vs. those in MFMIS structures [15], [22], [29]-[30]. The MFIS structure has also been the choice thus far for integration into advanced nodes [2].

A few studies have also examined the RF performance of MFIS NCFETs [12], [24]-[26]. A small improvement in f_T was reported through experiments in [12], and [24]-[26] reported on circuit-level figures of merit through simulations, with [24] and [26] employing a single-domain ferroelectric model that does

This work was supported in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada, and in part by Alberta Innovation & Advanced Education.

J. K. Wang, T. Cam, Z. C. Yuan, M. Wong, and M. Vaidyanathan are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: maniv@ualberta.ca).

P. S. Gudem is with the Department of Electrical and Computer Engineering, University of California, San Diego, CA 92093 USA.

K. D. Holland is with Qualcomm Inc., San Diego, CA 92121 USA.

D. Kienle is with the Theoretische Physik I, Universität Bayreuth, 95440 Bayreuth, Germany.

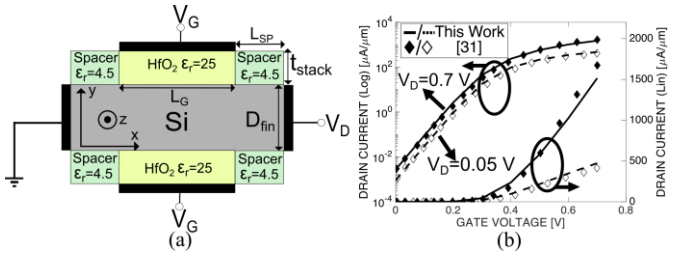

Fig. 1. (a) Schematic diagram of the baseline MOSFET device, where the fin height extends into the z-direction. (b) Calibration of baseline MOSFET device with the experimental results of [31].

TABLE I
DEVICE PARAMETERS

Symbol	Parameter	Value
L_G	Gate Length	20 nm
D_{fin}	Fin Width	7 nm
H_{fin}	Fin Height	46 nm
L_{SP}	Spacer Length	8 nm
t_{stack}	Oxide Stack Thickness	4.3 nm
ϕ_m	Metal Work Function	4.416 eV
$N_{\text{S/D}}$	Source and Drain Doping Concentration	10^{20} cm^{-3}
N_{ch}	Channel Doping Concentration	5 x 10^{17} cm^{-3}
μ_{eff}	Low-Field Effective Mobility	320 cm^2/Vs
β	Velocity Saturation Exponent	2 (electron) / 1 (hole)
v_{sat}	Saturation Velocity	2.1 x 10^7 cm/s

not capture spatial variation of potential in the ferroelectric. These promising results further strengthen the need for a more detailed investigation into the device-level RF performance metrics of MFIS NCFETs.

Motivated by the deficiencies of the MFMIS structure and the promising results of [12], [24], [25], and [26], this study takes the next step in unveiling the full RF potential of NCFETs by considering an MFIS NCFET structure simulated using a physics-based model that includes a spatially varying potential in the ferroelectric, and with the baseline model calibrated to the experimental results in [31], in conjunction with small-signal circuits. The focus will be on three important RF device figures of merit: the conventional metrics f_T and $f_{\max}$, including one important implication of the ferroelectric damping constant ρ on $f_{\max}$, and the metric $g_m f_T/I_D$, an important metric that captures RF performance in the context of required dc power consumption [32]-[34], where I_D is the dc drain current. The results of this work will be useful for the development and optimization of NCFET technology for future RF applications.

This paper is organized into four sections. Section II will summarize the methodologies used for the construction and calibration of our overall modeling approach, including choices of NCFET devices, physical modeling of the MOSFET and NCFET devices, and various intrinsic and extrinsic small-signal models used to obtain the relevant RF figures of merit. Section III will summarize the results with regard to dc performance, small-signal parameters, intrinsic and extrinsic f_T, $f_{\max}$, and $g_m f_T/I_D$. Section IV will summarize the main conclusions.

II. METHODOLOGIES

A. Overview of Approach

The dc model of the baseline MOSFET and NCFETs are numerically simulated using COMSOL Multiphysics [35], which is then used to obtain a quasi-static intrinsic small-signal model for the devices, with the component values found from perturbed dc solutions in the usual way [36, Ch. 8]. For the NCFET, this intrinsic small-signal model includes the impact of small-signal perturbation of the ferroelectric about a stable operating point at the center of its lossless S-shaped curve [1]; this small-signal lossless operation is augmented by a series damping resistor (described in Section II-E2) to account for the loss in the ferroelectric. Extrinsic parasitic elements will then be added to the intrinsic small-signal model to form extrinsic MOSFET and NCFET circuits that will be simulated to assess the RF performance of each type of device.

B. Baseline FET Design and Modeling

The baseline FET in this study is an n-type FinFET with dimensions set to the 10-nm node [31], [37], with a dielectric constant of 25 for HfO_2 [38]. The overall device structure can be seen in Fig. 1(a), with important parameters listed in Table I. Device simulations are conducted in 2-D using COMSOL Multiphysics with the drift-diffusion formalism [22], [29], assuming a geometrical invariance in the fin height direction.

To account for quantum confinement in the fin width direction, the modified local-density approximation [22], [39] has been used. This formalism corrects for both geometrical and energetic confinement effects by assuming an infinite barrier at the silicon-oxide interface and has been shown to have good agreement with Schrödinger-Poisson solvers for FinFET devices [22], [39]. Effective mass values have been taken from [22], with the z-direction assumed to be [1 0 0].

The baseline device has been calibrated to an experimental device in [31] through the adjustment of mobility parameters, as shown in Fig. 1(b). Transport parameters are listed in Table I, and these same parameters are used throughout the paper.

C. Comparison Methodology

Thus far, studies have shown different ways of comparing performance between a baseline MOSFET and an NCFET device. These differences are important to note, as they can lead to different impressions of performance superiority or inferiority for the NCFET technology.

In certain studies, *e.g.*, [11], [16], [20], [23]-[24], the underlying MOSFET is not modified and the ferroelectric layer is directly introduced on top of the stack to produce an NCFET, which changes the total oxide stack thickness t_{stack} of the device. This method results in an NCFET whose dielectric capacitance $C_{\text{ox,DE}}^{\text{NC}}$, which is the capacitance of the stack with the ferroelectric removed, is the same as the oxide capacitance $C_{\text{ox}}^{\text{MOS}}$ of the baseline MOSFET.

In other studies, *e.g.*, [5], [12], [18], [40], the NCFET is constructed by replacing a portion of the MOSFET oxide stack with a ferroelectric, while keeping t_{stack} the same. This results in an NCFET device where $C_{\text{ox,DE}}^{\text{NC}}$ may be different from $C_{\text{ox}}^{\text{MOS}}$.

In this study, t_{stack} is kept the same between the baseline and the NCFET. In practice, due to the limited space between fins in advanced nodes, it may be difficult to deposit a thick layer of ferroelectric on top of the existing FET structure [2]. Therefore, our method helps to assess the RF performance of NCFETs in a technologically relevant way. Hence, in this work, to obtain an NCFET, the HfO_2 of the structure in Fig. 1(a) is replaced by a ferroelectric-dielectric heterostructure having a ferroelectric

thickness of t_{FE} and a dielectric thickness of t_{DE} that sums to a total thickness of t_{stack}. We also note that the exact value of t_{stack}, impacted (for example) by the exact value for the dielectric constant of HfO_2 in the baseline device [38], would not affect the qualitative conclusions of this work.

Since various process-compatible ferroelectric materials [41] and thicknesses exist, and no gate-stack optimization approach has yet been proposed for the RF performance of MFIS NCFETs, a logical method to obtain meaningful initial calibration points that can serve as the basis for future optimization is to consider NCFETs with varying degrees of static performance improvements. The expected static performance improvement can be evaluated through the total oxide capacitance of the NCFET stack $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$, with this total specified by the series combination of the ferroelectric negative capacitance $C_{\mathrm{ox,FE}}^{\mathrm{NC}}$ and the dielectric capacitance $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$. By selecting ferroelectric and dielectric materials, thicknesses, or both, an increase in the total $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$ could be realized, *e.g.*, via an increase in $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$ compared to the baseline, or better capacitance matching such that $C_{\mathrm{ox,FE}}^{\mathrm{NC}}$ and $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$ are closer in magnitude. As $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$ increases, static performance improvement in the NCFET is intuitively expected based on classical velocity-saturated MOSFET theory [36, Ch. 6].

We will consider NCFETs with silicon-doped HfO_2 [2] as the ferroelectric, and SiO_2 [5], [18], [40] as the dielectric, both of which have been shown to be compatible for the fabrication of modern MFIS NCFETs. Three example NCFETs, created by varying t_{DE} to achieve successively increasing $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$, and hence successively improved static performance, will be used to benchmark the RF performance of NCFETs. These are devices B1 – B3 in Table II, where for B1, $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$ is smaller than $C_{\mathrm{ox}}^{\mathrm{MOS}}$; for B2, $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$ is similar to $C_{\mathrm{ox}}^{\mathrm{MOS}}$; and for B3, $C_{\mathrm{ox,tot}}^{\mathrm{NC}}$ is greater than $C_{\mathrm{ox}}^{\mathrm{MOS}}$.

D. NCFET Model and Solution Approach

1) Ferroelectric Electrostatics: The static ferroelectric is modeled using the multidomain Landau-Khalatnikov (LK) equation [13], [21], [42]-[43] for the y-direction polarization, with the time derivative component set to zero:

$$E_y(x,y) = 2\alpha P_y(x,y) + 4\beta P_y^3(x,y) + 6\gamma P_y^5(x,y) - k\nabla^2 P_y(x,y) \quad (1)$$

where $\alpha = -3.60 \times 10^8\ \mathrm{m \cdot F^{-1}}$, $\beta = 2.25 \times 10^{10}\ \mathrm{m^5 \cdot F^{-1} \cdot C^{-2}}$, and $\gamma = 1.67 \times 10^9\ \mathrm{m^9 \cdot F^{-1} \cdot C^{-4}}$ are the LK parameters calibrated to silicon-doped HfO_2 [41], [42], $k = 1 \times 10^{-8}\ \mathrm{m^3 \cdot F^{-1}}$ is the multidomain interaction parameter [19], P_y is the y-direction polarization, and E_y is the y-direction electric field. The x-direction polarization for the ferroelectric is modeled as an ordinary dielectric [21]:

$$E_x(x,y) = [(\epsilon_r - 1)\epsilon_0]^{-1} P_x(x,y) \quad (2)$$

where $\epsilon_r = 25$ is the dielectric constant for the x-direction, equal to that for a dielectric HfO_2 [38], ϵ_0 is the permittivity of free space, P_x is the x-direction polarization, and E_x is the x-direction electric field. In this formulation, variations of polarization and potential in the ferroelectric are allowed in both the x- and y- directions. Using (1) and (2), the ferroelectric electrostatics are self-consistently coupled into the overall FET simulation in the usual way through Poisson's equation.

TABLE II
NCFET DEVICE PARAMETERS

Device	Physical Dielectric Thickness (t_{DE})	Physical Ferroelectric Thickness (t_{FE})	Total Oxide Capacitance per Area
A (Baseline)	4.30 nm ($\epsilon_r = 25$)	0 nm	0.0515 F/m^2
B1 (NCFET)	1.00 nm ($\epsilon_r = 3.9$)	3.30 nm	0.0376 F/m^2
B2 (NCFET)	0.67 nm ($\epsilon_r = 3.9$)	3.63 nm	0.0595 F/m^2
B3 (NCFET)	0.39 nm ($\epsilon_r = 3.9$)	3.91 nm	0.1179 F/m^2

2) Devices: The different combinations of t_{DE} and t_{FE} used to realize B1 – B3 are listed in Table II. Here, we note that the thickness per cycle of deposition of SiO_2 can be around 0.1 nm [44] and silicon-doped HfO_2 can stay ferroelectric down to 3 nm [2]. Hence, the devices chosen here are all representative of possible devices given this material composition. The thicknesses t_{FE} and t_{DE} satisfy the capacitance matching condition for non-hysteretic operation [1]. Moreover, a higher t_{FE} and lower t_{DE} lowers the magnitude of the ferroelectric negative capacitance $C_{\mathrm{ox,FE}}^{\mathrm{NC}} = 1/(2\alpha t_{\mathrm{FE}})$ [1] and increases the magnitude of the dielectric capacitance $C_{\mathrm{ox,DE}}^{\mathrm{NC}} = \epsilon_r\epsilon_0/t_{\mathrm{DE}}$. This results in progressively better capacitance matching in devices B1, B2, and B3, which combined with the progressive increase of $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$, causes these devices to have progressively larger total oxide capacitances, as seen in Table II.

E. Intrinsic Small Signal Models

1) Baseline Intrinsic Model: For the baseline MOSFET, the classical small-signal model is used [36, Ch. 8], as seen in Fig. 2(a). The small-signal quantities in this model are extracted using dc solutions corresponding to small voltage perturbations on the terminals and the following formulas: $C_{\mathrm{gg}} = \Delta Q_G/\Delta V_G$, $C_{\mathrm{gd}} = \Delta Q_G/\Delta V_D$, $C_{\mathrm{gs}} = C_{\mathrm{gg}} - C_{\mathrm{gd}}$, $g_m = \Delta I_D/\Delta V_G$, and $r_o = \Delta V_D/\Delta I_D$, where Q_G is the charge on the gate terminals, I_D is the dc drain current, and the other symbols are identified in Figs. 1(a) and 2(a).

For the NCFET, the same method used for the MOSFET is used to extract intrinsic capacitive components. However, to account for the effects of ferroelectric damping under dynamic operation, a resistor $R_{\rho,\mathrm{eff}}$ has been added in series with the gate, as seen in Fig. 2(b).

2) Damping Resistor for NCFET: The damping resistor for a lumped ferroelectric can be modeled by $R_\rho = \rho t_{\mathrm{FE}}/A_{\mathrm{FE}}$ [42], where A_{FE} is the area of the ferroelectric. For an MFMIS structure, since the transistor can be considered as a separate circuit element from the ferroelectric with a common node between them, the use of $R_{\rho,\mathrm{eff}} \equiv R_\rho$ is an appropriate representation. However, since damping is distributed throughout the ferroelectric, strictly speaking, the lumped value may not be applicable for an MFIS NCFET. To account for the distributed effect, the correct value of an effective damping resistor $R_{\rho,\mathrm{eff}} \neq R_\rho$ should be investigated for the MFIS small-signal model.

To make a first-order estimate for the value of $R_{\rho,\mathrm{eff}}$, an equivalent circuit approach is used. As seen in Fig. 3(a), when a small perturbative voltage is applied at the gate of the MFIS NCFET, a charge response $\Delta Q(x,y)$ occurs throughout the intrinsic structure, leading to a non-uniform distribution of the total input capacitance, $C_{\mathrm{gg}}(x,y) = H_{\mathrm{fin}} \times \Delta Q(x,y)/\Delta V_G$. This input capacitance includes capacitive effects from both the

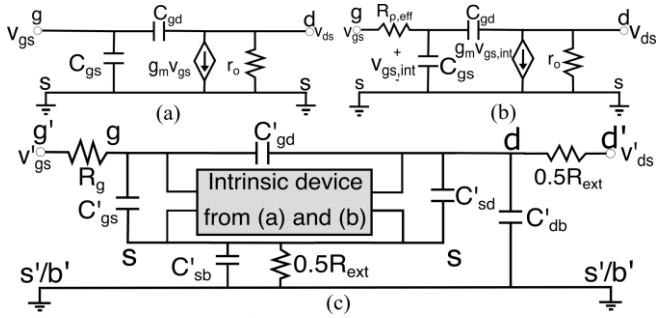

Fig. 2. Small-signal circuits for: (a) intrinsic MOSFET; (b) intrinsic NCFET; (c) extrinsic circuit for both MOSFET and NCFET, where the damping resistor $R_{\rho,\text{eff}}$ is inside the intrinsic box.

ferroelectric layer, the dielectric layer, and fringing fields through the ferroelectric and spacers.

From the distributed capacitance $C_{\text{gg}}(x,y)$, a few further assumptions can be made to obtain the first-order input circuit model seen in Fig. 3(b). First, the relatively small vacuum capacitance of the ferroelectric can be ignored, which allows each damping resistor R_n to be directly attached to each input capacitance C_n. Second, variation of the charge in the y-direction is neglected, which allows us to collapse $C_{\text{gg}}(x,y)$ into $C_{\text{gg}}(x) = \int C_{\text{gg}}(x,y)\,dy$. Finally, ferroelectric damping is assumed to be uniformly distributed in the x-direction, and hence among all capacitors, making $R_n = \rho t_{\text{FE}}/2H_{\text{fin}}dx$.

By evaluating the input resistance as the real part of the input impedance of Fig. 3(b), we have found that the value of $R_{\rho,\text{eff}}$ is constant in the frequency range used to extract f_T and f_{max}. The exact value depends on the device and bias point, and is between 22 and 32% *above* R_ρ for every bias point in all devices. Further, we have also confirmed that a lack of distribution in capacitance leads to $R_{\rho,\text{eff}} = R_\rho$, as expected.

While further refinements to the model can be made to capture effects such as horizontal field lines, as seen near the vertical edges of the ferroelectric region in Fig. 3(a), or the possibility of fringing fields that completely bypass the ferroelectric, these are neglected as second-order effects.

Therefore, to first order, we will use the equivalent circuit model presented in Fig. 3(b) and the corresponding device-dependent, bias-dependent $R_{\rho,\text{eff}} \sim 1.22$ to $1.32 \times R_\rho$ derived from the input resistance to benchmark the RF performance of NCFETs. However, to further preserve generality and account for any remaining uncertainty in the exact value to use for $R_{\rho,\text{eff}}$, we note that a change in $R_{\rho,\text{eff}}$ is analogous to a change in the damping constant ρ, and we have hence modulated ρ in this study. For initial benchmarks, a relatively low ρ of 1.80 m$\Omega \cdot$ m that does not affect digital operation has been chosen [45].

F. Modeling of Extrinsic Components

To account for parasitic resistances and capacitances not captured in the intrinsic model, an extrinsic circuit model is constructed using the classical method [36, Ch. 8], with the extrinsic source and body terminal shorted, as seen in Fig. 2(c). Here, we assume that the integration of the ferroelectric does not change extrinsic parasitic elements, which are bias-independent and depend only on the geometry of the extrinsic structure.

To obtain appropriate values for the elements, a 3-D single-fin extrinsic structure up to the access vias for each terminal has been used, similar in geometry to the test structure used in [12].

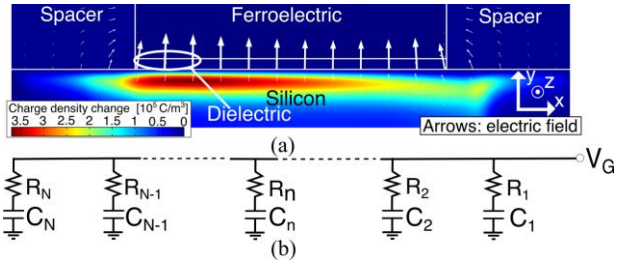

Fig. 3. (a) Change of charge as a function of position for device B2 (as specified in Table II) at $V_G = V_D = 0.7$ V and with $\Delta V_G = 0.02$ V, where the white arrows represent the electric field associated with these charges. Only the top half of the device is shown since the bottom half has symmetrical characteristics. The field lines in the ferroelectric region are too small to be visible. (b) Equivalent circuit used to evaluate $R_{\rho,\text{eff}}$.

This structure can be seen in Fig. 4, with critical dimensions given in Table III and Table I. For reference, the diagram in Fig. 1(a) is a 2-D representation of the intrinsic device region with translational invariance in the z-direction, contained within the dash-boxed region in Fig. 4(b). This intrinsic region has been hollowed for the extraction of extrinsic parasitic capacitances to avoid double counting of intrinsic capacitances.

Extrinsic contact-to-contact capacitances C'_{gd}, C'_{gs}, and C'_{sd} are obtained by applying small voltage perturbations at the terminals and examining changes of terminal charge. The source- and drain-to-wafer junction capacitances C'_{sb} and C'_{db} are obtained using classical formulas for depletion capacitance of p-n junctions [46]. Values for all these capacitances can be found in Table III.

Extrinsic resistances are obtained through the physical geometry in Fig. 4(a). For source and drain resistances, the resistance value is calculated by separating the resistance into three portions – via resistance, contact resistance, and epitaxial silicon resistance. The via is assumed to be tungsten, and the values of resistivity for the via and the contact used are $3 \times 10^{-5}\ \Omega \cdot \text{cm}$ [47] and $1 \times 10^{-9}\ \Omega \cdot \text{cm}^2$ [48], respectively. The epitaxial silicon resistance on each side is 10% of the total channel resistance, a reasonable choice considering the proportions shown in [48]. For the value of gate resistance R_g, the metal layer is also assumed to be made of tungsten [49], with a thickness-dependent resistivity from [47], and the distributed effects from a single gate contact have been taken into account in the calculation [36, Ch. 9]. Values for the extrinsic resistances used can also be found in Table III.

While the neglect of further layers of high-density interconnects beyond the terminal contacts and their associated parasitic capacitances in the extrinsic structure may cause an overestimation of f_T and f_{max} values, general trends concluded in this paper will not be affected by this approximation.

III. Results

A. Static Results

As shown from Fig. 5(a), all NCFET devices B1 – B3 have a lower off-current I_{off} and subthreshold slope (SS) compared to the baseline. In terms of on-current I_{on}, devices B1 – B3 respectively exhibit lower, similar, and higher I_{on} compared to the baseline. We also note that the non-hysteretic operation of the NCFET devices have been confirmed by dual-direction dc sweeps of V_G. These results are expected and in line with literature, but will be briefly discussed for completeness.

The lower I_{off} in NCFETs is consistent with results in the

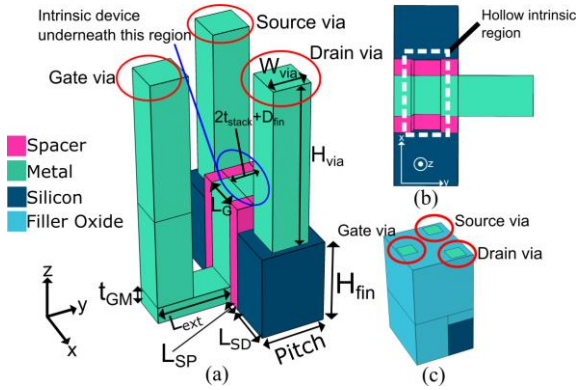

Fig. 4. (a) Extrinsic structure 3-D diagram. (b) Bottom view of extrinsic structure, the hollow intrinsic region is the dashed box. (c) The extrinsic structure after oxide fill.

TABLE III
EXTRINSIC STRUCTURE PARAMETERS

Parameter	Value	Parameter	Value
Pitch	34.0 nm	C'_{gd}	7.70 aF
H_{via}	88.0 nm	C'_{gs}	7.70 aF
W_{via}	19.5 nm	C'_{sd}	1.32 aF
L_{SD}	26.0 nm	C'_{sb}	1.87 aF
L_{ext}	40.0 nm	C'_{db}	1.45 aF (V_D = 0.7 V)
t_{GM}	9.2 nm	R_{ext}	880.86 Ω
		R_g	836.43 Ω

literature [19], [21], [29]. In addition to the enhancement of the total oxide capacitance that already suppresses I_{off}, drain coupling in NCFETs at low gate voltage leads to a suppression of channel potential and a raise in barrier energy that gets stronger as capacitance matching becomes better, which further suppresses the I_{off} [19], [21], [29]. Due to this additional effect, device B1 exhibits a lower I_{off} compared to the baseline despite having a lower total oxide capacitance compared to the baseline. In addition, since devices B1 – B3 have progressively better capacitance matching, this trend of progressively lower I_{off} is expected and also agrees with literature [19].

The results for I_{on} compared to the baseline can be intuitively interpreted through classical velocity-saturated MOSFET theory, where current in the inversion regime is proportional to the total oxide capacitance of the device [36, Ch. 6]. Since devices B1, B2, and B3 respectively have lower, similar, and higher total oxide capacitance, as listed in Table II, the same trend is exhibited in the I_{on} of these devices.

B. Results for the Small-Signal Parameters

Small-signal parameters for the devices are obtained using the method prescribed in Section II-E. The small-signal results for g_m, C_{gg}, and r_o can be seen in Fig. 5(b) – (d), for V_D = 0.7 V [10]. These results are in line with observations made in the previous literature [2] – [22] mentioned in Section I.

As seen from Fig. 5(b) and Fig. 5(c), compared to the baseline, the transconductance g_m and the input capacitance C_{gg}, the latter a combination of the ferroelectric capacitance, dielectric capacitance, and any fringing capacitances through the spacers, are lower for device B1, and higher for devices B2 and B3. Since both quantities are also directly proportional to the total oxide capacitance of the devices as described by classical velocity-saturated MOSFET theory [36, Ch. 8], this result can be understood by the same approach used to explain the I_{on} trends in Section III-A.

As seen from Fig. 5(d), devices B1 – B3 exhibit progressively higher r_o compared to that of the baseline. This phenomenon can be intuitively understood through the concept of drain coupling, as explained in detail in [14], where the increase in r_o is directly proportional to a coupling factor ζ_D that increases as matching improves. Since devices B1 – B3 have progressively better matching, this result is expected.

C. Cut-off Frequency f_T and $g_m f_T/I_D$

The cut-off frequency of the devices are obtained by simulating the circuits in Fig. 2. For each bias point, the cut-off frequency is extracted by extrapolating the magnitude of the short-circuit, common-source current gain to unity in the -20 dB/decade roll-off region, between 100 kHz and 3.3 GHz.

As seen in Fig. 6(a), the intrinsic (excluding parasitic components) cut-off frequency $f_{T,i}$ of the NCFETs are very similar to that of the MOSFETs at all bias points, with a maximum difference of 13% between the two classes of devices. To understand this result, the following approximate formula for $f_{T,i}$ can be utilized [36, Ch. 8]:

$$f_{T,i} \approx g_m/2\pi C_{gg} \tag{3}$$

As seen from (3), $f_{T,i}$ is directly proportional to g_m and inversely proportional to C_{gg}, meaning that a simultaneous change in g_m and C_{gg} in similar proportions would result in no change in $f_{T,i}$. As observed in Figs. 5(b) and (c) and discussed in Section III-B, the g_m and C_{gg} of an NCFET are both proportional to the total oxide capacitance per area. Therefore, the changes in these two parameters compensate each other in their impact on $f_{T,i}$, leading to the observed performance parity between NCFETs and the baseline MOSFET.

For the extrinsic cut-off frequency $f_{T,e}$, a degradation for both the baseline and the NCFET can be observed due to the addition of additional parasitic elements, as expected. Despite this drop, similar performance between the NCFET and the baseline continues to be observed, as seen from Fig. 6(a).

We have also confirmed through simulations that the addition of $R_{\rho,eff}$ does not impact $f_{T,e}$. This is consistent with the formula developed in [50], where $f_{T,e}$ is unaffected by resistances on the gate terminal, and can be approximated by

$$f_{T,e} \approx \frac{1}{2\pi}\frac{g_m}{C_{gg}+C'_{gg}+\left[\frac{1}{r_o}(C_{gg}+C'_{gg})+g_m\left(C_{gd}+C'_{gd}\right)\right](R_{ext})} \tag{4}$$

where $C'_{gg} = C'_{gd} + C'_{gs}$ is the total extrinsic input capacitance and the other components are those shown in Fig. 2(c).

For low-power RF applications, especially receiver LNAs [34], another important figure of merit to consider is $g_m f_T/I_D$, which captures dc power consumption in addition to RF performance [32]-[34] and is calculated here using $g_m \times f_{T,e}/I_D$. As seen in Fig. 6(b), for a given I_D, $g_m f_T/I_D$ follows the same trend as I_{on}, with device B3 achieving up to 51% higher values compared to the baseline. These trends can also be explained by the total oxide capacitance values listed in Table II, as done for I_{on} in Section III-A. Therefore, while NCFETs are expected to have similar f_T as the baseline, NCFETs with a high total oxide capacitance, *e.g.*, achieved through good capacitance matching, can achieve higher $g_m f_T/I_D$.

These results of similar f_T performance but higher $g_m f_T/I_D$ show consistency with previous literature for MFMIS devices

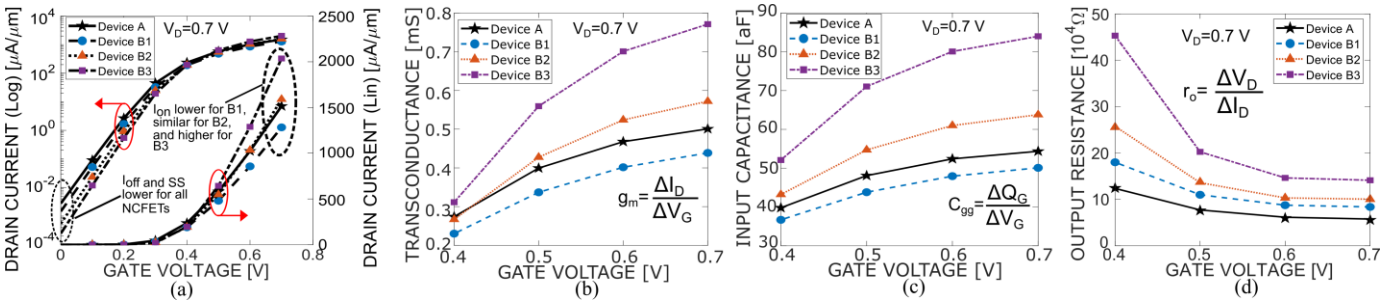

Fig. 5. Static and small-signal characteristics at various V_G with $V_D = 0.7$ V: (a) dc characteristics; (b) transconductance; (c) input capacitance; (d) output resistance.

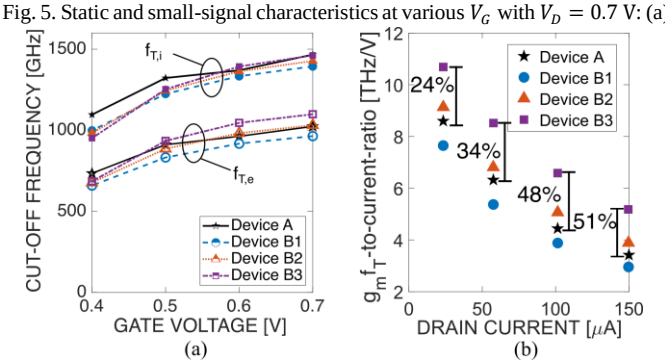

Fig. 6. (a) Cut-off frequency plotted against dc gate voltage at $V_D = 0.7$ V. (b) $g_m \times f_{T,e}/I_D$ plotted against dc drain current, with $V_D = 0.7$ V for all devices and the same I_D between devices achieved by adjusting V_G.

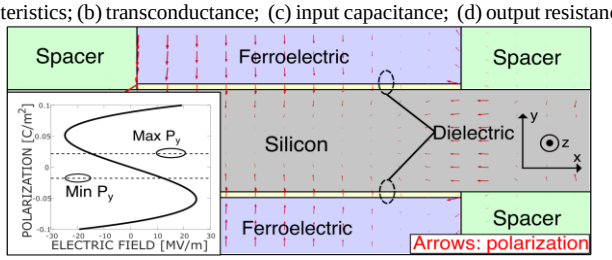

Fig. 7. Polarization as a function of position for device B3 at $V_G = V_D = 0.7$ V. Inset: Minimum and maximum ferroelectric polarization P_y across all bias points and all devices with the ferroelectric S-curve for a single lossless dipole, defined by (1) with $k = 0$.

[10], [16], despite the ferroelectric having a spatially dependent potential along the channel in an MFIS structure. The reason for this similarity can be explained by the capacitance of the ferroelectric at each of the bias points. While the potential variations along the length of the channel do cause the ferroelectric to have a spatially dependent polarization in an MFIS structure, as shown in Fig. 7, if we examine the limits of these polarizations, it can be seen in the inset that under all bias conditions and across all NCFET devices, the ferroelectric stays within the negative capacitance region. Therefore, from a capacitance viewpoint, the ferroelectric can be intuitively considered as a linear negative capacitor in series with a conventional MOSFET, which coincides with the MFMIS view of the structure.

Overall, our results thus show that while MFIS NCFETs would have a similar f_T performance, those with a higher total oxide capacitance can achieve a higher $g_m f_T/I_D$ than their baseline MOSFET counterparts.

D. *Maximum Oscillation Frequency*

The maximum oscillation frequency $f_{\max}$ of the devices are also extracted through simulation of Fig. 2(c) and extrapolation of Mason's unilateral gain [51] to unity from its -20 dB/decade roll-off region, between 100 kHz and 3.3 GHz.

The $f_{\max}$ of each device plotted against dc current can be seen in Fig. 8(a). It is evident from this plot that NCFET devices all have lower $f_{\max}$ compared to the baseline, with a larger decrease as t_{FE} increases. This is a direct consequence of the ferroelectric damping constant ρ and $R_{\rho,\text{eff}}$.

To understand this phenomenon, the following approximate formula for the $f_{\max}$ of a MOSFET can be used [50]

$$f_{\max} \approx \frac{f_{T,e}}{\sqrt{\frac{4}{r_o}R_g + 8\pi f_{T,e}\left(C_{gd}+C'_{gd}\right)\left[R_g+\eta_D R_d\right]}} \quad (5)$$

where $R_d = 0.5R_{ext}$ is the resistance on the drain side of the small-signal model in Fig. 2(c), and $\eta_D = (C_{gd} + C'_{gd} + C'_{sd})/(C_{gg} + C'_{gg})$ is the ratio of capacitances looking into the drain to those looking into the gate.

From (5), we can see that if gate resistance increases, $f_{\max}$ degrades. While the insertion of $R_{\rho,\text{eff}}$ degrades the accuracy of directly applying (5) to NCFETs, we have found that a simple replacement of R_g with $R_g + R_{\rho,\text{eff}} \times \left[C_{gg}/(C_{gg} + C'_{gg})\right]^2$ is sufficient for intuitive understanding and making first-order predictions, yielding results that are within 15% of the markers in Fig. 8(a) for devices B1, B2, and B3. With the replacement, we find the resulting increase in gate resistance due to ρ is the central cause of the observed decrease in $f_{\max}$ for NCFETs.

E. *Effect of Damping Constant on f_{max}*

While $R_{\rho,\text{eff}}$ is observed to decrease $f_{\max}$, the effects of the damping parameter is still an actively studied field for NCFETs, with methods still being developed to accurately extract the damping constant ρ [42], [45]. In the future, lower ρ may be discovered or engineered. To comprehensively evaluate the effects of ferroelectric damping, we have modulated ρ and evaluated the $f_{\max}$ performance of NCFETs in comparison to the baseline and the results have been plotted in Fig. 8(b).

To establish a meaningful comparison between NCFET and MOSFET devices for practical RF applications in which I_D is used to bias the device at its dc operating point, the gate voltages of the NCFET devices have been adjusted such that all devices carry the same dc bias current I_D. While an I_D corresponding to the baseline MOSFET biased at $V_G = 0.4$ V has been selected as an example, we have found that the choice of I_D does not change the general trend.

As seen from Fig. 8(b), as ferroelectric damping becomes lower, the $f_{\max}$ performance improves as expected. At high ρ, the resistor $R_{\rho,\text{eff}}$ dominates $f_{\max}$ performance for NCFETs, and therefore, for any given ρ, NCFETs with a smaller t_{FE} tend to perform better compared to those with a higher t_{FE}.

As ρ decreases, the $f_{\max}$ for devices with thicker ferroelectric layers start to converge to those with a thinner ferroelectric, as seen in Fig. 8(b), where the curves for devices B1 – B3 (ordered from lowest to highest t_{FE}) show vanishing

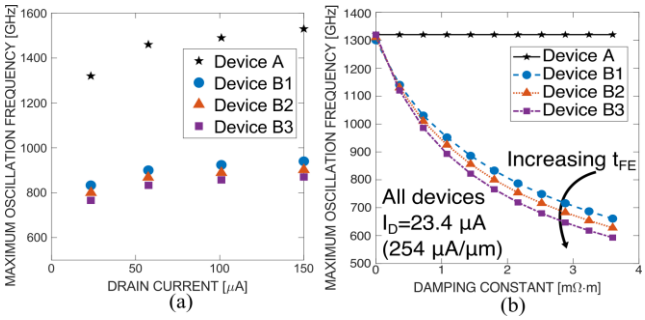

Fig. 8. (a) $f_{\max}$ plotted vs. dc drain current for each device. (b) $f_{\max}$ for different values of ρ for each device for a given current.

differences as ρ decreases. This convergence occurs because while a higher t_{FE} leads to a higher $R_{\rho,\mathrm{eff}}$, it simultaneously leads to better capacitance matching for a given ferroelectric-dielectric combination, which leads to a higher r_o. As ρ becomes smaller and hence $R_{\rho,\mathrm{eff}}$ becomes smaller, this difference in r_o has greater impact, and ultimately leads to the convergence of the curves.

If the ferroelectric has extremely low damping, corresponding to ρ approaching zero, one may expect from (5) that the NCFET can achieve a superior $f_{\max}$ performance compared to the baseline MOSFET due to an increase in r_o. However, this expected improvement is not observed, primarily because the product of total gate resistance and gate-drain capacitance, appearing algebraically as the second term in the denominator of (5), and well-known to dominate the $f_{\max}$ of FETs, remains sufficiently large to limit $f_{\max}$ despite the improvements to r_o.

Overall, it can be concluded through these results that the suppression of the damping constant ρ is important for the optimization of NCFETs for RF applications. With adequate suppression, similar $f_{\max}$ performance between NCFETs and the baseline MOSFET can be expected.

IV. Conclusions

The following conclusions can be drawn from this paper that investigates the RF performance of NCFETs with an MFIS stack structure, using a simulation methodology calibrated to the experimental results of [31]:

1) The intrinsic and extrinsic f_T of MFIS NCFET can be expected to be similar compared to the baseline MOSFET in a given technology, as shown in Fig. 6(a).
2) In comparison to a baseline MOSFET, the $f_{\max}$ of MFIS NCFETs can be additionally impacted by the ferroelectric damping term ρ, which effectively increases the gate resistance of an NCFET; however, if damping is adequately suppressed, NCFETs can achieve similar performance compared to the baseline MOSFET, as seen in Fig. 8(b).
3) MFIS NCFETs with a high total oxide capacitance, *e.g.*, achieved via good capacitance matching, are expected to have a substantially higher $g_m f_T/I_D$ [32]-[34] compared to the baseline MOSFET – by up to 51% for our devices, as shown in Fig. 6(b).

Overall, for NCFETs with high total oxide capacitance and low ρ, similar f_T and $f_{\max}$ performance but higher $g_m f_T/I_D$ is to be expected. With a performance parity in f_T and $f_{\max}$, and an improvement in $g_m f_T/I_D$, which is an important metric for RF performance [32]-[34], this work thus finds promise for next-generation, low-power RF applications with NCFETs.

References

[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405-410, Dec. 2007, doi: 10.1021/nl071804g.

[2] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J. Liu, J. Shi, H. J. Kim, R. Sporer, C. Serrao, A. Busquet, P. Polakowski, J. Muller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEDM Tech. Dig.*, Dec. 2017, pp. 15.1.1-15.1.4, doi: 10.1109/IEDM.2017.8268393.

[3] Y.- K. Lin, H. Agarwal, M.- Y. Kao, J. Zhou, Y.- H. Liao, A. Dasgupta, P. Kushwaha, S. Salahuddin, and C. Hu, "Spacer engineering in negative capacitance FinFETs," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 1009-1012, Jun. 2019, doi: 10.1109/LED.2019.2911104.

[4] A. I. Khan, U. Radhakrishna, S. Salahuddin, and D. Antoniadis, "Work function engineering for performance improvement in leaky negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1335-1338, Sep. 2017, doi: 10.1109/LED.2017.2733382.

[5] Z. Zhang, G. Xu, Q. Zhang, Z. Hou, J. Li, Z. Kong, Y. Zhang, J. Xiang, Q. Xu, Z. Wu, H. Zhu, H. Yin, W. Wang, and T. Ye, "FinFET with improved subthreshold swing and drain current using 3-nm ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 367-370, Mar. 2019, doi: 10.1109/LED.2019.2891364.

[6] J. Zhou, G. Han, J. Li, Y. Liu, Y. Peng, J. Zhang, Q.- Q. Sun, D. W. Zhang, and Y. Hao, "Negative differential resistance in negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 622-625, Apr. 2018, doi: 10.1109/LED.2018.2810071.

[7] D. Kwon, K. Chatterjee, A. J. Tan, A. K. Yadav, H. Zhou, A. B. Sachid, R. dos Reis, C. Hu, and S. Salahuddin, "Improved subthreshold swing and short channel effect in FDSOI n-channel negative capacitance field effect transistors," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 300-303, Feb. 2018, doi: 10.1109/LED.2017.2787063.

[8] J. Li, J. Zhou, G. Han, Y. Liu, Y. Peng, J. Zhang, Q.- Q. Sun, D. W. Zhang, and Y. Hao, "Correlation of gate capacitance with drive current and transconductance in negative capacitance Ge PFETs," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1500-1503, Oct. 2017, doi: 10.1109/LED.2017.2746088.

[9] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S. K. Gupta, "Device-circuit analysis of ferroelectric FETs for low-power logic," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3092-3100, Aug. 2017, doi: 10.1109/TED.2017.2717929.

[10] S. Mehrotra and S. Qureshi, "Analog/RF performance of thin (~10 nm) HfO_2 ferroelectric FDSOI NCFET at 20 nm gate length," in *Proc. 2018 IEEE SOI-3D-Subthreshold Microelectronics Technol. Unified Conf.*, Oct. 2018, pp. 1-3, doi: 10.1109/S3S.2018.8640153.

[11] H. Mehta and H. Kaur, "Study on impact of parasitic capacitance on performance of graded channel negative capacitance SOI FET at high temperature," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2904-2909, Jul. 2019, doi: 10.1109/TED.2019.2917775.

[12] K.- S. Li, Y.- J. Wei, Y.- J. Chen, W.- C. Chiu, H.- C. Chen, M.- H. Lee, Y.- F. Chiu, F.- K. Hsueh, B.- W. Wu, P.- G. Chen, T.- Y. Lai, C.- C. Chen, J.- M. Shieh, W.- K. Yeh, S. Salahuddin, and C. Hu, "Negative-capacitance FinFET inverter, ring oscillator, SRAM cell, and ft," in *IEDM Tech. Dig.*, Dec. 2018, pp. 31.7.1-31.7.4, doi: 10.1109/IEDM.2018.8614521.

[13] T. Rollo, H. Wang, G. Han, and D. Esseni, "A simulation based study of NC-FETs design: off-state versus on-state perspective," in *IEDM Tech. Dig.*, Dec. 2018, pp. 9.5.1-9.5.4, doi: 10.1109/IEDM.2018.8614514.

[14] H. Agarwal, P. Kushwaha, J. P. Duarte, Y.- K. Lin, A. B. Sachid, M.- Y. Kao, H.- L. Chang, S. Salahuddin, and C. Hu, "Engineering negative differential resistance in NCFETs for analog applications," *IEEE Trans. Electron Devices*, vol. 65, no. 5, pp. 2033-2039, May 2018, doi: 10.1109/TED.2018.2817238.

[15] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structure," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 867-873, Mar. 2018, doi: 10.1109/TED.2018.2794499.

[16] Y. Li, Y. Kang, and X. Gong, "Evaluation of negative capacitance ferroelectric MOSFET for analog circuit applications," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4317-4321, Oct. 2017, doi: 10.1109/TED.2017.2734279.

[17] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y.- K. Lin, H.- L. Chang, S. Salahuddin, and C. Hu, "Compact models of negative-capacitance FinFETs: lumped and distributed charge models," in *IEDM Tech. Dig.*, Dec. 2016, pp. 30.5.1-30.5.4, doi: 10.1109/IEDM.2016.7838514.

[18] D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y.- H. Liao, A. J. Tan, C. Hu, and S. Salahuddin, "Negative capacitance FET with 1.8-nm-thick Zr-doped HfO2 oxide," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 993-996, Jun. 2019, doi: 10.1109/LED.2019.2912413.

[19] Y.- K. Lin, H. Agarwal, P. Kushwaha, M.- Y. Kao, Y.- H. Liao, K. Chatterjee, S. Salahuddin, and C. Hu, "Analysis and modeling of inner fringing field effect on negative capacitance FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2023-2027, Apr. 2019, doi: 10.1109/TED.2019.2899810.

[20] Y. Liang, X. Li, S. K. Gupta, S. Datta, and V. Narayanan, "Analysis of DIBL effect and negative resistance performance for NCFET based on a compact SPICE model," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5525-5529, Dec. 2018, doi: 10.1109/TED.2018.2875661.

[21] A. K. Saha, P. Sharma, I. Dabo, S. Datta, and S. K. Gupta, "Ferroelectric transistor model based on self-consistent solution of 2D poisson's, non-equilibrium green's function and multi-domain Landau Khalatinikov equations," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.5.1-13.5.4, doi: 10.1109/IEDM.2017.8268385.

[22] G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: above-threshold behavior," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1591-1598, Mar. 2019, doi: 10.1109/TED.2019.2892186.

[23] R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook and A. Dixit, "Evaluation of 10-nm bulk FinFET RF performance - conventional versus NC-FinFET," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1246-1249, Aug. 2018, doi: 10.1109/LED.2018.2846026.

[24] Y. Liang, X. Li, S. George, S. Srinvasa, Z. Zhu, S. K. Gupta, S. Datta, and V. Narayanan, "Influence of body effect on sample-and-hold circuit design using negative capacitance FET," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3909-3914, doi: 10.1109/TED.2018.2852679.

[25] Y.-C. Lu and V. P.-H. Hu, "Evaluation of analog circuit performance of ferroelectric SOI MOSFETs considering interface trap charges and gate length variations," in *Proc. Silicon Nanoelectronics Workshop*, Jun. 2019, pp. 1-3, doi: 10.23919/SNW.2019.8782942.

[26] Y. Liang, Z. Zhu, X. Li, S. K. Gupta, S. Datta, and V. Narayanan, "Utilization of negative-capacitance FETs to boost analog circuit performances," *IEEE Trans. Very Large Scale Integra. (VLSI) Syst*., vol. 27, no. 12, pp. 2855-2860, Dec. 2019, doi: 10.1109/TVLSI.2019.2932268.

[27] A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, "Negative capacitance behavior in a leaky ferroelectric," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4416-4422, Nov. 2016, doi: 10.1109/TED.2016.2612656.

[28] M. Hoffmann, M. Pesic, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10891-10899, May 2018, doi: 10.1039/C8NR02752H.

[29] G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical investigation of short-channel effects in negative capacitance MFIS and MFMIS transistors: subthreshold behavior," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5130-5136, Nov. 2018, doi: 10.1109/TED.2018.2870519.

[30] X. Zhang, X. Gong, and G. Liang, "Analysis on performance of ferroelectric NC-FETs based on real-space gibbs-free energy with atomic channel structure," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 1100-1106, Feb. 2019, doi: 10.1109/TED.2018.2888930.

[31] C. Auth, A. Aliyarukuju, A. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buechler, V. Chikarmane, G. Ding, Q. Fu, H. Gomez, W. Han, D. Hanken, M. Haranm N. Hattendorf, R. Heussner, H. Hiramatsu, B. Ho, S. Jalobiar, I. Jin, S. Joshi, S. Kirby, S. Kosaraju, H. Kothari, G. Leatherman, K. Lee, J. Leib, A. Madhavan, K. Marla, H. Meyer, T. Mule, C. Parker, S. Parthasarathy, C. Pelto, L. Pipes, M. Sprinkle, A. St. Armor, C. Stauss, R. Suri, D. Towner, A. Tripathi, A. Tura, C. Ward, and A. Yeoh, "A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig*., Dec. 2017, pp. 29.1.1-29.1.4, doi: 10.1109/IEDM.2017.8268472.

[32] W. Sansen, "Analog design procedures for channel lengths down to 20 nm," in *Proc. IEEE 20th Int. Conf. Electron., Circuits, Syst. (ICECS)*, Dec. 2013, pp. 337-340, doi: 10.1109/ICECS.2013.6815423.

[33] A. Shameli and P.Heydari, "Ultra-low power RFIC design using moderately inverted MOSFETs: an analytical/experimental study," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Jun. 2016, pp. 1-4, doi: 10.1109/RFIC.2006.1651193.

[34] W. Sansen, "Analog CMOS from 5 micrometer to 5 nanometer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Feb. 2015, pp. 22-27, doi: 10.1109/ISSCC.2015.7062848.

[35] COMSOL Inc., Los Angeles, CA, USA. *COMSOL Multiphysics v5.4.* (2018) [Online]. Available: www.comsol.com, Accessed on: Sep. 26, 2019.

[36] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York, NY, USA: WCB McGraw-Hill, 1999.

[37] International Roadmap for Devices and Systems, "More Moore," 2017. [Online]. Available: https://irds.ieee.org/images/files/pdf/2017/2017IRDS_MM.pdf.

[38] J. Robertson, "High dielectric constant oxides," *Eur. Physical J. Appl. Phys.*, vol. 28, no. 3, pp. 265-291, Dec. 2004, doi: 10.1051/epjap:2004206.

[39] O. Penzin, G. Paasch, and L. Smith, "Nonparabolic multivalley quantum correction model for InGaAs double-gate structures," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2246-2250, Jul. 2013, doi: 10.1109/TED.2013.2264165.

[40] M.- J. Tsai, P.- J. Chen, C.- C. Hsu, D.- B. Ruan, F.- J. Hou, P.- Y. Peng, and Y.- C. Wu, "Atomic-level analysis of sub-5-nm-thick Hf0.5Zr0.5O2 and characterization of nearly hysteresis-free ferroelectric FinFET," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1233-1236, Aug. 2019, doi: 10.1109/LED.2019.2922239.

[41] J. Muller, P. Polakowski, S. Mueller, and T. Mikolajick, "Ferroelectric hafnium oxide based materials and devices: assessment of current status and future prospects," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 5, pp. N30-N35, Feb. 2015, doi: 10.1149/2.0081505jss.

[42] Z. C. Yuan, P. S. Gudem, M. Wong, J. K. Wang, T. B. Hook, P. Solomon, D. Kienle, and M. Vaidyanathan, "Toward microwave s- and x-parameter approaches for the characterization of ferroelectric for applications in FeFETs and NCFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2028-2035, Apr. 2019, doi: 10.1109/TED.2019.2901668.

[43] P. Lenarcyzk and M. Luisier, "Physical modeling of ferroelectric field-effect transistors in the negative capacitance regime," in *Proc. Int. Conf. Simul. Semicond. Processes Devices*, Sep. 2016, pp. 311-314, doi: 10.1109/SISPAD.2016.7605209.

[44] L. F. Pena, C. E. Nanayakkara, A. Mallikarjunan, H. Chandra, M. Xiao, X. Lei, R. M. Pearlstein, A. Derecskei-Kovacs, and Y. J. Chabal, "Atomic layer deposition of silicon dioxide using aminosilanes di-sec-butylaminosilane and bis(tert-butylamino) silane with ozone," *J. Physical Chemistry C*, vol. 120, no. 20, pp. 10721-11312, May 2016, doi: 10.1021/acs.jpcc.6b01803.

[45] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1328-1330, Sep. 2017, doi: 10.1109/LED.2017.2731343.

[46] A. S. Sedra and K. C. Smith, "Diodes," in *Microelectronic Circuits*, 5th ed. New York: Oxford University Press, 2004, ch. 3, sec. 3.73, pp. 200-202.

[47] P. Petroff, T. T. Sheng, A. K. Sinha, G. A. Rozgonyi, and F. B. Alexander, "Microstructure, growth, resistivity, and stress in thin tungsten films deposited by rf sputtering," *J. Appl. Physics*, vol. 44, no. 6, pp. 2545-2554, Oct. 2003, doi: 10.1063/1.1662611.

[48] H. Wu, O. Gluschenkov, G. Tsutsui, C. Niu, K. Brew, C. Durfee, C. Prindle, V. Kamineni, S. Michizuki, C. Lavoie, E. Nowak, Z. Kiu, J. Yang, S. Choi, J. Demarrest, L. Yu, A. Carr, W. Wang, J. Strane, S. Tsai, Y. Liang, H. Amnapu, I. Saraf, K. Ryan, F. Lie, W. Kleemeier, K. Choi, N. Cave, T. Yamashita, A. Knorr, D. Gupta, B. Haran, D. Guo, H. Bu, and M. Khare, "Parasitic resistance reduction strategies for advanced CMOS FinFETs beyond 7nm," in *IEDM Tech. Dig.*, Dec. 2018, pp. 35.4.1-35.4.4, doi: 10.1109/IEDM.2018.8614661.

[49] T. Ando, B. Kannan, U. Kwon, W. L. Lai, B. P. linder, E. A. Cartier, R. Haight, M. Copel, J. Bruley, S. A. krishnan, and V. Narayanan, "Simple gate metal anneal (SIGMA) stack for FinFET replacement metal gate toward 14nm and beyond," in *Proc. VLSI Symp.*, Jun. 2014, doi: 10.1109/VLSIT.2014.6894358.

[50] T. C. Lim and G. A. Armstrong, "The impact of the intrinsic and extrinsic resistances of double gate SOI on RF performance," *Solid-State Electron.*, vol. 50, no. 5, pp. 774-783, May 2006, doi: 10.1016/j.sse.2006.04.010.

[51] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Trans. Microwave Theory Techn.*, vol. 40, no. 5, pp. 864-879, May 1992, doi: 10.1109/22.137392.