Name: Adan Shahid EE-272L Digital Systems Design

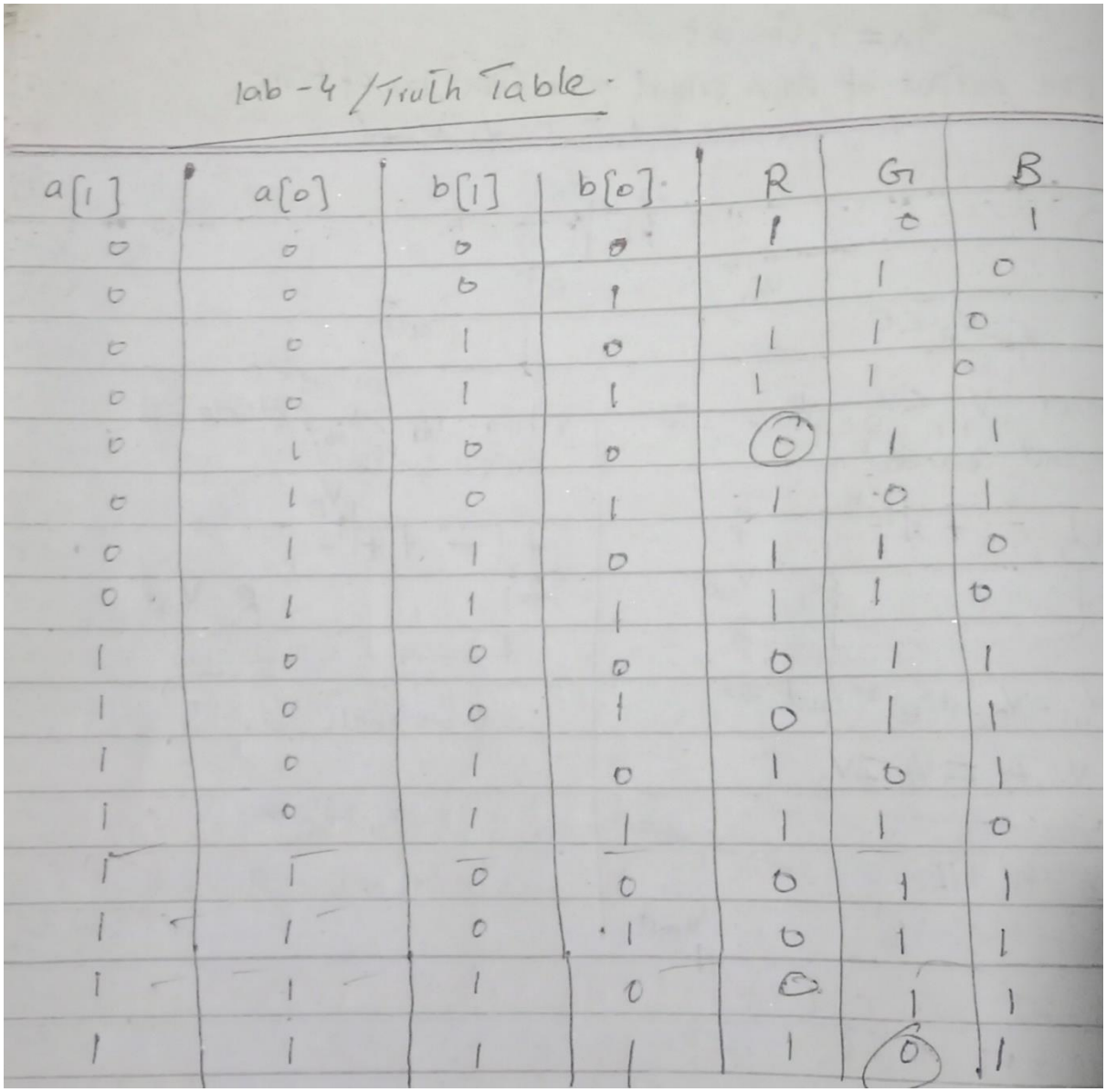
Reg. No.: 2022-EE-119 Marks Obtained: _____

Lab Manual

DSD Lab Manual Evaluation Rubrics

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

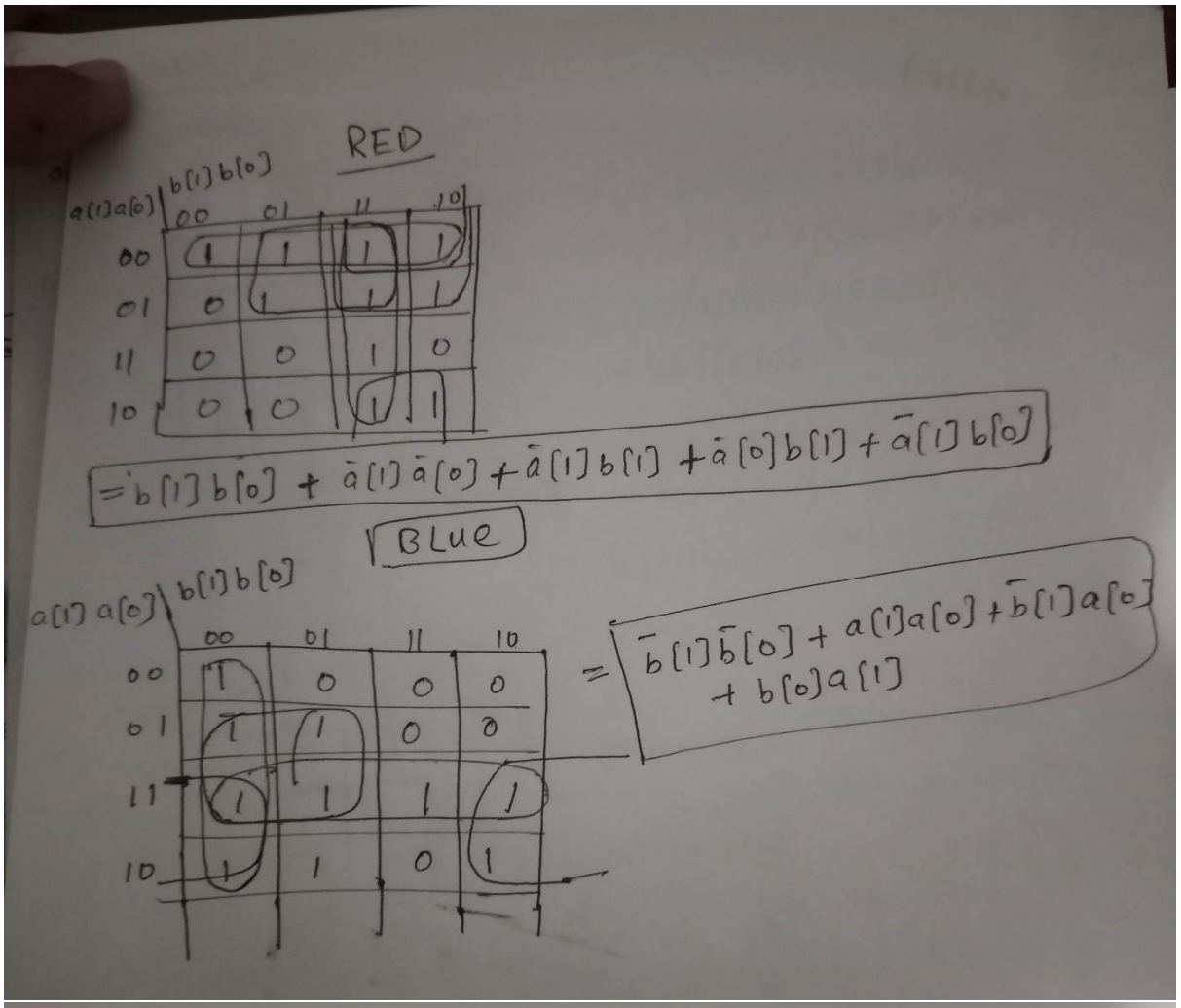
Task (a):

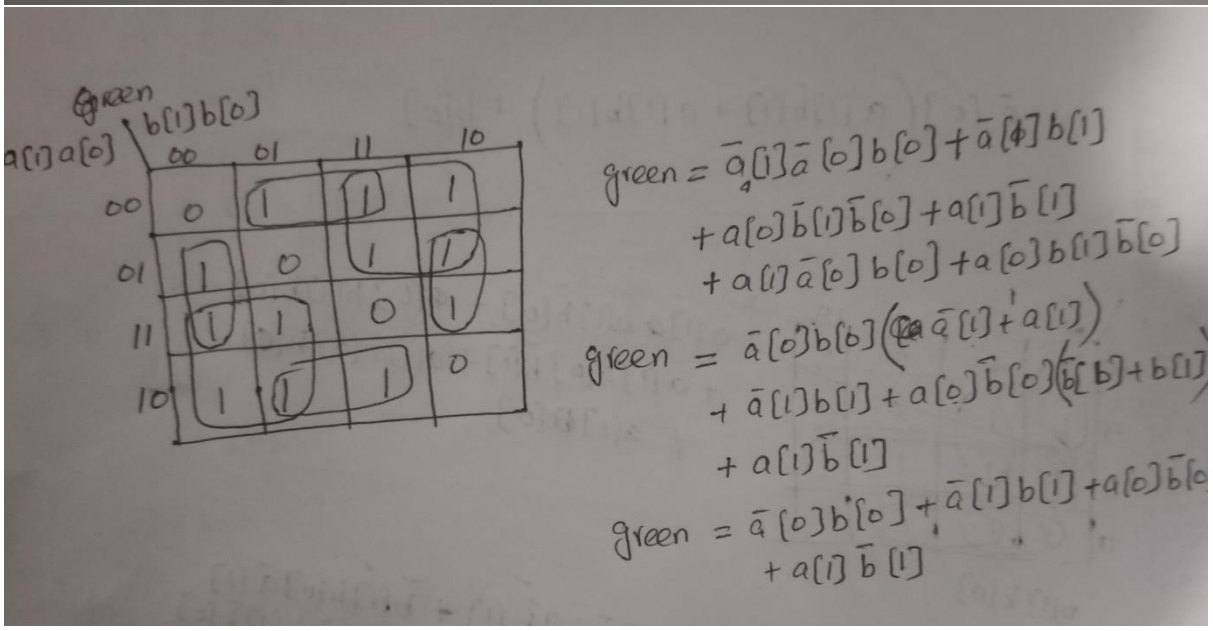


lab-4 / Truth Table:

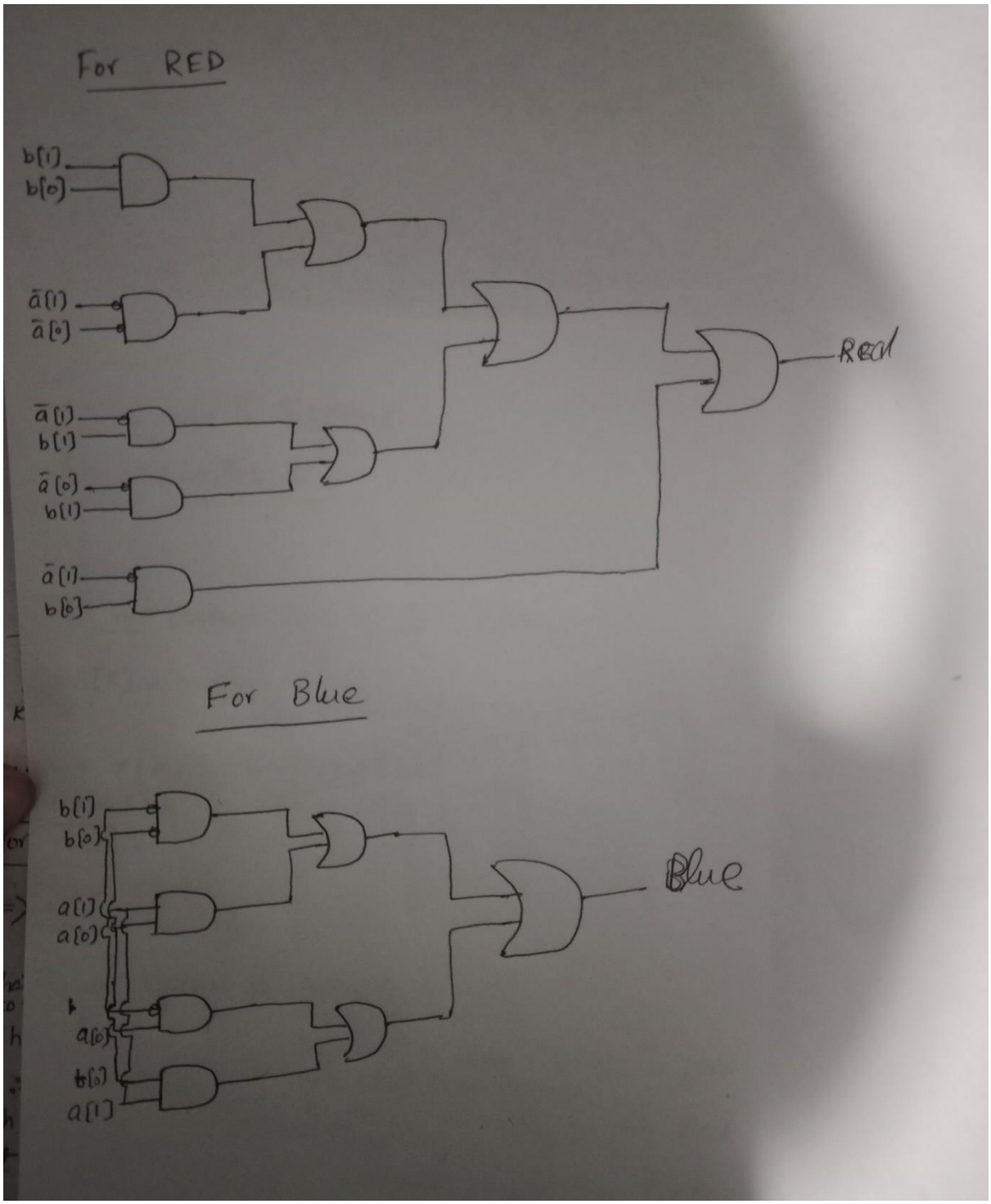
a[1]	a[0]	b[1]	b[0]	R	G	B
0	0	0	0	1	0	1
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	1	1	0
0	1	0	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	0
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Task (b)

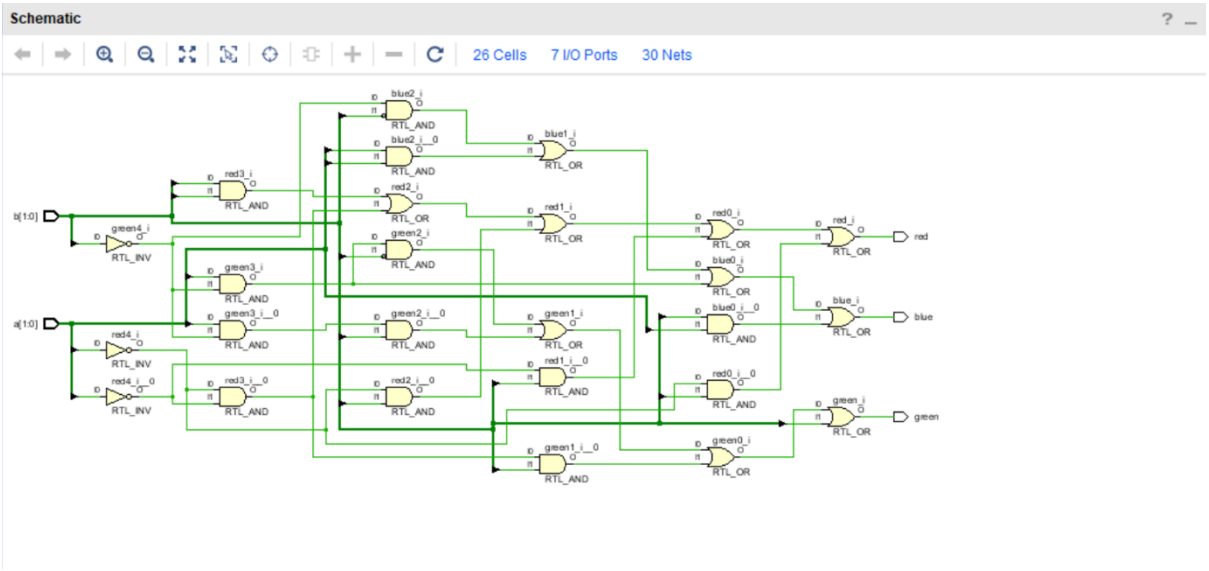

RED
b[1] b[0]
a[1] a[0]
00 01 11 10
00 1 1 1 1
01 0 1 1 1
11 0 0 1 0
10 0 0 1 1
= b[1] b[0] + ā[1] ā[0] + ā[1] b[1] + ā[0] b[1] + ā[1] b[0]
BLUE
b[1] b[0]
a[1] a[0]
00 01 11 10
00 1 0 0 0
01 1 1 0 0
11 1 1 1 1
10 1 1 0 1
= b̄[1] b̄[0] + a[1] a[0] + b̄[1] a[0] + b[0] a[1]


green
b[1] b[0]
a[1] a[0]
00 01 11 10
00 0 1 1 1
01 1 0 1 1
11 1 1 0 1
10 1 1 1 0
green = ā[1] ā[0] b[0] + ā[1] b[1]
+ a[0] b̄[1] b̄[0] + a[1] b̄[1]
+ a[1] ā[0] b[0] + a[0] b[1] b̄[0]
green = ā[0] b[0] (a ā[1] + a[1])
+ ā[1] b[1] + a[0] b̄[0] (b̄[1] + b[1])
+ a[1] b̄[1]
green = ā[0] b̄[0] + ā[1] b[1] + a[0] b̄[0]
+ a[1] b̄[1]

Task (c)


For RED
b[1]
b[0]
ā[1]
ā[0]
ā[1]
b[1]
ā[0]
b[1]
ā[1]
b[0]
Red
For Blue
b[1]
b[0]
a[1]
a[0]
a[0]
b[0]
a[1]
Blue

Task (d)



Part (e)

a[0]	blue	8.044	SLOW	2.391	FAST
a[0]	green	8.056	SLOW	2.368	FAST
a[0]	red	8.439	SLOW	2.510	FAST
a[1]	blue	8.769	SLOW	2.659	FAST
a[1]	green	8.782	SLOW	2.634	FAST
a[1]	red	9.200	SLOW	2.771	FAST
b[0]	blue	8.615	SLOW	2.615	FAST
b[0]	green	8.638	SLOW	2.604	FAST
b[0]	red	9.054	SLOW	2.740	FAST
b[1]	blue	8.375	SLOW	2.473	FAST
b[1]	green	8.398	SLOW	2.461	FAST
b[1]	red	8.816	SLOW	2.599	FAST

Part (f)

IBUF	4
OBUF	3
LUT4	3
Bonded IOB	7
Slice LUT*s	2
LUT as Logic	2

Simulation on Questasim