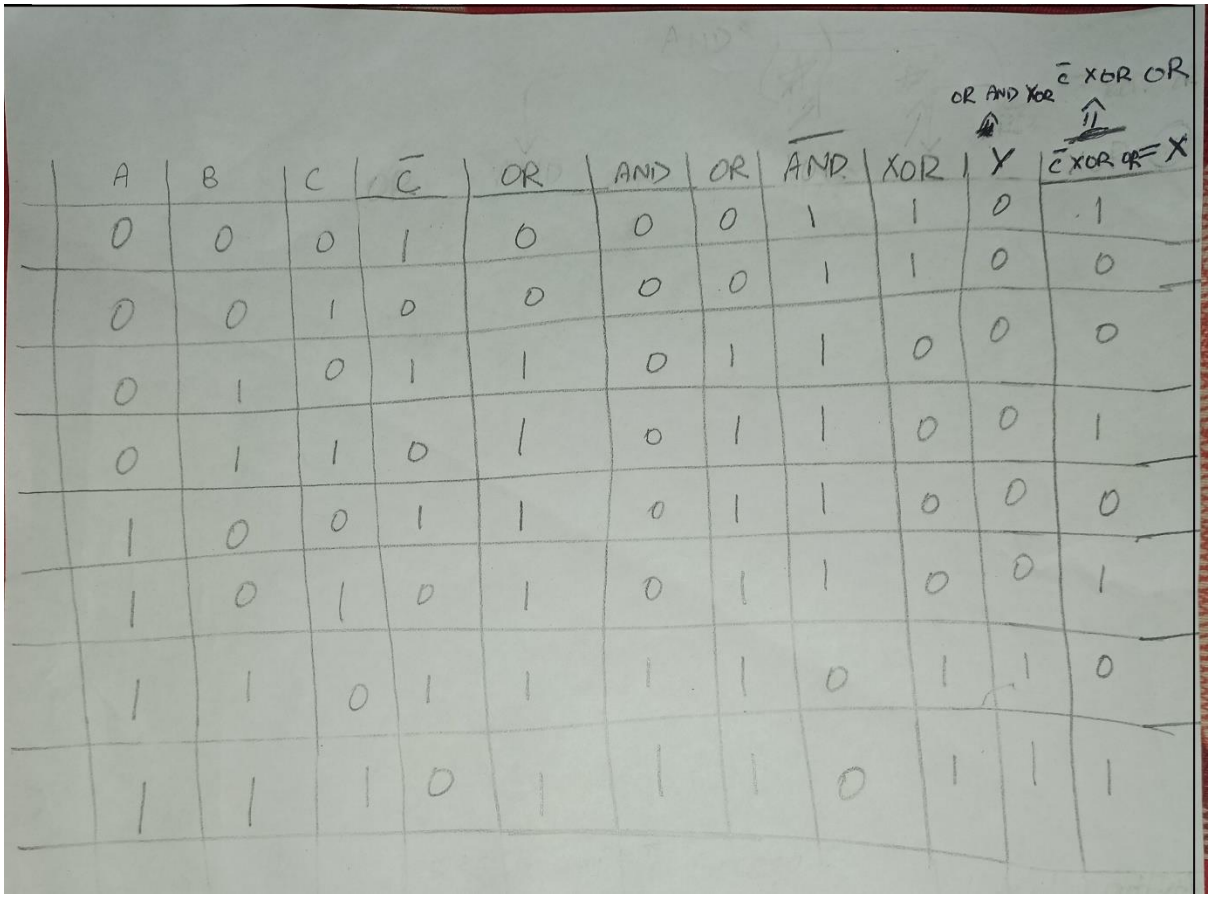
Part 1

a) Truth Table of the circuit:



A	B	C	$\bar{C}$	OR	AND	OR	$\overline{AND}$	XOR	X	$\bar{C}$ XOR OR = X
0	0	0	1	0	0	0	1	1	0	1
0	0	1	0	0	0	0	1	1	0	0
0	1	0	1	1	0	1	1	0	0	0
0	1	1	0	1	0	1	1	0	0	1
1	0	0	1	1	0	1	1	0	0	0
1	0	1	0	1	0	1	1	0	0	1
1	1	0	1	1	1	1	0	1	1	0
1	1	1	0	1	1	1	0	1	1	1

b) Maximum combinational Delay:

From port c to port x, we have maximum combinational delay of 8.951.

c) Resource Utilization:

Slice LUTs*	1
LUT as logic	1
Bonded IOB	5
IBUF	3
OBUF	2
LUT3	1
LUT2	1

Part 2

E: > Semester 4 Labs > EE-120B Digital Systems > Lab_3 > lab3.sv

```
1   module mycircuit(output x, y,
2                    input a , b , c);
3   assign p1 = ~(a & b);
4   assign p2 = a | b;
5   assign p3 = p1 ^ p2;
6   assign y = p2 & p3;
7   assign c1 = ~c;
8   assign x = c1 ^ p2;
9   endmodule
```