

| Subject Title: Computer Organization Common to CSE Branch | | | | | |
|---|---------------------------|---|---|---|---|
| Course Code: | Year and Semester: II - I | L | T | P | C |
| Prerequisites: Digital Logic Design | | 4 | 0 | 0 | 3 |

Course Objectives:

- To understand basic structures of computers and to understand various machine instructions.
- To understand basic structures of computers and to understand various machine instructions.
- To analyse ALU & I/O organization of a computer.
- To understand various memory systems.
- To analyse functionalities done by processing unit and also learn micro programmed control.

Course Outcomes:

By the end the of the course, the student will be able to

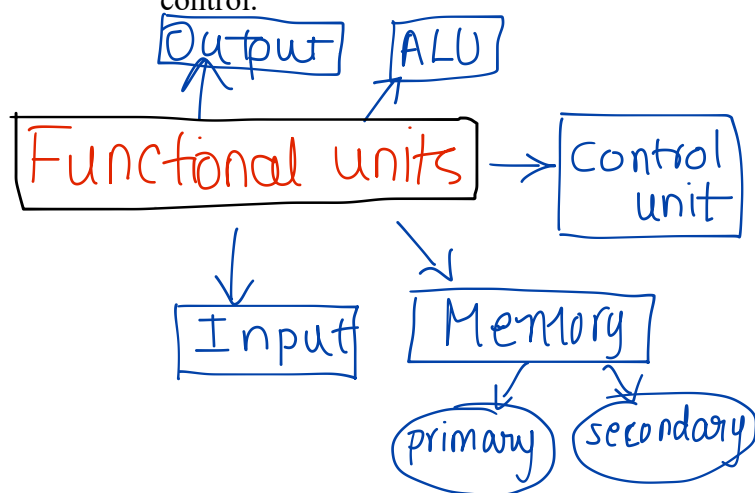
CO-1: Able to **understand** basic structures of computers and to **understand** various machine instructions.

CO-2: Able to **learn and use** the addressing modes and types of instructions.

CO-3: Able to analyze I/O organization of a computer.

CO-4: Able to **understand** various memory systems.

CO-5: Able to **analyze** functionalities done by processing unit and also learn micro programmed control.



Syllabus

Unit – I: Basic Structure of a Computer and Machine Instructions.

Introduction, History of Computer Generations, Functional unit, Basic Operational concepts, Bus structures, System Software, Performance. Number representation: Fixed Point and Floating Point representation. Instruction and Instruction Sequencing: Register Transfer Notation, Assembly Language Notation, Basic Instruction Types

Unit – II: Addressing modes and types of Instructions

Addressing Modes, Basic Input/output Operations, and role of Stacks and Queues in computer programming equation.

Component of Instructions: Logical Instructions, shift and Rotate Instructions. Type of Instructions: Arithmetic and Logic Instructions, Branch Instructions, Addressing Modes, Input/output Operations

Unit – III: Basic building blocks for the ALU:

Adder, Subtractor, Shifter, Multiplication and division circuits. Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, Buses: Synchronous Bus, Asynchronous Bus, Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)

Unit – IV: The Memory Systems

Basic memory circuits, Memory System Consideration, Read- Only Memory: ROM, PROM, EPROM, EEPROM, Flash Memory, Associative Memory, Cache Memories: Mapping Functions, INTERLEAVING, Secondary Storage: Magnetic Hard Disks, Optical Disks.

Unit – V: Processing unit

Fundamental Concepts: Register Transfers, Performing an Arithmetic or Logic Operation, Fetching a Word from Memory, Execution of Complete Instruction, Hardwired Control, MICRO PROGRAMMED CONTROL: Microinstructions, Micro program Sequencing, Wide Branch Addressing Microinstructions with next –Address Field.

| Learning Resources | |
|---|--|
| Text Books: | |
| 1. Computer Organization, Carl Hamacher, ZvonksVranesic, SafeaZaky, 5th Edition, McGraw Hill. 2.Computer Architecture and Organization by William Stallings, PHI Pvt. Ltd., Eastern Economy Edition, Sixth Edition, 2003 | |
| Reference Books | |
| 1. Computer Architecture and Organization, John P. Hayes, 3rd Edition, McGraw Hill. 2. Computer System Architecture by M Morris Mano, Prentice Hall of India, 2001 | |
| e- Resources & other digital material | |
| | |

| Course Outcomes | |
|---|---|
| Upon successful completion of the course, the student will be able to | |
| CO1 | Able to understand basic structures of computers and to understand various machine instructions. {Understand level, KL2} |
| CO2 | Ableto learn and use the addressing modes and types of instructions. {Apply level, KL3} |
| CO3 | Able to analyze I/O organization of a computer. {Apply level, KL3} |
| CO4 | Able to understand various memory systems. { Apply level, KL3} |
| CO5 | Able to analyze functionalities done by processing unit and also learn micro programmed control. {Apply level, KL3} |

CO-PO-PSO Mapping:

| CO'S | STATEMENT | PO's | PSO's |
|------------|---|------------------------------|------------|
| CO1 | Able to understand basic structures of computers and to understand various machine instructions | PO1 | PSO2 |
| CO2 | Ableto learn and use the addressing modes and types of instructions | PO1, PO3 | PSO2 |
| CO3 | Able to analyze I/O organization of a computer | PO2, PO3 | PSO1 |
| CO4 | Able to understand various memory systems | PO2, PO3 | PSO1 |
| CO5 | Able to analyze functionalities done by processing unit and also learn micro programmed control | PO1, PO2, PO3, PO4,PO11,PO12 | PSO1, PSO2 |

CO-PO Mapping Matrix:

| Course Outcome | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO 10 | PO 11 | PO 12 |
|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|-------|
| CO1 | 2 | - | - | - | - | - | - | - | - | - | - | - |
| CO2 | 2 | - | 2 | - | - | - | - | - | - | - | - | - |
| CO3 | - | 2 | 2 | - | - | - | - | - | - | - | - | - |
| CO4 | - | 2 | 2 | - | - | - | - | - | - | - | - | - |
| CO5 | 2 | 2 | 2 | 1 | - | - | - | - | - | - | 2 | 2 |

CO-PSO Mapping Matrix:

| | PSO-1 | PSO-2 |
|------------|-------|-------|
| CO1 | - | 2 |
| CO2 | - | 2 |
| CO3 | 2 | - |
| CO4 | 2 | - |
| CO5 | 2 | 2 |

MICRO SYLLABUS**Unit – I: Basic Structure of a Computer and Machine Instructions.**

Introduction, History of Computer Generations, Functional unit, Basic Operational concepts, Bus structures, System Software, Performance. Number representation: Integer - unsigned, signed (sign magnitude, 1's complement, 2's complement); Characters - ASCII coding, other coding schemes; Real numbers - fixed and floating point, IEEE754 representation. Instruction and Instruction Sequencing: Register Transfer Notation, Assembly Language Notation, Basic Instruction Types

Unit – II: Addressing modes and types of Instructions

Addressing Modes, Basic Input/output Operations, and role of Stacks and Queues in computer programming equation.

Component of Instructions: Logical Instructions, shift and Rotate Instructions. Type of Instructions: Arithmetic and Logic Instructions, Branch Instructions, Addressing Modes, Input/output Operations

Unit – III: Basic building blocks for the ALU

Adder, Subtractor, Shifter, Multiplication and division circuits. Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, Buses: Synchronous Bus, Asynchronous Bus, Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)

Unit – IV: The Memory Systems

Main Memory: Basic memory circuits, Memory System Consideration, Read- Only Memory: ROM, PROM, EPROM, EEPROM, Flash Memory, and Associative Memory.

Cache Memories: Mapping Functions, INTERLEAVING,

Secondary Storage: Magnetic Hard Disks, Optical Disks.

Unit – V: Processing unit

Fundamental Concepts: Register Transfers, Performing an Arithmetic or Logic Operation, Fetching a Word from Memory, Execution of Complete Instruction, Hardwired Control, MICRO PROGRAMMED CONTROL: Microinstructions, Micro program Sequencing, Wide Branch Addressing Microinstructions with next –Address Field.

| Learning Resources |
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| e- Resources & other digital material |
| https://nptel.ac.in/courses/106/105/106105163/ |