Microprocessors

A microprocessor requires an external memory for program/data storage.

Instruction execution requires movement of data from the external memory to the microprocessor or vice versa.

Usually, microprocessors have good computing power and they have higher clock speed to facilitate faster computation.

Microcontrollers

A microcontroller has required on-chip memory with associated peripherals. A microcontroller can be thought of a microprocessor with inbuilt peripherals.

Microcontroller maybe called computer on chip since it has basic features of microprocessor(like ALU, registers, flags, program counter, stack pointer, clock and interrupt circuit)

- A microcontroller does not require much additional interfacing ICs for operation and it functions as a stand alone system.

- Microcontroller are special purpose devices , while microprocessors are general purpose devices.

- There are numerous microcontrollers and many of them are application specific.

MICROCONTROLLER APPLICATIONS

- Microcontrollers are used extensively in robotics.
- In addition to control applications such as the home monitoring system, microcontrollers are frequently found in embedded applications.
- Among the many uses that you can find one or more microcontrollers: automotive applications, appliances (microwave oven, refrigerators, television and VCRs, stereos), automobiles (engine control, diagnostics, climate control).

INTEL 8051 (8 BIT MASK ROM)

Features:

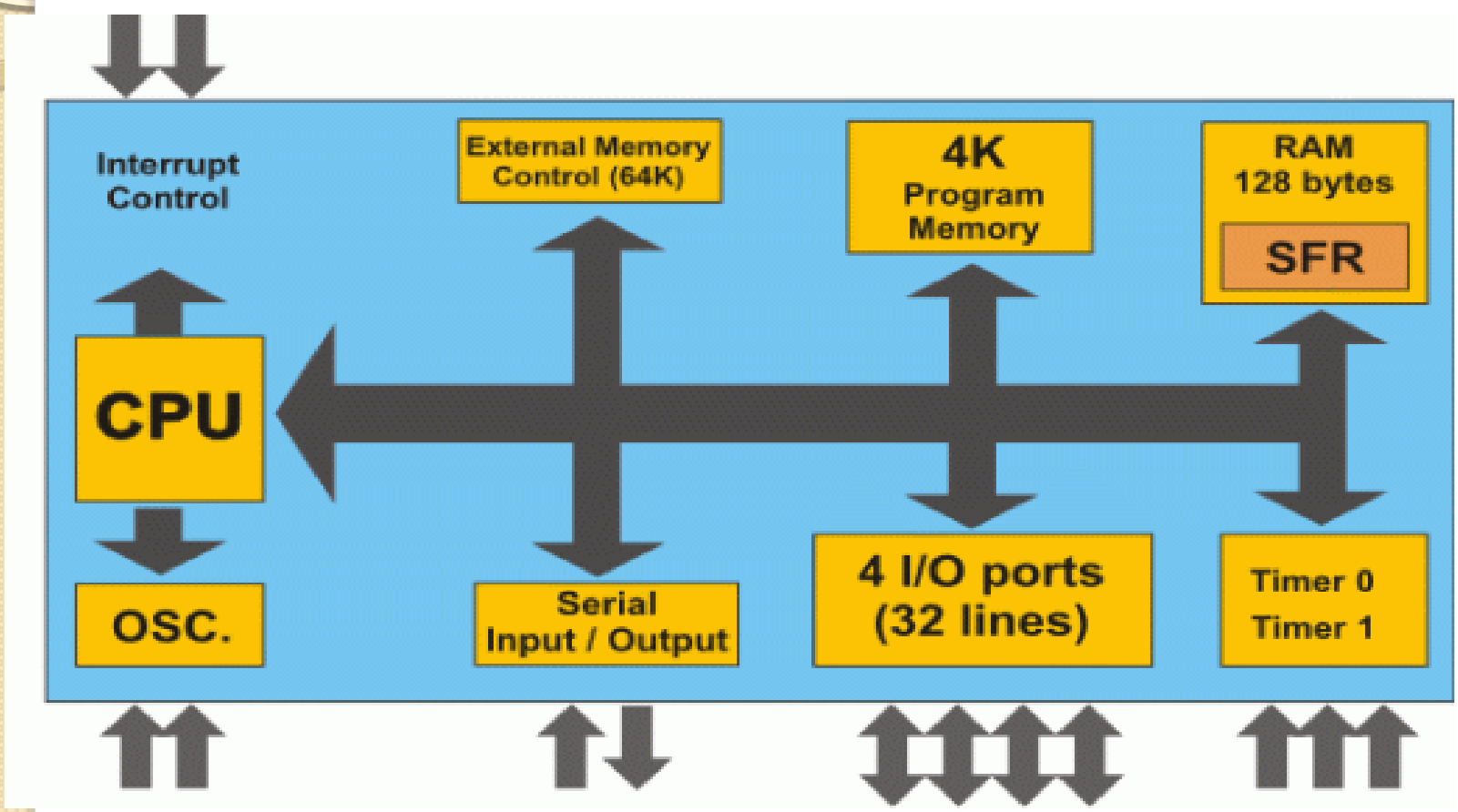
- 4 KB on chip program memory(internal ROM).
- 128 bytes on chip data memory(internal RAM).
- 8 bit CPU (means it can work on only 8 bits of data at a time) with register A and B.
- 8-bit data bus

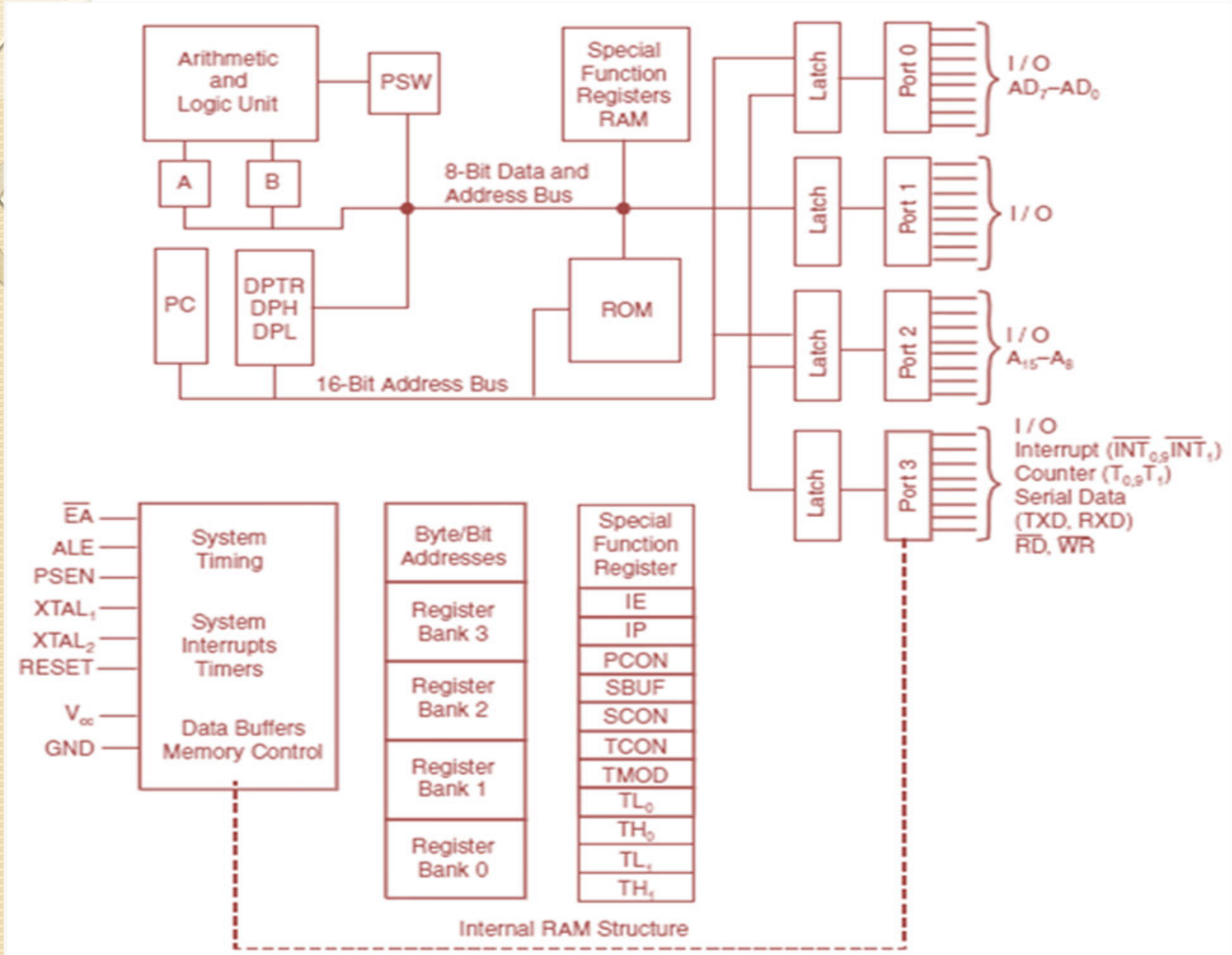
- 16-bit address bus
- Two 16 bit timers (T0 and T1).
- Four 8-bit ports(P0-P3) i.e. 32 I/O pins.

- 16-bit program counter(PC) and data pointer(DPTR) registers.
- 8 bit Program Status Word(PSW)- the flag register.
- 8 bit Stack Pointer(SP).
- 4 register banks.

Typical applications

- 8051 chips are used in a wide variety of control systems, telecom applications, robotics as well as in the automotive industry , TV, video games, washing machine.


Interrupt Control
External Memory Control (64K)
4K Program Memory
RAM 128 bytes
SFR
CPU
OSC.
Serial Input / Output
4 I/O ports (32 lines)
Timer 0
Timer 1


Arithmetic and Logic Unit
PSW
A
B
PC
DPTR DPH DPL
Special Function Registers RAM
8-Bit Data and Address Bus
ROM
16-Bit Address Bus
Latch
Port 0
I / O
AD7–AD0
Port 1
I / O
Port 2
I / O
A15–A8
Port 3
I / O
Interrupt (INT0, INT1)
Counter (T0, T1)
Serial Data
(TXD, RXD)
RD, WR
EA
ALE
PSEN
XTAL1
XTAL2
RESET
Vcc
GND
System Timing
System Interrupts Timers
Data Buffers Memory Control
Byte/Bit Addresses
Register Bank 3
Register Bank 2
Register Bank 1
Register Bank 0
Special Function Register
IE
IP
PCON
SBUF
SCON
TCON
TMOD
TL0
TH0
TL1
TH1
Internal RAM Structure

Registers of 8051

- Various registers used for specific functions e.g. A,PC etc which are not part of internal RAM.
- These registers are known as Special Function Registers (SFR).
- These registers maybe addressed using internal addresses range from 80H to FFH except the Program Counter.
- The addresses from range 00H to 7FH are used by RAM registers.

- **Internal Memory (ROM AND RAM)**

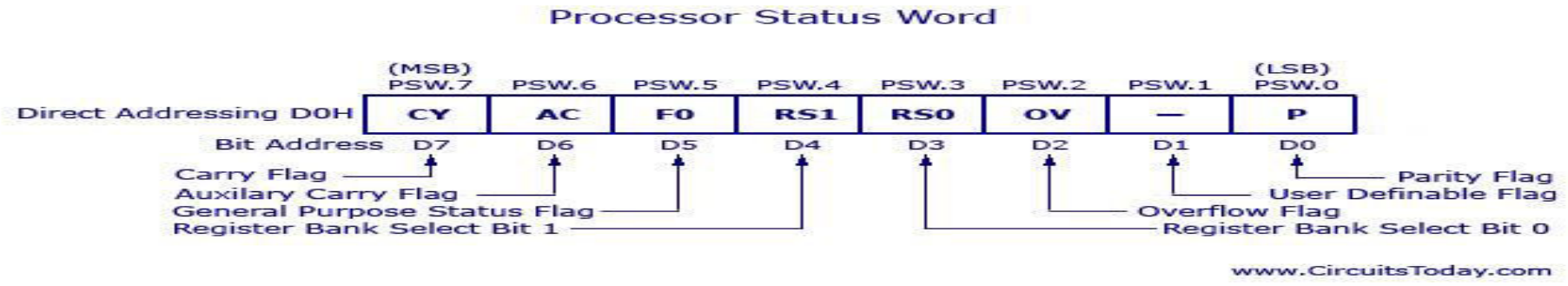
  - ROM (4K) is used to store program code for application at time of manufacturing, once written cant be altered.

  - RAM (128 Byte) used to store variable data during execution of program.

i) Working Registers

- With the register banks from locations 00H to 1FH, you may only read or write a full byte (8 bits) at these locations.
- Each register can be addressed by name e.g. R5 of bank 2 can be accessed by name R5, after selecting bank 2 by making RS0=0 and RS1=1 in PSW register.
- Or it can be addressed by address 15H, whether bank 2 is selected or not.

- On resetting 8051 , register bank 0 is selected by default.
- The D3 and D4 bits of register PSW are often referred to as PSW.3 and PSW.4 since they can be accessed by bit addressable instructions SETB and CLR.
- For eg. “SETB PSW.3” will make PSW.3=1 and select bank register 1.



(ii) Bit Addressable Registers (16 Byte)

- 16 registers of RAM with byte address range 20H to 2FH are bit addressable.
- Each bit of these 16 registers(16*8=128 bits) has its own address range from 00H to 7FH.
- These addressable bits are useful , when any information represented by a single bit is to be stored.

- Because internal RAM has limited space available, so there is no need to use 8-bit register when a single bit solves the purpose.

- With bit-addressable RAM (20H to 2FH) you can read or write any single bit in this region by using the unique address for that bit.

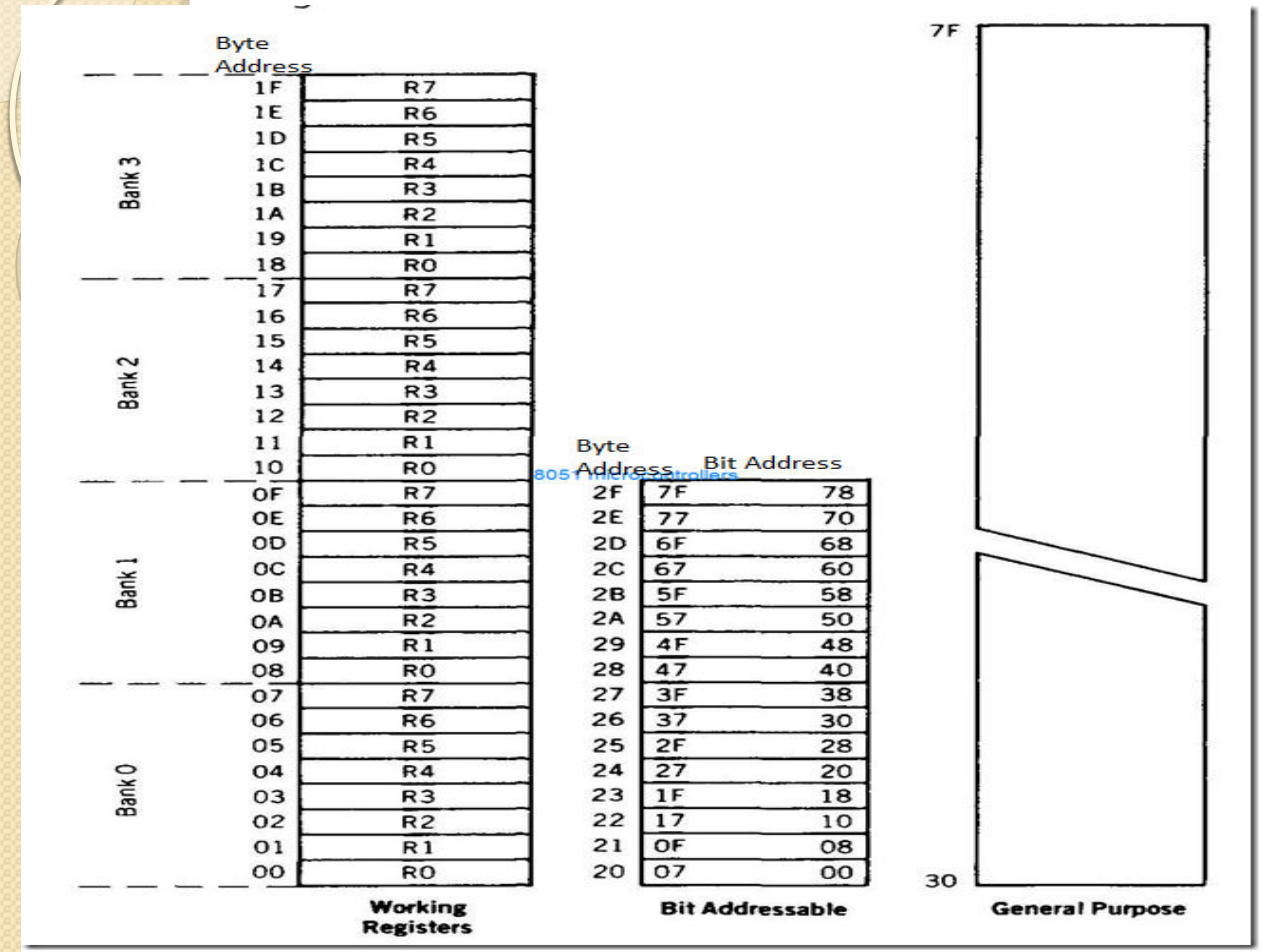
Byte Addr	Bit Number 7	6	5	4	3	2	1	0
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00

Fig :-
Bit Addressable Area

(iii) General Purpose Area (80 Byte)

- The area above the bit area, from 30H to 7FH is the general purpose area which is shared with DATA and SFR.

- With the general purpose RAM from 30H to 7FH, you may only read or write a full byte (8 bits) at these locations i.e. it is byte addressable.



Internal RAM organization

Special Function Register

- There **are 21 Special function registers (SFR)** in 8051 micro controller and this includes Register A, Register B, Processor Status Word (PSW), PCON etc.

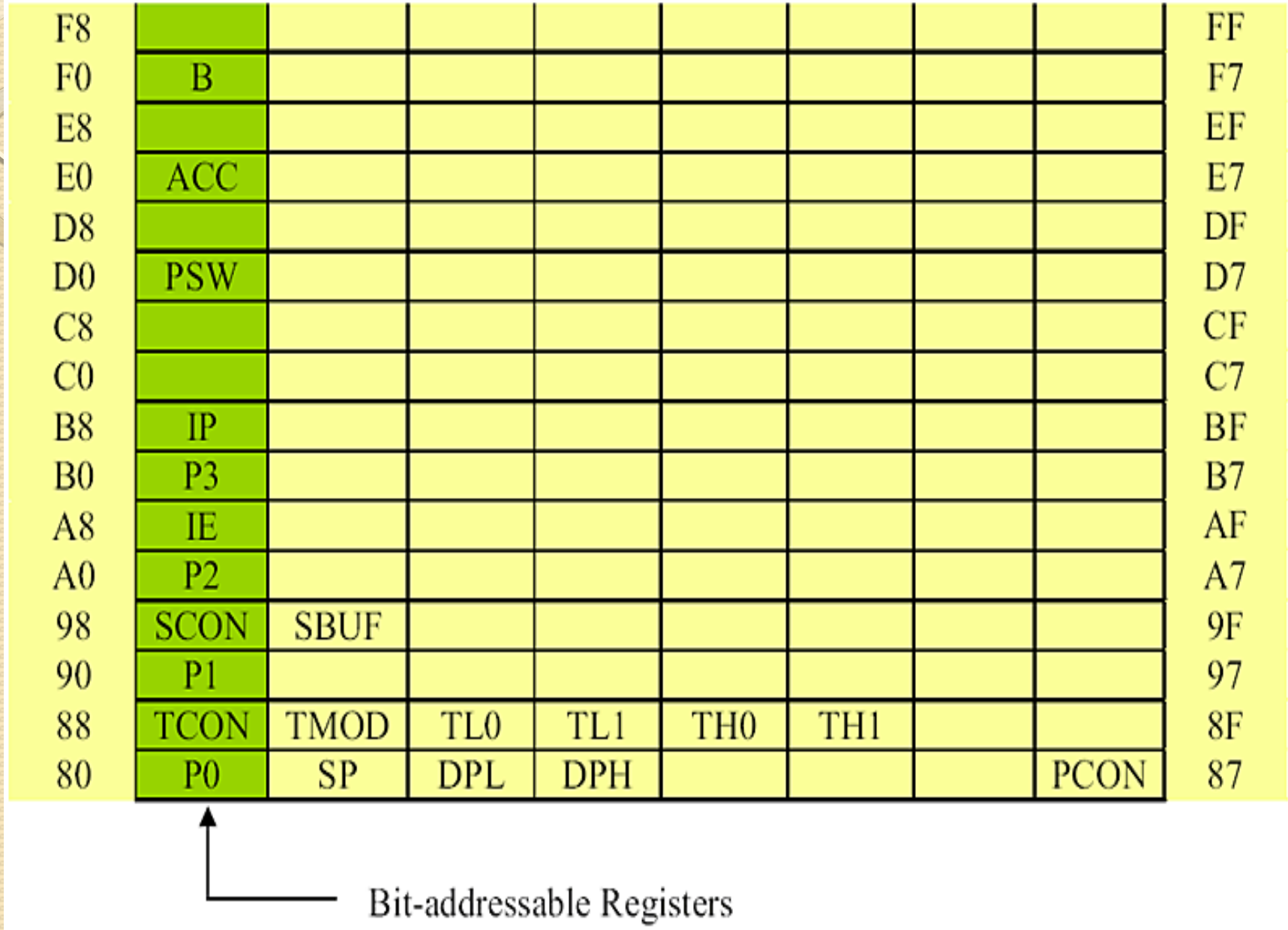
- There are 21 unique locations for these 21 special function registers and each of these register is of 1 byte size.

- Some of these special function registers ***are bit addressable*** (which means you can access 8 individual bits inside a single byte), while some others are ***only byte addressable.***

- The **Special Function Register** (SFR) is the upper area of addressable memory, from address 80H to FFH. There are 128 memory locations intended to be occupied by them. A, B, PSW, DPTR are called SFR.

- The addresses ranging from 00H to 7FH are used by RAM registers.

- This area of memory cannot be used for data or program storage.


F8
F0
E8
E0
D8
D0
C8
C0
B8
B0
A8
A0
98
90
88
80
B
ACC
PSW
IP
P3
IE
P2
SCON
SBUF
P1
TCON
TMOD
TL0
TL1
TH0
TH1
P0
SP
DPL
DPH
PCON
FF
F7
EF
E7
DF
D7
CF
C7
BF
B7
AF
A7
9F
97
8F
87
Bit-addressable Registers

NAME	FUNCTION	INTERNAL RAM ADDRESS
A	ACCUMULATOR	E0H*
B	ARITHMETIC OPERATIONS	F0H*
DPH	ADDRESSING EXTERNAL MEMORY	83H
DPL	ADDRESSING EXTERNAL MEMORY	82H
IE	INTERRUPT ENABLE CONTROL	A8H*
IP	INTERRUPT PRIORITY	B8H*
P0	INPUT/OUTPUT PORT 0	80H*
P1	INPUT/OUTPUT PORT 1	90H*

P3	INPUT/OUTPUT PORT 3	B0H*
PC	PROGRAM COUNTER	--
PCON	POWER MODE CONTROL	87H
PSW	PROGRAM STATUS WORD (FLAGS)	D0H*
SCON	SERIAL PORT CONTROL	98H*
SBUF	SERIAL DATA BUFFER	99H
SP	STACK POINTER	81H
TMOD	TIMER/COUNTER MODE CONTROL	89H
TCON	TIMER/COUNTER CONTROL	88H*
TL0	TIMER 0 LOW-BYTE	8AH
TH0	TIMER 0 HIGH-BYTE	8CH
TL1	TIMER 1 LOW-BYTE	8BH

A and B Registers

- These registers are used to store the result of various arithmetic & logical operations.
- The A register is called the **accumulator**, and by default it receives the result of all arithmetic operations.
- It is used for addition, subtraction , multiplication and division etc.

- Register A is also used for data transfer b/w microcontroller & external memory.

- The B register is used with the accumulator for multiplication & division or to store data and has no other function. In this registers we can store data up to 16 bit.

Processor Status Word (PSW)

- This is a vital SFR in the functioning of micro controller. This register reflects the status of the operation that is being carried out in the processor.
- PSW register is both bit and byte addressable.
- Flags are flip-flops, grouped together inside PSW and Power Mode Control (PCON) registers.

- The F0 is a general purpose flag defined by the programmer to record some events in program.

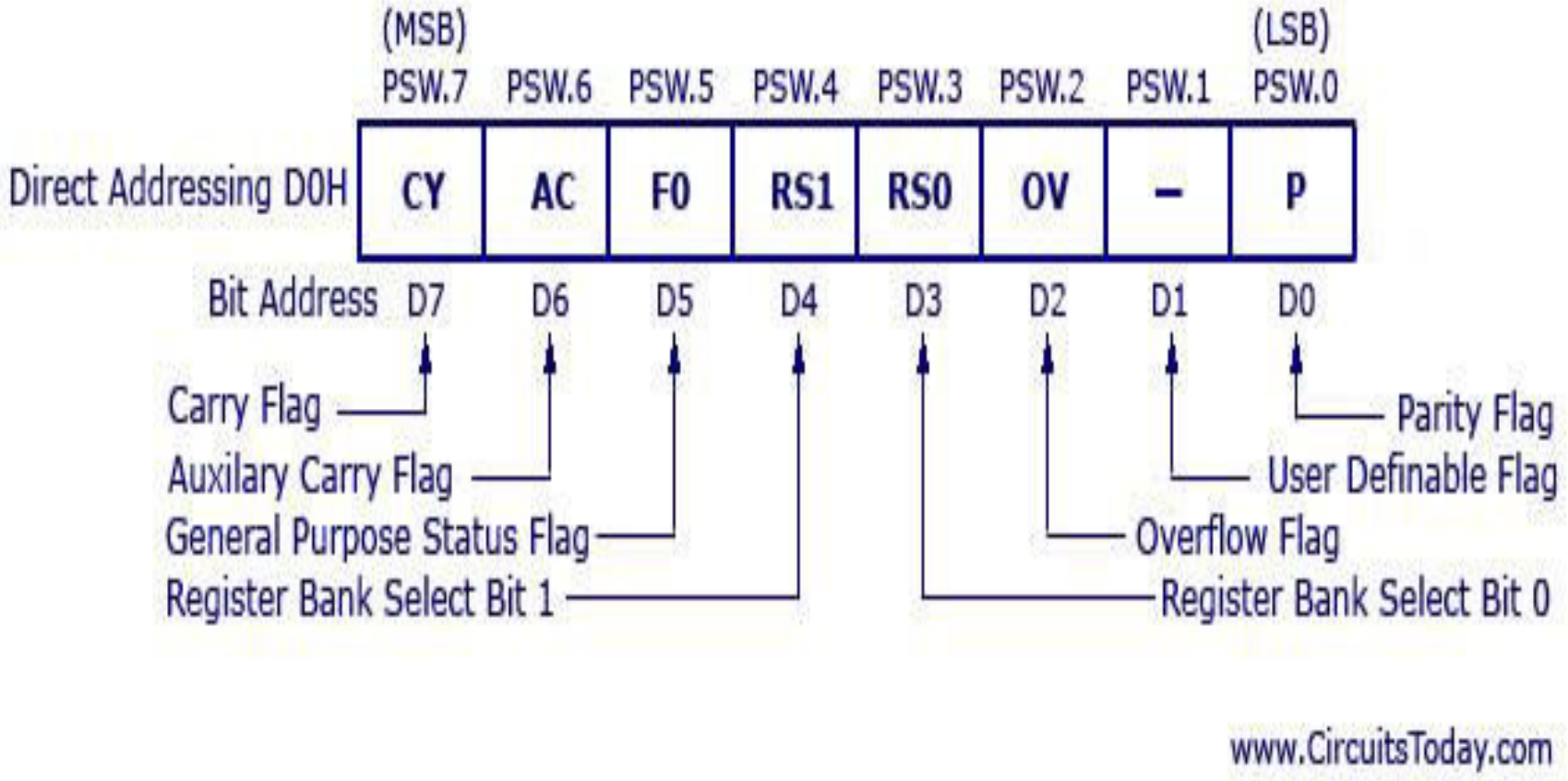
- The physical address of PSW starts from D0H. The individual bits are then accessed using D1, D2 … D7.

P the parity flag

- The parity flag reflects the number of 1 s in the A (accumulator) register only.

- If the A register contains an odd number of ls, **then P = 1. Therefore, P = 0 if A has an even number of 1s.**

Processor Status Word



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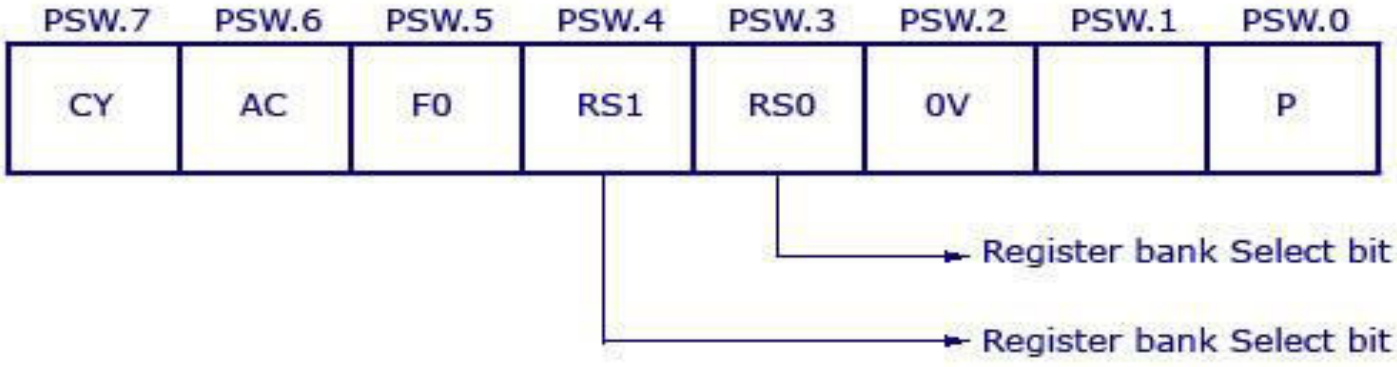
Processor Status Word



RS1	RS0	Register Bank	Register Bank Status
0	0	0	Register Bank 0 is selected
0	1	1	Register Bank 1 is selected
1	0	2	Register Bank 2 is selected
1	1	3	Register Bank 3 is selected

Bit No	Bit Symbol	Direct Address	Name	Function
0	P	D0	Parity	This bit will be set if ACC has odd number of 1's after an operation. If not, bit will remain cleared.
1	-	D1		User definable bit
2	OV	D2	Overflow	OV flag is set if there is a carry from bit 6 but not from bit 7 of an Arithmetic operation. It's also set if there is a carry from bit 7 (but not from bit 6) of Acc
3	RS0	D3	Register Bank select bit 0	LSB of the register bank select bit. Look for explanation below this table.
4	RS1	D4	Register Bank select bit 1	MSB of the register bank select bits.
5	F0	D5	Flag 0	User defined flag
6	AC	D6	Auxiliary carry	This bit is set if data is coming out from bit 3 to bit 4 of Acc during an Arithmetic operation.
7	CY	D7	Carry	Is set if data is coming out of bit 7 of Acc during an Arithmetic operation.

OV the overflow flag

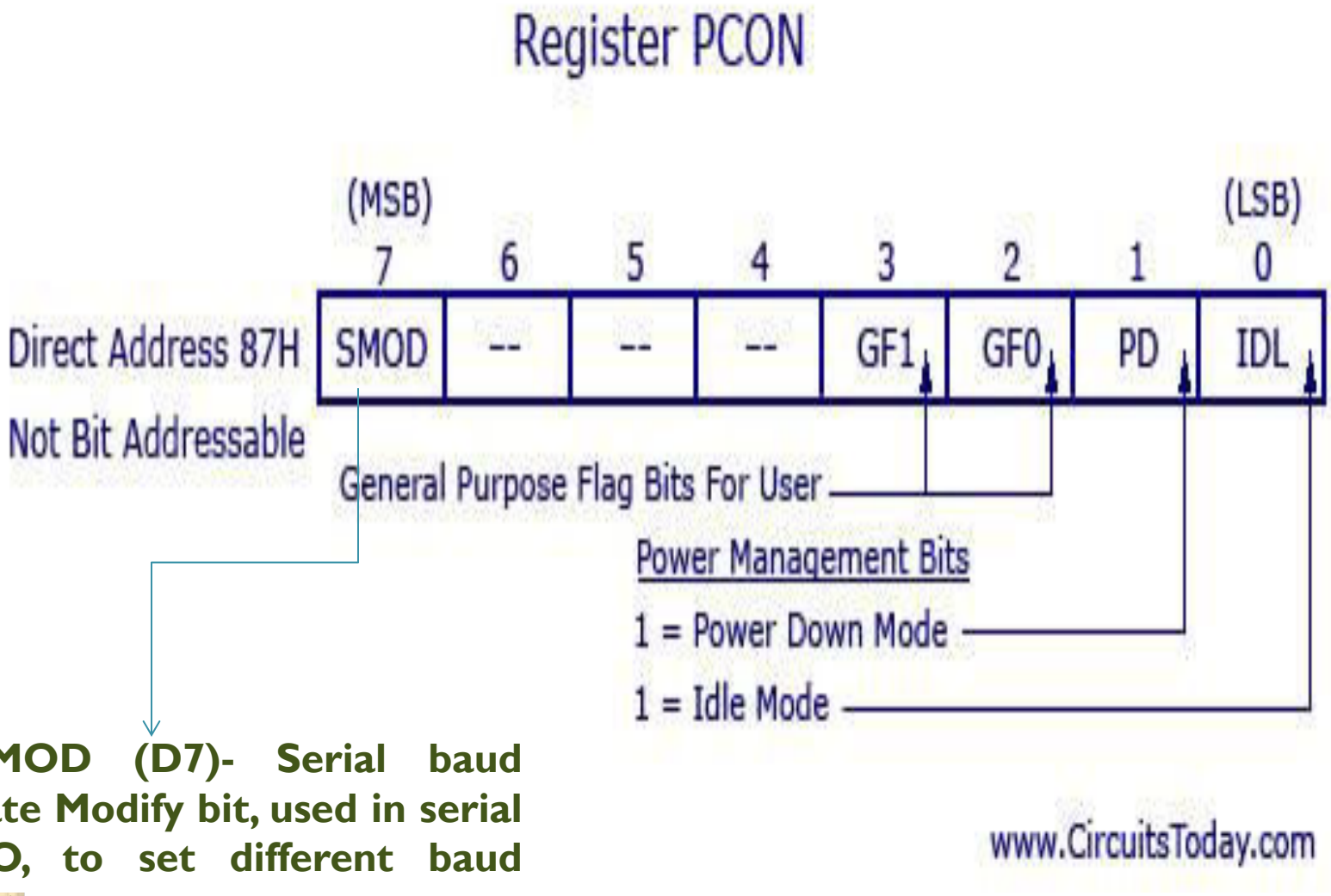
- This flag is set whenever the result of a signed number operation is too large, causing the high-order bit to overflow into the sign bit.
- In general, the carry flag is used to detect errors in unsigned arithmetic operations.
- The overflow flag is only used to detect errors in signed arithmetic operations.

Power Mode control Register (PCON)

- Power management using a microcontroller is something you see every day in mobile phones. PCON is not bit addressable.

- A mobile phone can automatically go into stand by mode when not used for a couple of seconds, this is achieved by power management feature of the controller used inside that phone.

- This register is used for efficient power management of 8051 micro controller. This is a dedicated SFR for power management alone. There are 2 modes for this register :- ***Idle mode and Power down mode.***



SMOD (D7)- Serial baud rate Modify bit, used in serial I/O, to set different baud rates

POWER DOWN MODE:

- By setting the PD bit of the PCON register from within the program we can turning off its internal oscillator and reduces power consumption enormously.
- The only way to get the micro controller back to normal mode is by reset.
- While the microcontroller is in Power Down mode, the state of all SFR registers and I/O ports remains unchanged.
- By setting it back into the normal mode, the contents of the SFR register is lost, but the content of internal RAM is saved.

IDLE MODE:

- Upon the IDL bit of the PCON register is set, the microcontroller turns off the greatest power consumer-CPU unit while peripheral units such as serial port, timers and interrupt system continue operating normally.
- In Idle mode, the state of all registers and I/O ports remains unchanged.
- In order to exit the Idle mode and make the microcontroller operate normally, it is necessary to enable and execute any interrupt or reset.

Program Counter

- It is a 16 bit register, used to hold the address of program instruction byte to be fetched from the memory and executed. The ROM may be:

i. On-chip ROM, memory address range from 0000H to 0FFFH.

ii. Additional external ROM , for address exceeding 0FFFH up to FFFFH.

iii. Totally external ROM , address range from 0000H to FFFFH.

- PC is automatically incremented after every instruction byte is fetched . It is the only register which does not have an internal address.

Data Pointer(DPTR)

- It is made up of two 8-bit registers DPH and DPL used to provide memory address for (i) internal and external code access and (ii) external data access.
- The DPTR register is the only user accessible register it is used to point to data, often used to point to data in external memory.
- The 8 bit registers DPH and DPL are assigned internal addresses, but the whole 16-bit register DPTR doesn't have a single internal address.

Stack Pointer(SP)

- Stack is an area of internal RAM that is used to store and retrieve data during execution of program.
- Stack pointer is an 8 bit register used to store 8 bit address of one of the locations in RAM, called the top of stack.
- It is a byte addressable register, which means you cant access individual bits of stack pointer.

- The Stack & Stack Pointer can be used in same way as for 8085 microprocessor using PUSH and POP instructions.
- The content of the stack pointer points to the last stored location of system stack.
- To store something new in system stack , the SP must be incremented by 1 first and then execute the “store” command.

SFR	Address	Function
DPH	83	Data pointer registers (High). Only byte addressing possible.
DPL	82	Data pointer register (Low). Only byte addressing possible.
IP	B8	Interrupt priority. Both bit addressing and byte addressing possible.
IE	A8	Interrupt enable. Both bit addressing and byte addressing possible.
SBUF	99	Serial Input/Output buffer. Only byte addressing is possible.
SCON	98	Serial communication control. Both bit addressing and byte addressing possible.
TCON	88	Timer control. Both bit addressing and byte addressing possible.
TH0	8C	Timer 0 counter (High). Only byte addressing is possible.
TL0	8A	Timer 0 counter (Low). Only byte addressing is possible.
TH1	8D	Timer 1 counter (High). Only byte addressing is possible.
TL1	8B	Timer 1 counter (Low). Only byte addressing is possible.
TMOD	89	Timer mode select. Only byte addressing is possible.

SCON

- **(Serial Control, Addresses 98h, Bit-Addressable):** SCON controls Data Communication. The Serial Control SFR is used to configure the behavior of the 8051's on-board serial port.

- This SFR controls the baud rate of the serial port, whether the serial port is activated to receive data, and also contains flags that are set when a byte is successfully sent or received.

SCON : Serial Port Control Register (Bit Addressable)

SM0	SM1	SM2	REN	TN8	RB8	TI	RI

SM0	SCON.7	Serial Port mode specifier (NOTE 1).
SM1	SCON.6	Serial Port mode specifier (NOTE 1).
SM2	SCON.5	Enables the multiprocessor communication feature in mode 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0 (See table 9).
REN	SCON.4	Set/Cleared by software to Enable/Disable reception.
TB8	SCON.3	The 9th bit that will be transmitted in modes 2 & 3. Set/Cleared by software.
RB8	SCON.2	In modes 2 & 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	SCON.1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI	SCON.0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or half way through the stop bit time in the other modes (except see SM2). Must be cleared by software.

Note 1 :

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	SHIFT REGISTER	Fosc./12
0	1	1	8 bit UART	Variable
1	0	2	8 bit UART	Fosc./64 OR Fosc./32
1	1	3	8 bit UART	Variable

- **SM0 & SM1** :- The four modes are defined above . Selecting the Serial Mode selects the mode of operation (8-bit/9-bit, UART or Shift Register) and also determines how the baud rate will be calculated. In modes 0 and 2 the baud rate is fixed based on the oscillators frequency. In modes 1 and 3 the baud rate is variable based on how often Timer 1 overflows.

- **SM2:-** It is a flag for "Multiprocessor communication." However, when SM2 is set the "RI" flag will only be triggered if the 9th bit received was a "1". That is to say, if SM2 is set and a byte is received whose 9th bit is clear, the RI flag will never be set. This can be useful in certain advanced serial applications.

- **REN** is "Receiver Enable." If you want to receive data via the serial port, set this bit.

- **TB8 :-** This bit is used in modes 2 and 3. In modes 2 and 3, a total of nine data bits are transmitted. The first 8 data bits are the 8 bits of the main value, and the ninth bit is taken from TB8. If TB8 is set and a value is written to the serial port, the data bits will be written to the serial line followed by a "set" ninth bit. If TB8 is clear the ninth bit will be "clear.“

- The **RB8** also operates in modes 2 and 3 and functions essentially the same way as TB8, but on the reception side. When a byte is received in modes 2 or 3, a total of nine bits are received. In this case, the first eight bits received are the data of the serial byte received and the value of the ninth bit received will be placed in RB8.

- **TI :-** It means "Transmit Interrupt.“When the TI bit is set, the program may assume that the serial port is "free" and ready to send the next byte.

- **RI** :- It means "Receive Interrupt."It functions similarly to the "TI" bit, but it indicates that a byte has been received.

Interrupt Enable Register

→ We can configure the 8051 so that any of the following events will cause an interrupt:

- Timer 0 Overflow.
- Timer 1 Overflow.
- Reception/Transmission of Serial Character.
- External Event 0.
- External Event 1.

Your program may enable and disable interrupts by modifying the IE SFR (A8h)

IE : Interrupt Enable Register (Bit Addressable)

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	-	-	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, interrupt source is individually enable or disabled by setting or clearing its enable bit.
-	IE.6	Not implemented, reserved for future use*.
-	IE.5	Not implemented, reserved for future use*.
ES	IE.4	Enable or disable the Serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

Interrupt Priority

IP : Interrupt Priority Register (Bit Addressable)

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is the corresponding interrupt has a higher priority.

			PS	PT1	PX1	PT0	PX0

-	IP.7	Not implemented, reserved for future use*.
-	IP.6	Not implemented, reserved for future use*.
-	IP.5	Not implemented, reserved for future use*.
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 Interrupt priority level.
PX1	IP.2	Defines External Interrupt priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

- Interrupts with high priority can interrupt another interrupt with a low priority; lower priority interrupt continues after higher is finished.

- If 2 interrupts with same priority occur at same time then they have the following ranking :-

1. IE0
2. TF0
3. IE1
4. TF1
5. SERIAL=RI OR TI

SBUF

- SBUF is physically two registers . One is write only and is used to hold data to be transmitted out of 8051 via TxD . Any value written to SBUF will be sent out the serial port's TXD pin.

- The other is read only and holds received data from external sources via RxD . any value which the 8051 receives via the serial port's RXD pin will be delivered to the user program via SBUF.

- Likewise, In other words, SBUF serves as the output port when written to and as an input port when read from.

PORTS

There are four 8-bit ports: P0, P1, P2 and P3.

- **PORT P1 (Pins 1 to 8)**: The port P1 is a general purpose input/output port which can be used for a variety of interfacing tasks. The other ports P0, P2 and P3 have dual roles or additional functions.

- **PORT P3 (Pins 10 to 17)**: Port P3 acts as a normal I/O port, but Port P3 has additional functions such as, serial transmit and receive pins, 2 external interrupt pins, 2 external counter inputs, read and write pins for memory access.

- **PORT P2 (Pins 21 to 28):** PORT P2 can also be used as a general purpose 8 bit port when no external memory is present, but if external memory access is required then PORT P2 will act as an address bus in conjunction with PORT P0 to access external memory. PORT P2 acts as A8-A15.

- **PORT P0 (Pins 32 to 39):** PORT P0 can be used as a general purpose 8 bit port when no external memory is present, but if external memory access is required then PORT P0 acts as a multiplexed address and data bus that can be used to access external memory in conjunction with PORT P2. P0 acts as AD0-AD7.

Timers/Counters Programming

- Many microcontroller applications require counting of external events such as generation of precise internal time delays b/w computer actions.

- To relieve the processor of this burden two 16 bit up counters named T0 and T1 are provided for the general use of the programmer.

They can be used as :-

1. The **timer** to generate time delay.
   - The counters T0 and T1 maybe programmed to count internal clock pulse to work as timer.
2. An event **counter**.
   - To count external clock pulses to work as counter.
   - These clock pulses could represent the number of wheel rotations, or any other event that can be converted to pulses.

Registers

- The counters are divided into two 8-bit registers , TL for Timer Low and TH for Timer High :-

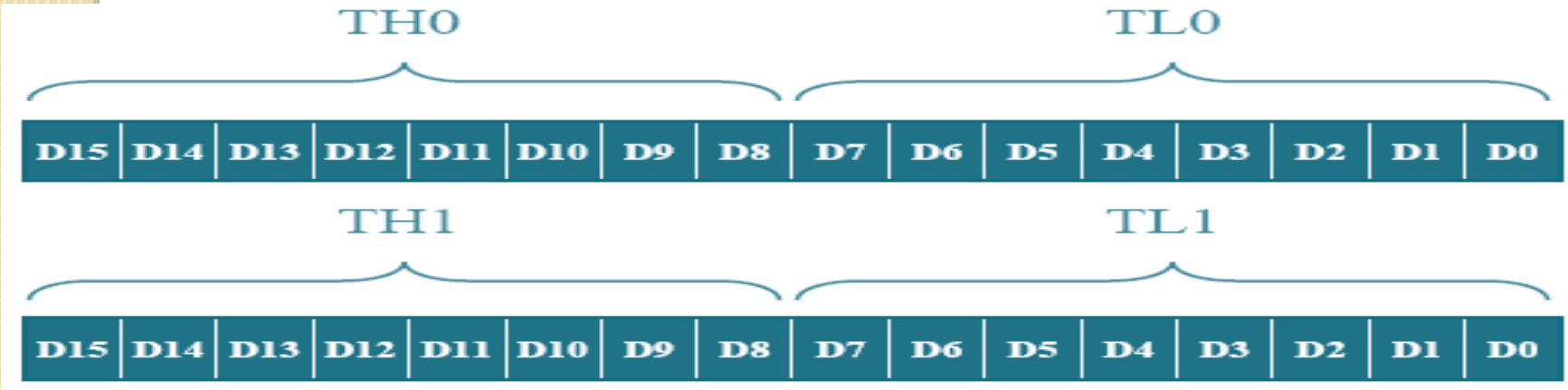
- TH0, TL0 : timer/counter register of timer 0
- TH1, TL1 : timer/counter register of timer 1

- Two Special function Registers TMOD and TCON are used to control the counter action of these counters by changing their bit status using certain instructions.

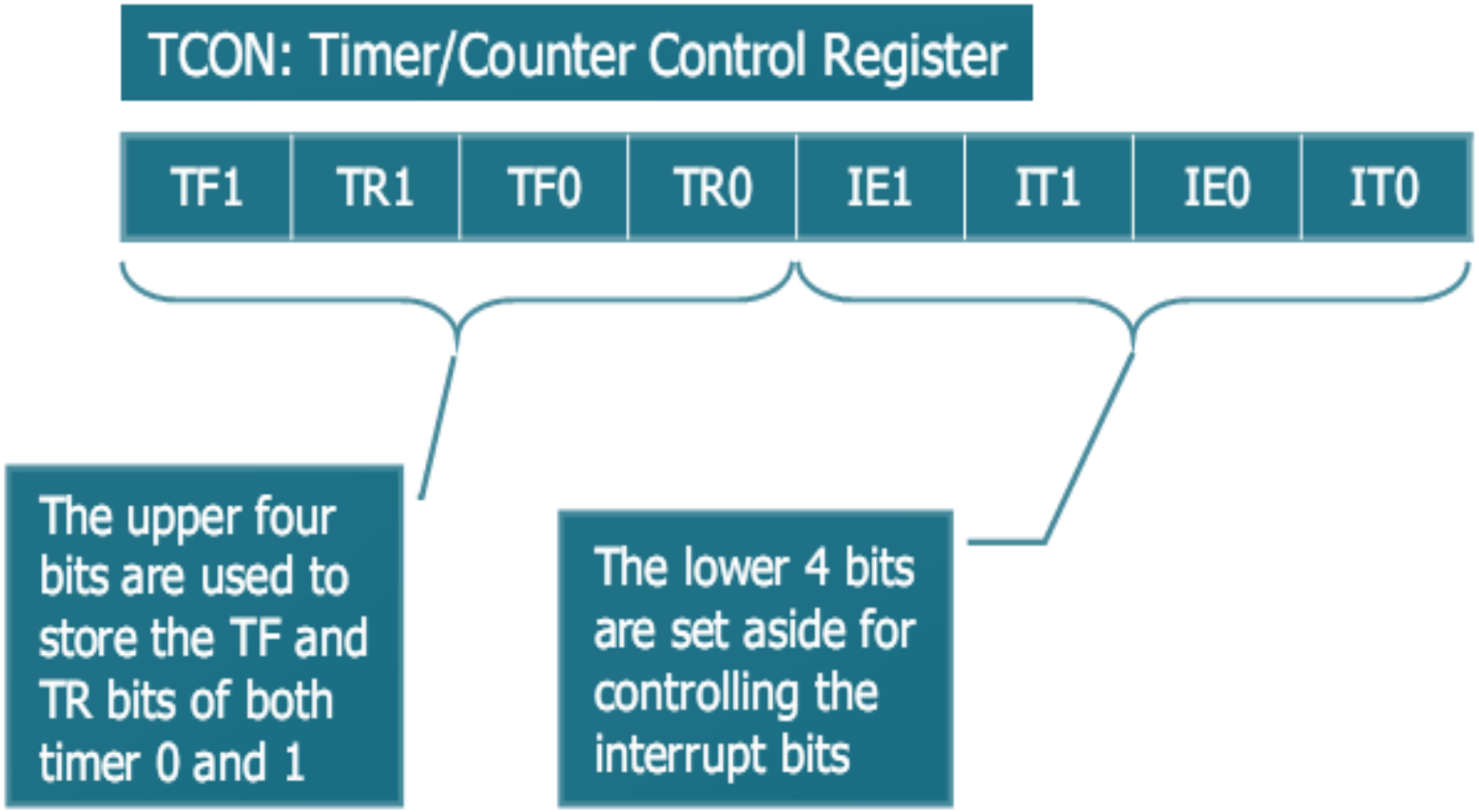
- TMOD : Mode Select register
- TCON : Control Register

Timer0 and Timer1 Registers

- Accessed as lower byte and higher byte
  - The lower byte register is TL0 / TL1
  - The higher byte register is TH0 / TH1
  - Accessed like any other register
    - MOV TL0, #4Fh :- this command moves the value 4Fh into the TL0 SFR.



TIMER CONTROL (TCON) register



- TCON register is also one of the registers whose bits are directly in control of timer operation.

- Only 4 bits of this register are used for this purpose, while rest of them is used for interrupt control. Bit addressable as TCON.0 to TCON.7.

Timer control and Flag bits

- **TR** (Timer run control bit)
  - TR0 for Timer/counter 0; TR1 for Timer/counter 1.
  - TR is set by programmer to turn timer/counter on/off.
- **TF** (Timer flag bit)
  - TF0 for timer/counter 0; TF1 for timer/counter 1.
  - TF is like a carry. Originally TF=0. When TH-TL rolls over from FFFFH to 0000, the 8051 sets TF to 1.

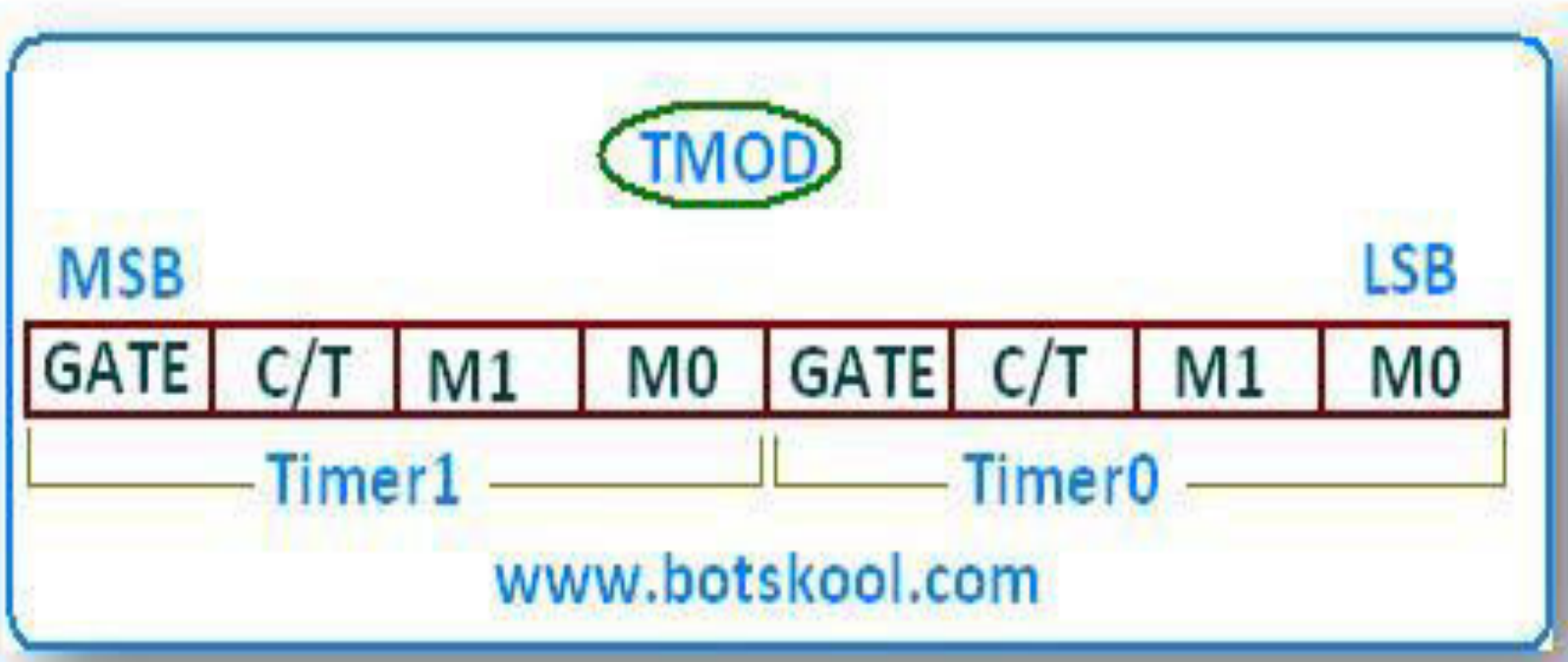
- TF1:- Timer1 Overflow flag. Set when timer rolls from all 1s to 0.Cleared when processor executes routine ISR.
- TR1:- Timer1 Run control bit. Set to 1 to enable timer to count; cleared to 0 by program to halt timer.
- TF0:- Timer0 Overflow Flag. Set when timer rolls from all 1s to 0.Cleared when processor executes routine ISR.
- IE1 :- External Interrupt 1 Edge flag . Set to 1 when a high to low edge signal is received on port 3 pin 3.3 (INT1). Not related to timer operations.

- IT0 :- External Interrupt 0 signal type control bit. Set to 1 by program to enable external interrupt 0 to be triggered by a falling edge signal. Set to 0 by program to enable a low level signal on external interrupt 0 to generate an interrupt.

- IE0 :- External Interrupt 0 Edge flag. Set to 1 when a high to low edge signal is received on port 3 pin 3.2 (INT0). Not related to timer operations.

- IT1 :- External Interrupt 1 signal type control bit. Set to 1 by program to enable external interrupt 1 to be triggered by a falling edge signal. Set to 0 by program to enable a low level signal on external interrupt 1 to generate a interrupt.

TIMER MODE CONTROL(TMOD) REGISTER

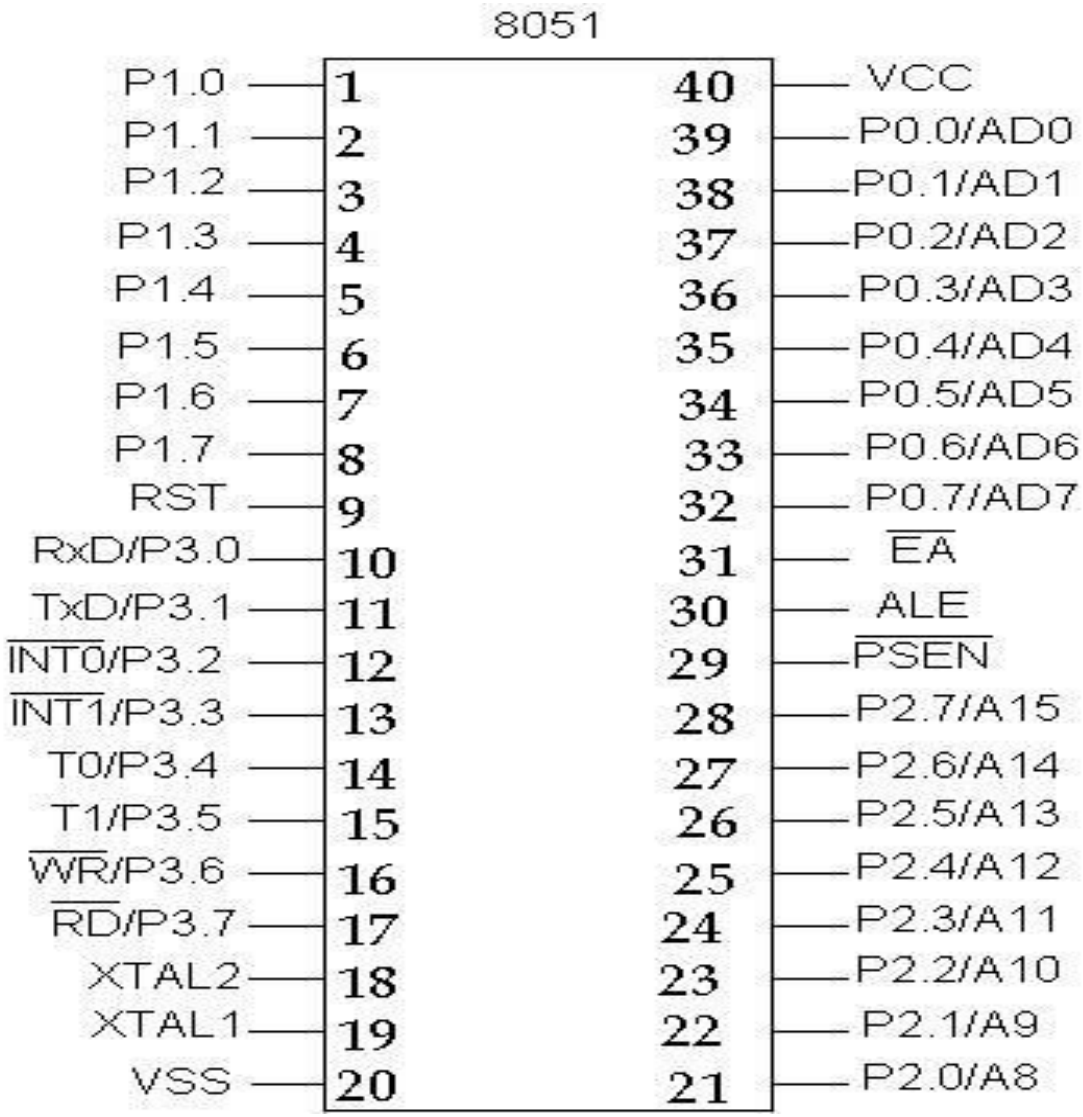


TMOD is not bit addressable.

Bit	Name	Function	Timer
7	GATE1	When this bit is set the timer will only run when INT1 (P3.3) is high. When this bit is clear the timer will run regardless of the state of INT1	1
6	C/T1	When this bit is set the timer will count events on T1 (P3.5). When this bit is clear the timer will be incremented every machine cycle	1
5	T1M1	Timer mode bit	1
4	T1M0	Timer mode bit	1
3	GATE0	When this bit is set the timer will only run when INT0 (P3.2) is high. When this bit is clear the timer will run regardless of the state of INT0	0
2	C/T0	When this bit is set the timer will count events on T0 (P3.4). When this bit is clear the timer will be incremented every machine cycle	0
1	T0M1	Timer mode bit	0
0	T0M0	Timer mode bit	0

M1	M0	MODE	DESCRIPTION
0	0	Mode 0	13 bit timer
0	1	Mode 1	16 bit timer
1	0	Mode 2	8 bit auto reload
1	1	Mode 3	Split timer

PIN DIAGRAM


8051
P1.0 1
P1.1 2
P1.2 3
P1.3 4
P1.4 5
P1.5 6
P1.6 7
P1.7 8
RST 9
RxD/P3.0 10
TxD/P3.1 11
INT0/P3.2 12
INT1/P3.3 13
T0/P3.4 14
T1/P3.5 15
WR/P3.6 16
RD/P3.7 17
XTAL2 18
XTAL1 19
VSS 20
40 VCC
39 P0.0/AD0
38 P0.1/AD1
37 P0.2/AD2
36 P0.3/AD3
35 P0.4/AD4
34 P0.5/AD5
33 P0.6/AD6
32 P0.7/AD7
31 EA
30 ALE
29 PSEN
28 P2.7/A15
27 P2.6/A14
26 P2.5/A13
25 P2.4/A12
24 P2.3/A11
23 P2.2/A10
22 P2.1/A9
21 P2.0/A8

BASIC PINS

- **PINS 1 TO 8 (P1.0 to P1.7) :** This is PORT 1 , it is 8-bit bi-directional I/O port. It is bit/byte addressable. When logic '1' is written into port latch then it works as input mode. It functions as simply I/O port and it does not have any alternative function.

- **PIN 9 (RST) :** PIN 9 is the reset pin which is used to reset the microcontroller's internal registers and ports upon starting up.

- **PIN 10 TO 17 (P3.0 to P3.7) :** This is PORT 3, these Pins are similar to Pins of Port 1. These Pins can be used as universal Input or output. These are dual function Pins.

- **PIN 10 (RxD/P3.0) :** It is an Input signal. Through this I/P signal microcontroller receives serial data of serial communication circuit.

- **PIN 11 (TxD/P3.1) :** It is O/P signal of serial port. Through this signal data is transmitted.

- **PINS 12 & 13 :** P3.2 & P3.3 i.e. INT0 & INT1 are external hardware interrupt I/P signals. Through this user, programmer or peripheral interrupts to microcontroller.

- **PINS 14 & 15 :** P3.4 & P3.5 i.e. (T0 & T1) are input signal to internal timer-0 and timer-1 circuit respectively. External clock pulses can connect to timer-0 and timer-1 through these I/P signals.

- **PIN 16 ($\overline{\text{WR}}$/P3.6) :** It is active low write O/P control signal. During External RAM (Data memory) access it is generated by microcontroller. when $\overline{\text{WR}}$=0 , then performs write operation.

- **PIN 17 ($\overline{\text{RD}}$/P3.7) :** It is active low read O/P control signal. During External RAM (Data memory) access it is generated by microcontroller when $\overline{\text{RD}}$=0 , then performs read operation from external RAM.

- **PINS 18 & 19 :** The 8051 has a built-in oscillator amplifier hence we need to only connect a crystal at these pins to provide clock pulses to the circuit.

- **PINS 21 TO 28 (P2.0 to P2.7) :** This is PORT 2 , it is 8-bit bi-directional I/O port. It is bit/byte addressable. During external memory access it functions as higher order address bus (A8-A15).

- **PINS 29, 30 & 31** : As described in the features of the 8051, this chip contains a built-in flash memory. In order to program this we need to supply a voltage of +12V at pin 31.

i) If external memory is connected then PIN 31, also called EA/VPP, should be connected to ground to indicate the presence of external memory.

ii) PIN 30 is called ALE (address latch enable), which is used when multiple memory chips are connected to the controller and only one of them needs to be selected.

iii) PIN 29 is called PSEN. This is "program store enable". In order to use the external memory it is required to provide the low voltage (0) on both PSEN and EA pins.

- **PINS 32 TO 39 (P0.0 to P0.7) :** This is Port 0 , it is 8-bit bi-directional I/O port. It is bit/ byte addressable. During external memory access, it functions as multiplexed data and low-order address bus AD0-AD7.

- **PINS 40 and 20** : Pins 40 and 20 are VCC and ground respectively. The 8051 chip needs +5V 500mA to function properly.