

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR (An Institution of National Importance under NITs Act, Established by Govt. of India) मालवीय राष्ट्रीय प्रौद्योगिकी संस्थान जयपुर

JLN	Marg,	Jaipur-302017	(India)
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Code: CST301	Computer Architecture	Credit: 03	
Couc. CS1301		L-T-P: (3-0-0)	
	Flynn Classification, Stack machines, subroutine calls, allocation		
Course Content	and evaluation of data in stack machines. SIMD, SPMD and MIMD.		
	CPU Organization: Addressing techniques, Instruction formats:		
	Instruction set design, Instruction types: example for zero address,		
	one address, two address and three address machines, Stack, accumulator and general purpose register organization. Register		
	Transfer Language: arithmetic, logic and shift micro operations and		
	their hardware implementations as a simple ALU. Control Unit,		
	Hardwired and Micro programmed control unit design.		
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	Memory Organization: device characteristics, RAM organization: 1D		
	and 2D organization, Virtual memory - Paging and Segmentation,		
	High speed memories: Associative and Cache memory.		
	Input-Output Design: IO interface, Bus structure, Modes of data		
	transfer, Interrupts, Input Output Processor, Serial Communication		
	Pipelining: Pipeline structure, Pipeline types - Instruction and		
	Arithmetic pipelines. Interleaved memory organization, instruction		
	prefetch, data buffers, pipeline performance measures. Array		
	processors: Routing mechanisms, Static v/s dynamic netwo Multiprocessor systems, data flow concepts. Parallel proces		
	languages.	Silig	
	1. J.L. Hennessy and D.A. Patterson, Computer Architectu	re: A Quantitative	
Important Text	Approach, 4th Edition Elsevier.	10. 11 Quantitudive	
Books/References	± ±		
	3. David Culler: Parallel Computer Architecture: A Hardware/Software		
	Approach, Morgan Kaufmann.		
	4. Hwang and Briggs: Computer Architecture and Parallel	Processing,	
	McGraw-Hill.		