INDIAN INSTITUTE OF TECHNOLOGY PATNA

Logic-sim CS226- Lab 11

Q1: Design an FSM that produces output (*P _odd)* one if successive samples of input (1 bit input *X)* have an odd number of 1s.

(a) Implement and simulate using D flip flop and basic logic gates
(b) Implement and simulate using JK flip flop and basic logic gates
(c) Implement and simulate using T flip flop and basic logic gates
(d) Implement and simulate using R-S flip flop and basic logic gates

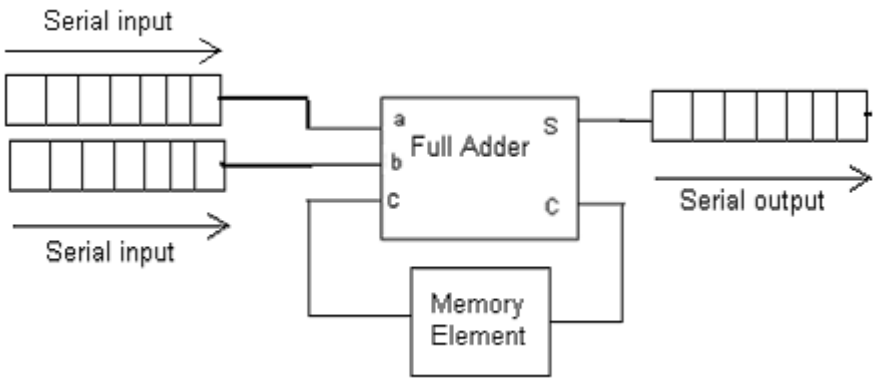
(20 points)

Q2: Design a 2-bit counter with following behavior
C0C1: 00 Stop counting
C0C1: 01 count up
C0C1:10 Count down
C0C2:11 : count by 2.
(C0 & C1 are the control inputs)

(20 points)

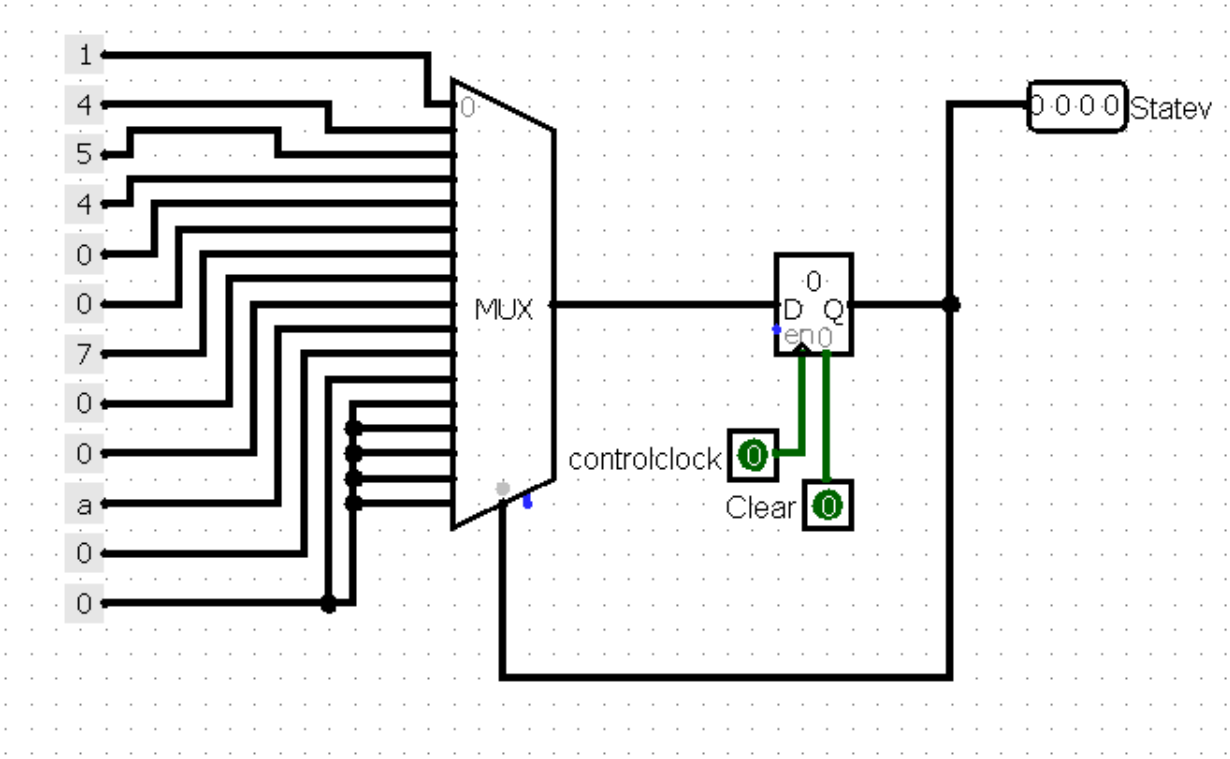
I. Implement and simulate using D flip flops and basic logic gates
II. Implement and simulate using JK flip flops and basic logic gates

Q3: Design and simulate an 8 bit serial adder using single full adder. Using D flip flop as the memory element. Assume parallel in- serial out shift register at the input.



(20 points)

Q4: Simulate the behavior of the circuit below



(10 points)

(Q5) Design a counter that counts in the following sequence: 000, 010, 111, 100, 110, 011, 001, and repeat.

I. Implement and simulate using D flip flops and basic logic gates

II. Implement and simulate using JK flip flops and basic logic gates

(10 points)

(Q6) Repeat the problem Q2 for 3 bit counter. Design using D flip flops and basic gates.

(20 points)

Submit Report with hand written solutions with schematic for the problems Q1 and Q2 (by end of the class). Show the simulations to TAs. Submit your .circ file containing your various transistor-level/logic level implementations

- The simulation files p1.circ, p2.circ, p3.circ, p4.circ, p5.circ and p6.circ
- Zip the above five files. Zip file name is your role number.

Course work submission through Email: cs225.iitp@gmail.com
(use email subject Lab11_Logicsim_your roll number).
This work is due on: : April 01, 2019