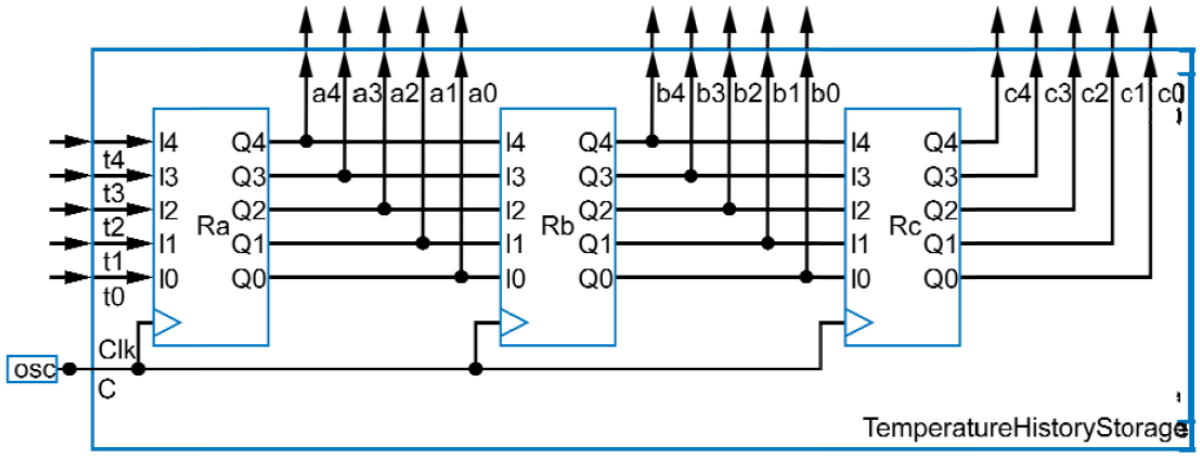
INDIAN INSTITUTE OF TECHNOLOGY PATNA
CS226- Switching Theory Lab

Lab 10

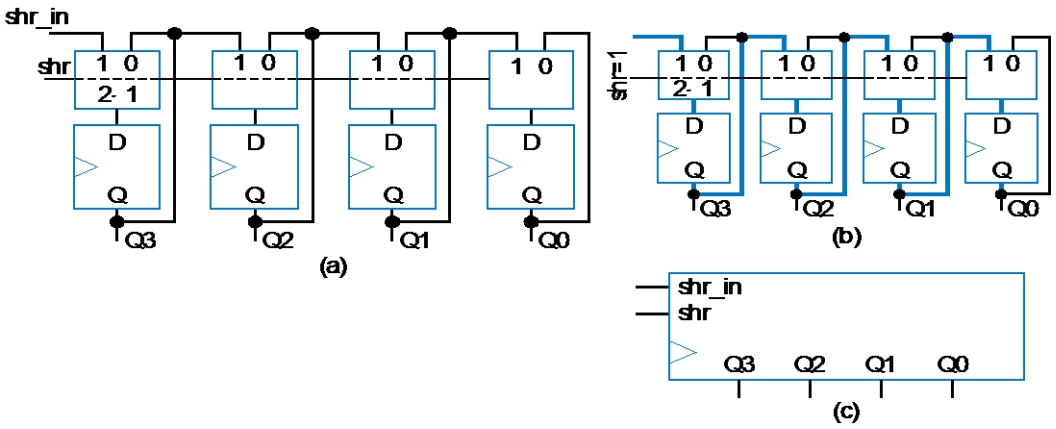
Register file design (Logic-Sim)

Q1:
Using standard build in sequential elements build a 5 bit parallel in parallel out register.
Implement the following the temperature History Storage.



Q2: Design 4 bit register to either shift or retain, use 2x1 muxes

- shr: 0 means retain, 1 shift
- shr_in: value to shift in



Q3: Study the given register file-32x32 (with two read port and one write port). Test it using appropriate test environment.

Q4: Re-design a new register file -16x16 (with two read port and one write port.

Q5: Using Q4 design , read two 16 bit numbers from the register file and add them using an adder block and write back to the result to a new register.

Submission:

Submit your .circ file containing your various implementations. Show the simulations to TAs.

- The simulation files p1.circ, p2.circ, p3.circ, and p4.circ
- Zip the above five files. Zip file name is your role number.

Course work submission through Email: cs225.iitp@gmail.com
(use email subject Lab10_Logicsim_your roll number).
This work is due on: : 25h March 2019