J-K positive latch and J-K negative edge-triggered Flip-Flop
EE210P - Digital System Design

***Abstract*—This report demonstrates the operation of J-K positive latch and J-K negative edge-triggered Flip-Flop . Verilog language, which is a Hardware Descriptive Language (HDL), is used to describe the low level hardware, on Xilinx Vivado.**

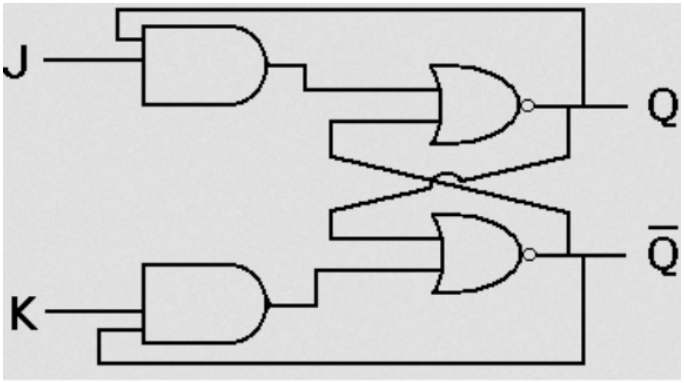
I. Introduction

A. Latch and Flip-Flop

Latches are basic storage elements that operate with signal levels (rather than signal transitions). Latches controlled by a clock transition are flip-flops. eg- SR Latch.
Flip flop is an extended version of latch by integrating it with a clock. A clock pulse is a time varying voltage signal applied to control the operation (triggering) of a flip flop. eg- JK Flip Flop, D Flip Flop.

B. J K Latch

JK latch is an electronic devise that is mostly is similar to RS latch. This latch consists of 2 inputs J and K as shown in the below figure. The ambiguous state has been eliminated here: when the inputs of Jk latch are high, then output toggles. The output feedback to inputs is the only difference we see here, which is not there in the RS latch. The circuit diagram is displayed here -

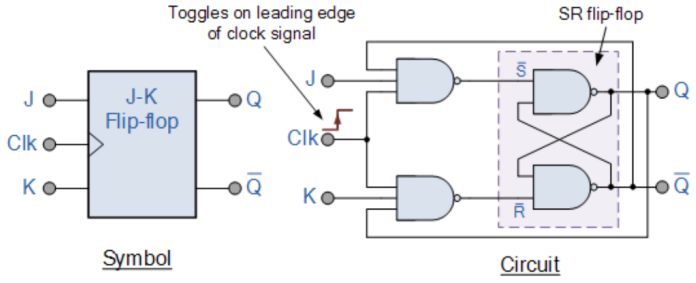


The truth table is displayed bellow -

J_n	K_n	Q_n	$\overline{Q_n}$	Q_{n+1}	Action
0	0	0	1	0	$= Q_n$ = No change
0	0	1	0	1	
0	1	0	1	0	= 0 = Reset
0	1	1	0	0	
1	0	0	1	1	= 1 = Set
1	0	1	0	1	
1	1	0	1	1	$= \overline{Q_n}$ = Toggle
1	1	1	0	0	

C. J K Flip Flop

This simple JK flip Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The two inputs labelled “J” and “K” are not shortened abbreviated letters of other words, such as “S” for Set and “R” for Reset, but are themselves autonomous letters chosen by its inventor Jack Kilby to distinguish the flip-flop design from other types.



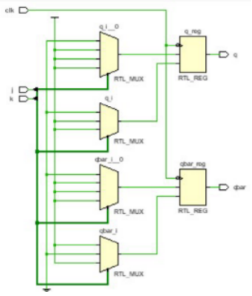
The truth table is displayed bellow -

	Clock	Input		Output		Description
	Clk	J	K	Q	$\overline{Q}$	
same as for the SR Latch	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	¯_	0	1	1	0	Reset Q » 0
	X	0	1	0	1	
	¯_	1	0	0	1	Set Q » 1
	X	1	0	1	0	
toggle action	¯_	1	1	0	1	Toggle
	¯_	1	1	1	0	

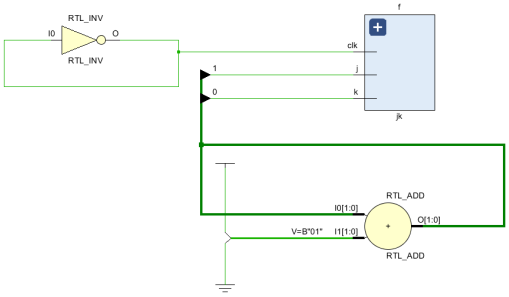
II. SYNTHESIS AND SIMULATIONS

REFERENCES

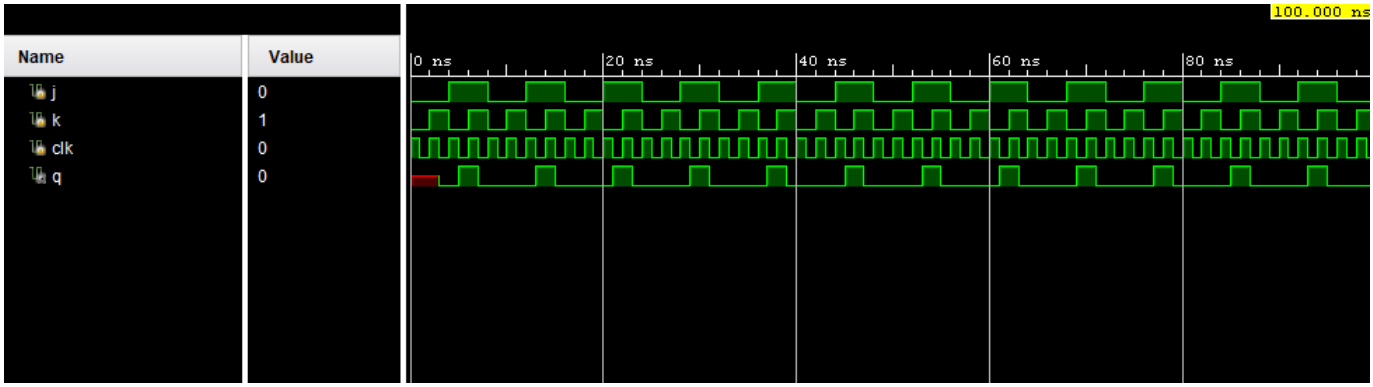
[1] Schematic Diagram of J-K positive Latch



[2] Schematic Diagram of J-K negative edge-triggered Flip-Flop



[3] Test Bench Waveform



[4] Design Source Code

```
1   `timescale 1ns / 1ps
2   module jk(j,k,q,clk);
3   input j,k,clk;
4   output reg q;
5   always @(negedge clk)
6   case({j,k})
7   2'b00: q<=q;
8   2'b01: q<=0;
9   2'b10: q<=1;
10  2'b11: q<=~q;
11  endcase
12  endmodule
13
```

[5] Test Bench Code

```
1   `timescale 1ns / 1ps
2   module test();
3   reg j,k,clk;
4   wire q;
5   jk f(.j(j),.k(k),.q(q),.clk(clk));
6   initial begin
7   j=0;
8   k=0;
9   clk=1;
10  end
11  always #1 clk=~clk;
12  always #2 {j,k}={j,k}+1'b1;
13  initial #100 $finish;
14  endmodule
15
```

III. CONCLUSION

We verify the principles and working mechanism of J K positive Latch and adding clock to it purpose the same for J K negative edge-triggered Flip-Flop

REFERENCES

[1] Digital Design by Morris Mano