Parallel-In-Parallel-Out D-FF
EE210P - Digital System Design

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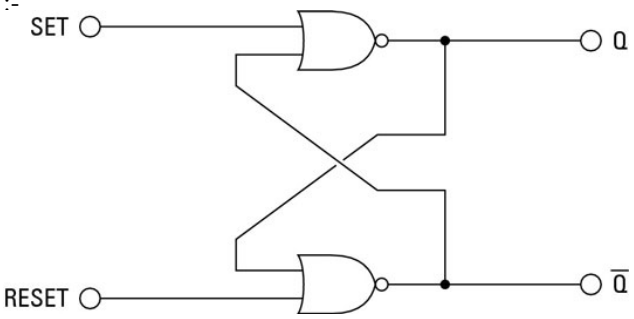
***Abstract*—This report demonstrates the operation of Parallel-In-Parallel-Out (PIPO) Register using multiplexer-based negative edge D - Flip Flop (D-FF) . Verilog language, which is a Hardware Descriptive Language (HDL), is used to describe the low level hardware, on Xilinx Vivado.**

I. Introduction

A shift register is one type of sequential logic circuit where its output mainly depends on its input previous output. This register includes a set of Flip Flops (FF) where these are connected within cascade which means, one FF output is simply connected to the input of another FF. This register is used to store as well as shift the group of binary data. The number of FFs available within the shift register mainly depends on the no. of binary bits stored within the register. For instance; here had stored 4-bits of binary data, hence four flip-flops are being used. Let come to it's different modules one by one.

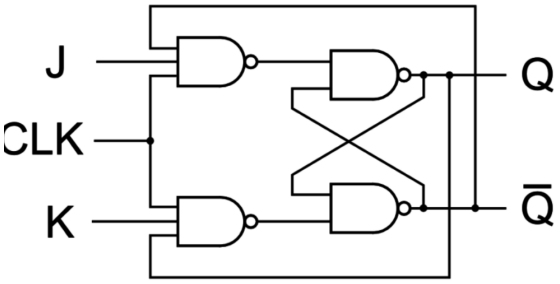
A. Latch

A Latch is a special type of logical circuit. The latches have low and high two stable states. Due to these states, latches also refer to as bistable-multivibrators. A latch is a storage device that holds the data using the feedback lane. The latch stores 1 -bit until the device set to 1. The latch changes the stored data and constantly trials the inputs when the enable input set to 1. eg- SR Latch, D latch. An example is displayed bellow :-



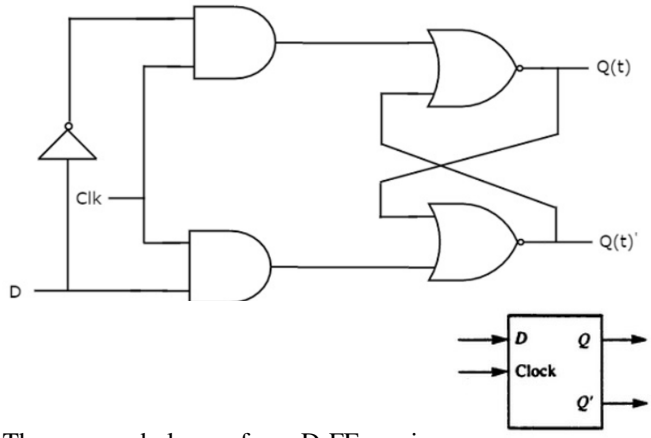
B. Flip Flop

Flip flop is an extended version of latch by integrating it with a clock. A clock pulse is a time varying voltage signal applied to control the operation (triggering) of a flip flop. For example, if a clock pulse is of frequency 1 Hz, the voltage it will supply will oscillate between X Volts and Y Volts(X and Y are any dc voltages), and this change occurs every half second. say it is 0 V in the first half second then it will be +5V in the next half second and the cycle continues. eg- JK Flip Flop, D Flip Flop. An example is displayed bellow :-



C. D - Flip Flop

The D flip-flop (D-FF) is a two-input flip-flop. The inputs are the data (D) input and a clock (CLK) input. The clock is a timing pulse generated by the equipment to control operations. The D flip-flop is used to store data at a predetermined time and hold it until it is needed. This circuit is sometimes called a delay flip-flop. The circuit is displayed bellow :-



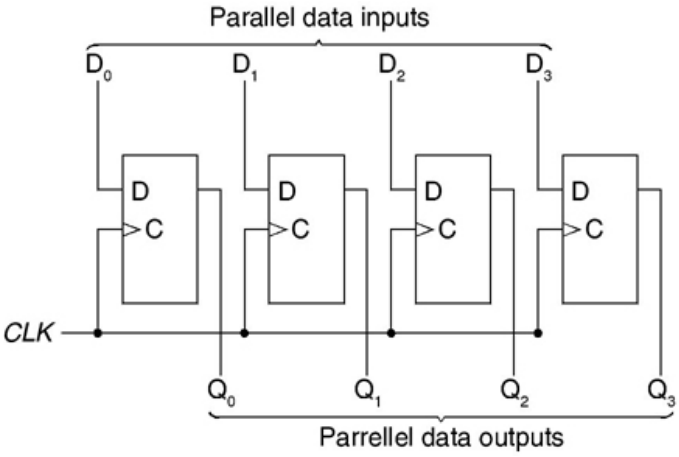
The symbol of D-FF is

Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

D. Parallel-In-Parallel-Out Register

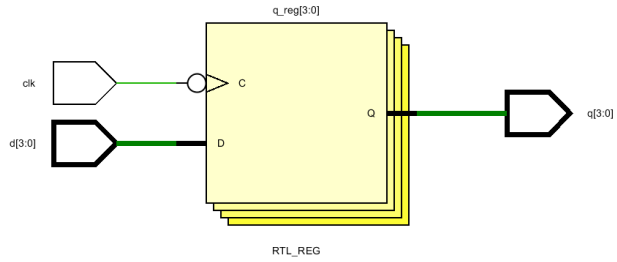
Registers are data storage devices that are more sophisticated than latches. A register is a group of binary cells suitable for holding binary information. A group of cascaded flip-flops used to store related bits of information is known as a register. Latch and Flip-Flops comes under it. eg - SR Register, T flip-flops. Parallel-In-Parallel-Out Register (PIPO) shift register which is also known as parallel in the parallel-out shift register as individual inputs are generating it's own individual output and a clock is connected to make combinations of parallel circuits(or we can say inputs and outputs are parallel and that unit is independent). The circuit is displayed bellow :-



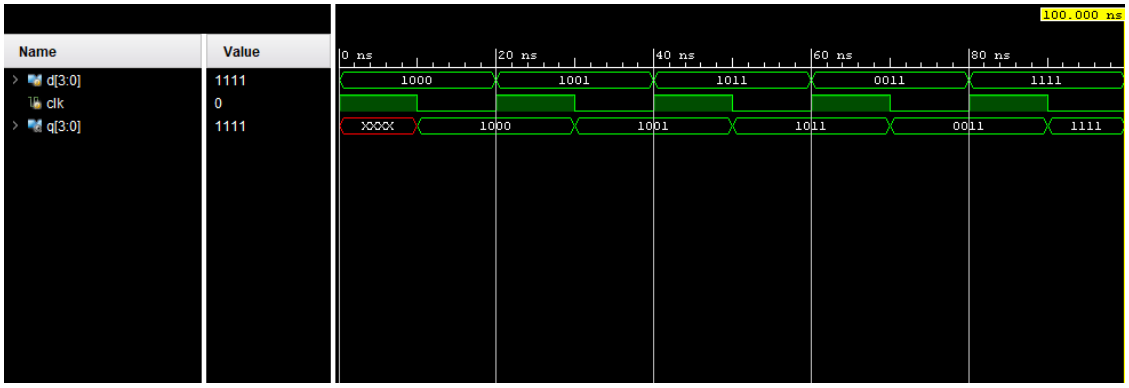
II. SYNTHESIS AND SIMULATIONS

REFERENCES

[1] Schematic Diagram of 4-bit Parallel-In-Parallel-Out (PIPO) Register



[2] Test Bench Waveform



[3] Design Source Code

```
1   `timescale 1ns / 1ps
2   module pipo(d,clk,q);
3   input clk;
4   input [3:0] d;
5   output reg [3:0] q;
6   always @(negedge clk)
7   q=d;
8   endmodule
9
```

[4] Test Bench Code

```
1   `timescale 1ns / 1ps
2
3   module test;
4   reg [3:0] d;
5   reg clk;
6   wire [3:0] q;
7   pipo ptc(d,clk,q);
8   initial
9   begin
10  clk=1;d=4'b1000;
11  #1 0
12  clk=0;d=4'b1000;
13  #10
14  clk=1;d=4'b1001;
15  #10
16  clk=0;d=4'b1001;
17  #10
18  clk=1;d=4'b1011;
19  #10
20  clk=0;d=4'b1011;
21  #10
22  clk=1;d=4'b0011;
23  #10
24  clk=0;d=4'b0011;
25  #10
26  clk=1;d=4'b1111;
27  #10
28  clk=0;d=4'b1111;
29  #10
30  $stop;
31  end
32  endmodule
33
```

III. CONCLUSION

We can make N-bit Parallel-In-Parallel-Out (PIPO) Register using multiplexer-based negative edge using some combinations of D Flip Flop (D-FF) and a clock.

REFERENCES

[1] Digital Design by Morris Mano