Low Power Design –
An Emerging Discipline

Historical figure of merit for VLSI design –performance (circuit speed) and chip area (circuit density/cost)

Power dissipation is now an important metric in VLSI design

- No single major source for power savings across all design levels – Required a new way of THINKING!!!
  Companies lack the basic power-conscious culture and designers need to be educated in this respect
- Overall Goal – To reduce power dissipations but
  maintaining adequate throughput rate

Need for Low Power VLSI Chips

Power dissipation was neglected due to
– Low device density
– Low operating frequency
• Now it is important issue due to
– High device density
– High operating frequency
– Proliferation of portable consumer electronics
– Concerns on Environments and energy sources

Competitive Reasons – Low Power

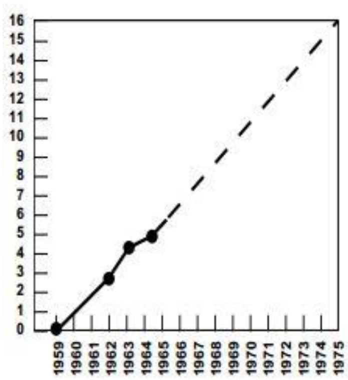
• Battery Powered Systems – Extended Battery Life and reduce weight and size.
• High-Performance Systems
– Cost
• Package (chip carrier, heat sink, card slots, plenum,)

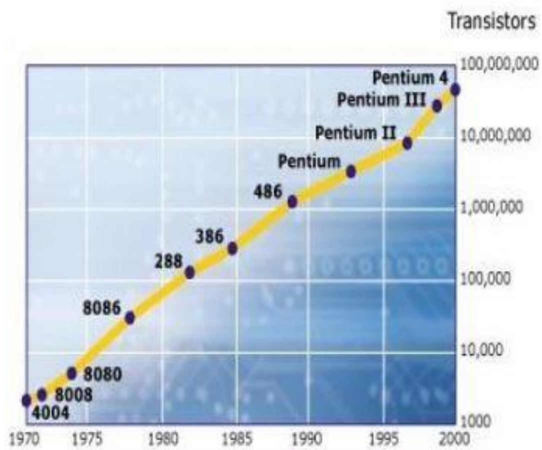
• Power Systems (supplies, distribution, regulators, …)
• Fans (noise, power, reliability, area, …)
• Operating cost to customer – Energy Star issue.
– Reliability
• Failure rate increase by 4X for *Tj* @ 110C vs 70C
• Mission critical operation at 100C
– Size and Weight – Product footprint (office and desk space.

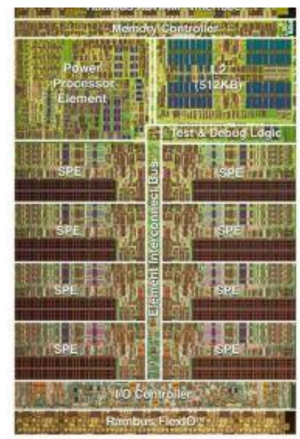
Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

- He made a prediction that semiconductor technology will double its effectiveness every 18 months







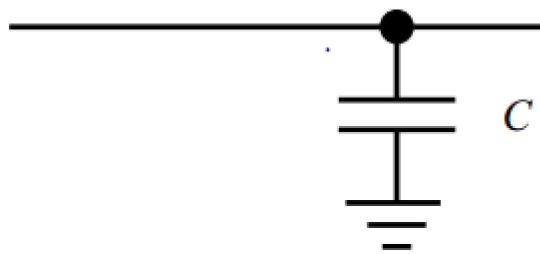
234M transistors in

Unit 3: Probabilistic Power Analysis Methods

Basic Idea

- View signals as a random processes

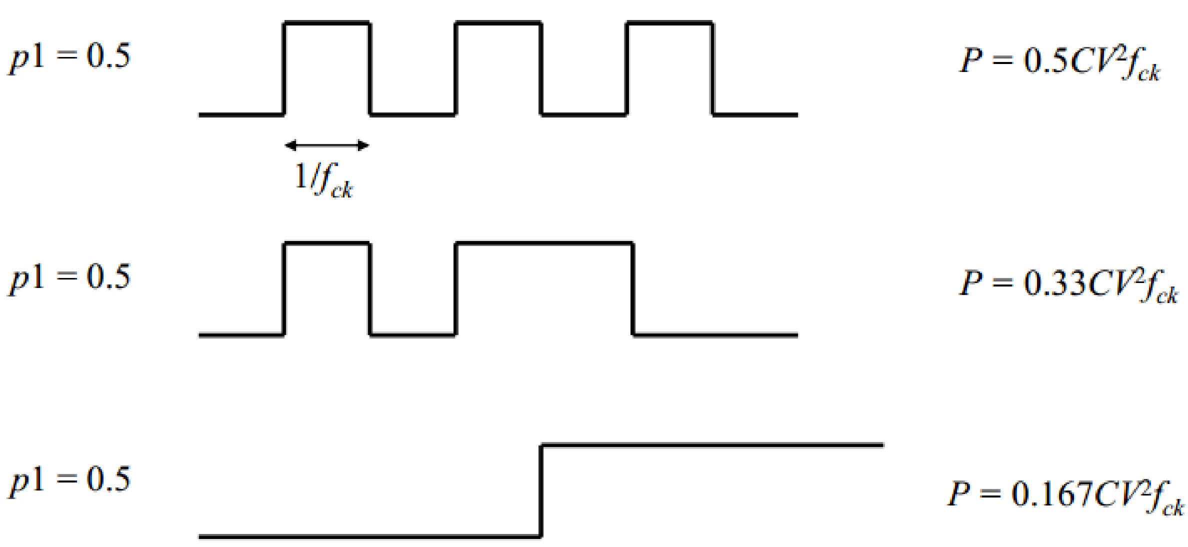
- Prob{s(t) = 1} = p1
  p0 = 1 – p1



0→1 transition probability = (1 – p1) p1

Power, P = (1 – p1) p1 CV2fck

Source of Inaccuracy



Observe that the formula, Power, P = (1 – p1) p1 CV2fck, is not correct

Switching Frequency

Number of transitions per unit time:

$$T = \frac{N(t)}{t}$$

For a continuous signal:

$$T = \lim_{t \to \infty} \frac{N(t)}{t}$$

T: is defined as the transition density

Static Signal Probabilities

Observe signal for interval t0 + t1

– Signal is 1 for duration t1

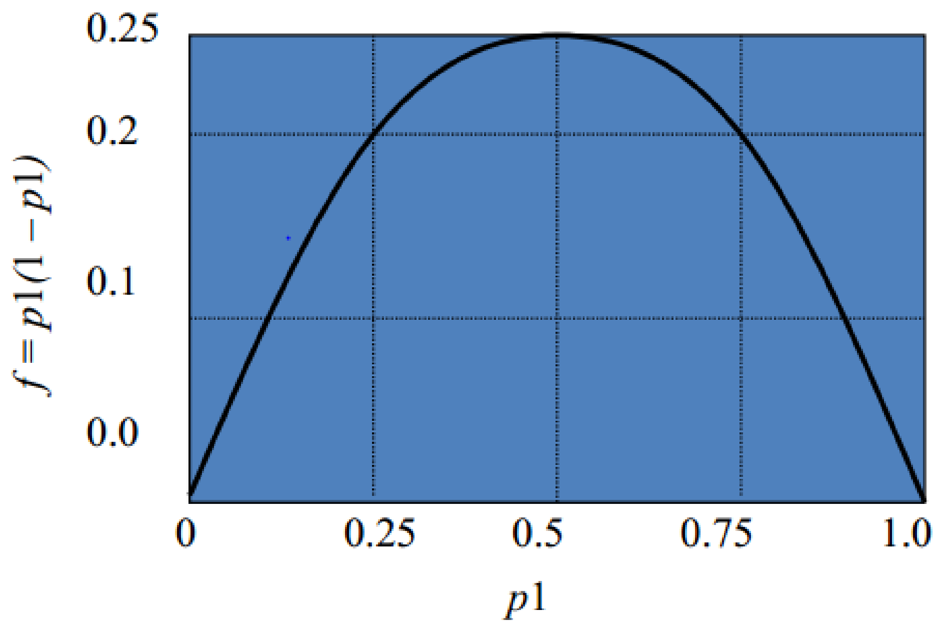
– Signal is 0 for duration t0
– Signal probabilities:
• $p1 = t1/(t0 + t1)$
• $p0 = t0/(t0 + t1) = 1 – p1$

Static Transition Probabilities

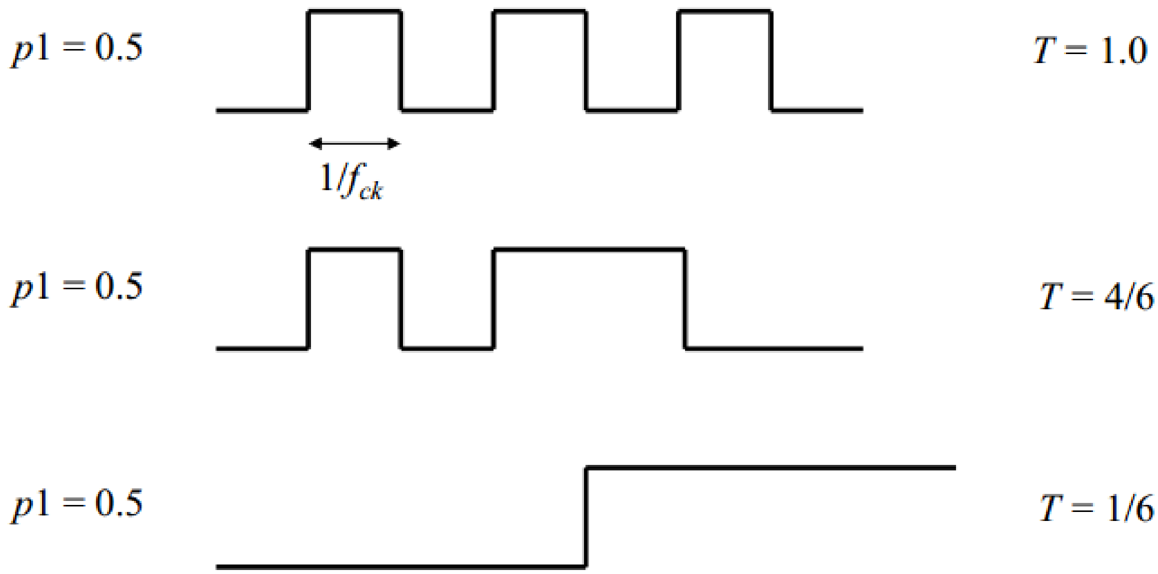
• Transition probabilities:
• $T01 = p0$ Prob{signal is 1 | signal was 0} $= p0\ p1$
• $T10 = p1$ Prob{signal is 0 | signal was 1} $= p1\ p0$
• $T = T01 + T10 = 2\ p0\ p1 = 2\ p1\ (1 – p1)$

• Transition density: $T = 2\ p1\ (1 – p1)$
• Transition frequency: $f = T/ 2$
• Power = $CV2T/ 2$ (correct formula)

Static Transition Frequency



Inaccuracy in Transition Density



Observe that the formula, $T = 2\,p1\,(1 - p1)$, is not correct.

Cause for Error and Correction

- Probability of transition is not independent of the present state of the signal
- Consider probability $p01$of a $0 \rightarrow 1$ transition,
- Then $p01 \neq p0\ p1$
- We can write $p1 = (1 - p1)p01 + p1\ p11$

$$p1 = \frac{p01}{1 - p11 + p01}$$

Correction (Cont.)

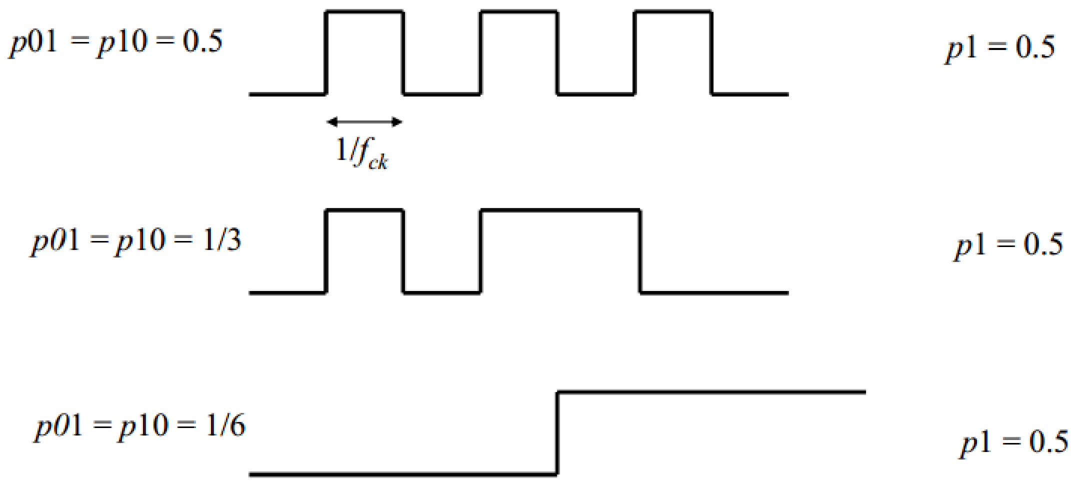
- Since p11 + p10 = 1, i.e., given that the signal was previously 1, its resent value can be either 1 or 0,

Therefore,

$$p1 = \frac{p01}{p10 + p01}$$

This uniquely gives signal probability as a function of transition probabilities.

Transition and Signal probabilities



Probabilities: p0, p1, p00, p01, p10, p11

- $p01 + p00 = 1$
- $p11 + p10 = 1$
- $p0 = 1 - p1$

$$p1 = \frac{p01}{p10 + p01}$$

Transition Density

- $T = 2p_1(1 - p_1) = p_0 p_{01} + p_1 p_{10}$

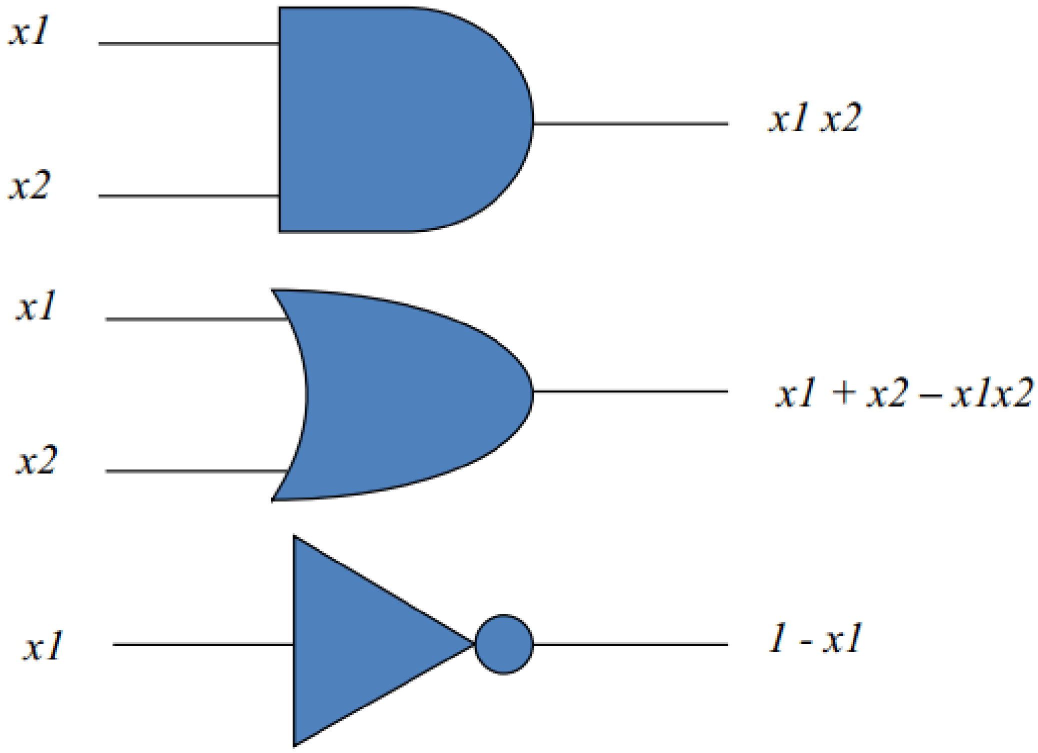
$= 2 p_{10} p_{01} / (p_{10} + p_{01})$

$= 2 p_1 p_{10} = 2 p_0 p_{01}$

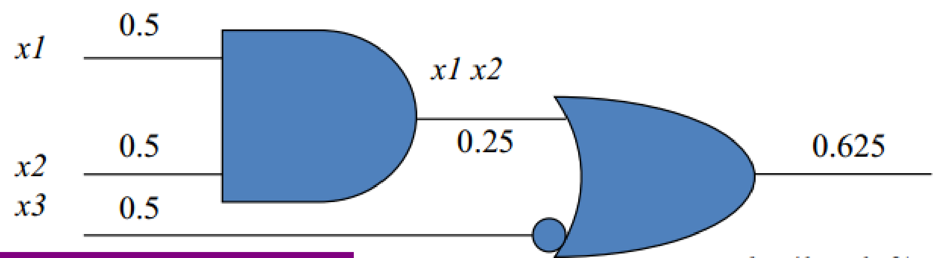
Power Calculation

- Power can be estimated if transition density is known for all signals.
- Calculation of transition density requires
  – Signal probabilities
  – Transition densities for primary inputs; computed from vector statistics

Signal Probabilities


x1
x2
x1 x2
x1
x2
x1 + x2 – x1x2
x1
1 - x1

Signal Probabilities

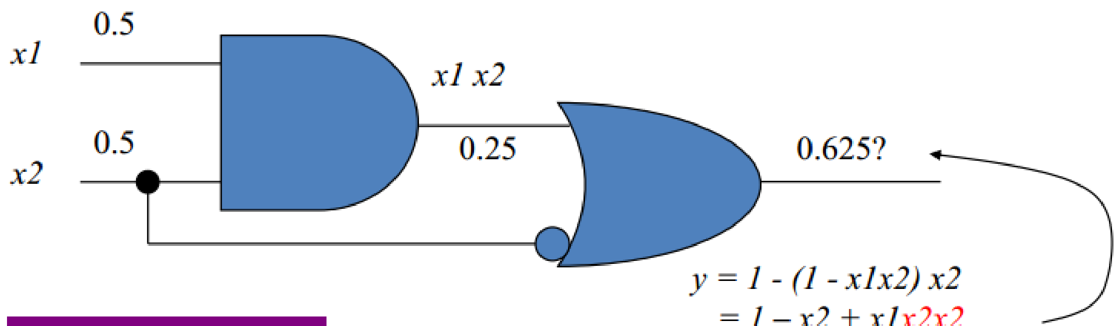


X1	*X2*	*X3*	*Y*
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$$
\begin{aligned}
y &= 1 - (1 - x1x2)\, x3 \\
&= 1 - x3 + x1x2x3 \\
&= 0.625
\end{aligned}
$$

***Ref:* K. P. Parker and E. J. McCluskey, "Probabilistic Treatment of General**

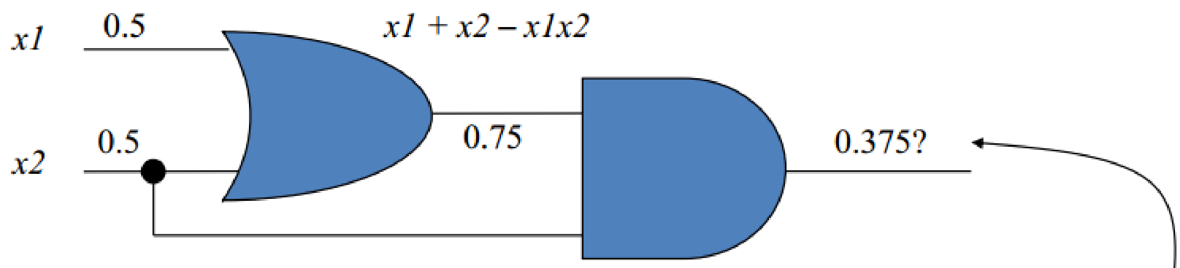
Correlated Signal Probabilities



$$
\begin{aligned}
y &= 1 - (1 - x1x2)\,x2 \\
&= 1 - x2 + x1\,x2x2 \\
&= 1 - x2 + x1x2 \\
&= 0.75
\end{aligned}
$$

X1	*X2*	*Y*
0	0	1
0	1	0
1	0	1
1	1	1

Correlated Signal Probabilities



$$\begin{aligned} y &= (x1 + x2 - x1x2)\, x2 \\ &= x1x2 + x2x2 - x1x2x2 \\ &= x1x2 + x2 - x1x2 \\ &= x2 \\ &= 0.5 \end{aligned}$$

X1	*X2*	*Y*
0	0	0
0	1	1
1	0	0
1	1	1

Observation

- Numerical computation of signal probabilities is accurate for fan out-free circuits.

Remedies

- Use Shannon's expansion theorem to compute signal probabilities.
- Use Boolean difference formula to compute transition densities.

Shannon's Expansion Theorem

- C. E. Shannon, "A Symbolic Analysis of Relay and Switching Circuits," *Trans. AIEE*, vol. 57, pp. 713-723, 1938.

- Consider: Boolean variables, X1, X2, . . . , Xn
- Boolean function, F(X1, X2, . . . , Xn)

- Then F = Xi F(Xi=1) + Xi' F(Xi=0)

- Where
- Xi' is complement of X1
- Cofactors, F(Xi=j) = F(X1, X2, . . , Xi=j, . . , Xn), j = 0 or 1

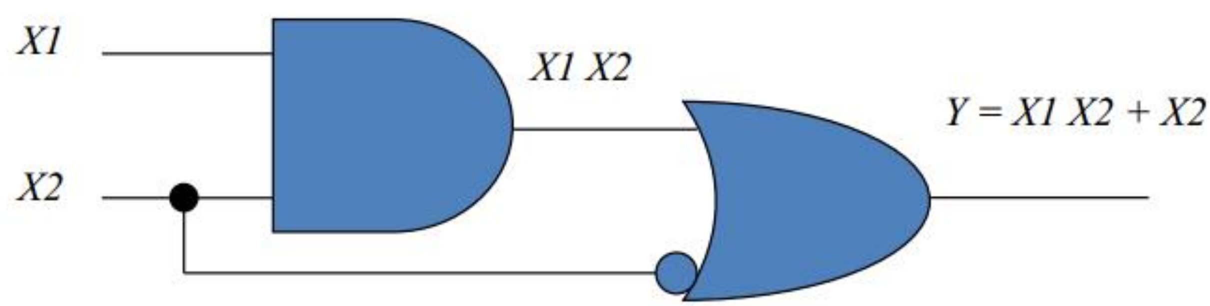
Expansion about Two Inputs

- F = XiXj F(Xi=1, Xj=1) + XiXj' F(Xi=1, Xj=0)+ Xi'Xj F(Xi=0, Xj=1) + Xi'Xj' F(Xi=0, Xj=0)

• In general, a Boolean function can be expanded about any number of input variables.

• Expansion about k variables will have 2k terms.

Correlated Signal Probabilities



X1	X2	Y
0	0	1
0	1	0
1	0	1
1	1	1

Shannon expansion about the reconverging input:

Y = X2 Y(X2=1) + X2’ Y(X2=0)
= X2 (X1) + X2’ (1)

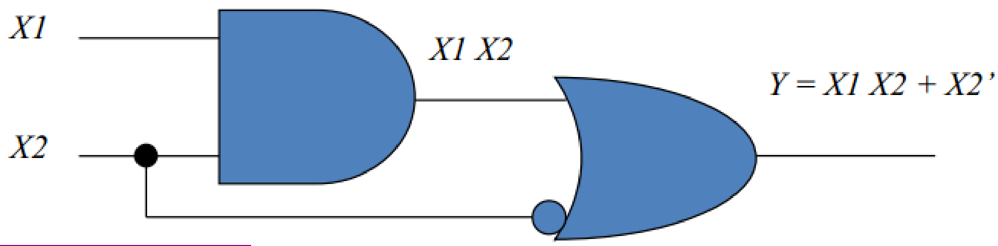
Correlated Signals

- When the output function is expanded about all reconverting input variables,
- All cofactors correspond to fan out-free circuits.
- Signal probabilities for cofactor outputs can be calculated without error.
- A weighted sum of cofactor probabilities gives the correct probability of the output.

- For two reconverging inputs:

$$f = x_i x_j f(X_i=1, X_j=1) + x_i(1-x_j) f(X_i=1, X_j=0) + (1-x_i)x_j f(X_i=0, X_j=1) + (1-x_i)(1-x_j) f(X_i=0, X_j=0)$$

Correlated Signal Probabilities



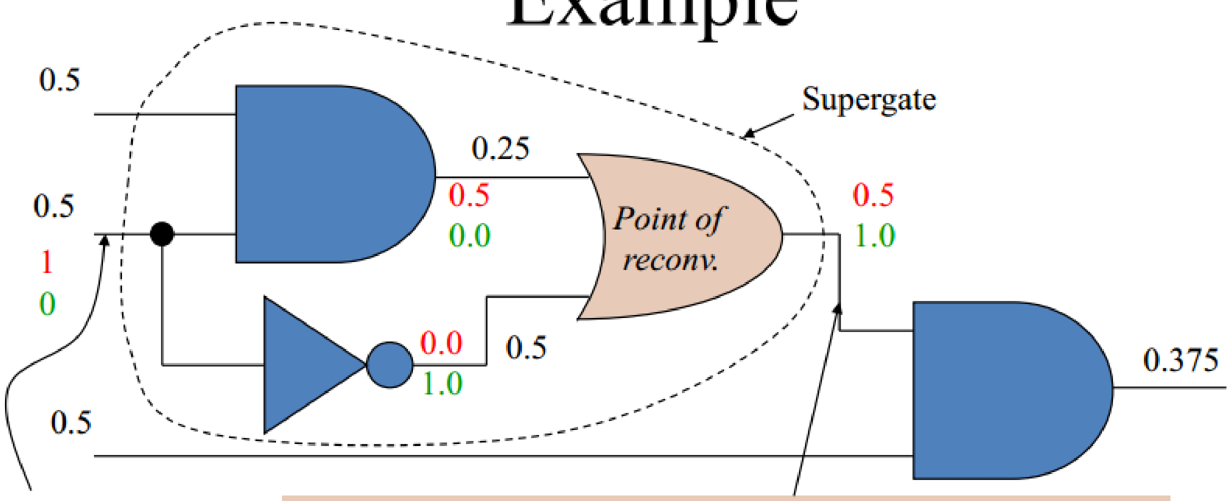
X1	X2	Y
0	0	1
0	1	0
1	0	1
1	1	1

Shannon expansion about the reconverging input:

$$Y = X2\ Y(X2{=}1) + X2'\ Y(X2{=}0)$$
$$= X2\ (X1) + X2'\ (1)$$

$$y = x2\ (0.5) + (1-x2)\ (1)$$
$$= 0.5\ (0.5) + (1-0.5)\ (1)$$
$$= 0.75$$

Example

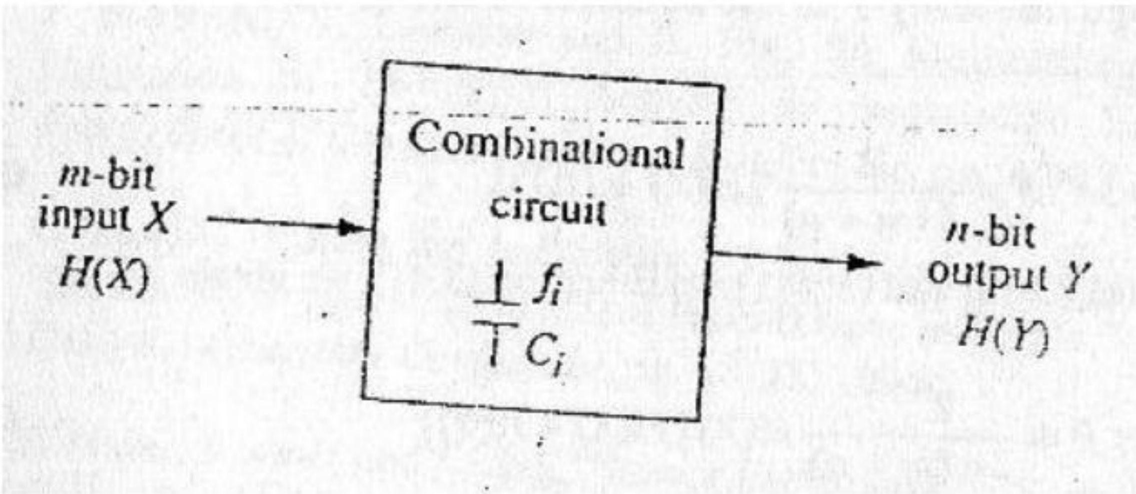


Signal probability for supergate output
= 0.5 Prob{rec. signal = 1} + 1.0 Prob{rec. signal = 0}
= 0.5 × 0.5 + 1.0 × 0.5 = 0.75

Signal entropy

- The entropy of a set of logic signals is a measure of its randomness
- Entropy correlates to the average switching frequency of the signals
- Skewed occurrence probability gives a low probability measure
- If signal switching is active, it maximizes the entropy of the signals
- These observations prompts the idea of using signal entropy for power estimation.

Power estimation of combinational logic using entropy analysis



Combinational circuit
$\perp f_i$
$\top C_i$
m-bit input X
H(X)
n-bit output Y
H(Y)

Entropy

- Entropy based approach
  - Entropy: Measure of uncertainty in a random va
  - Entropy H of a random variable x is given by

$$H(x) = p\log\frac{1}{p} + (1-p)\log\frac{1}{1-p}$$

    - p: probability of x being 1

- Recall that

$$P_{avg} \propto D_{avg}.GE.C_{avg}$$

  - D_{avg}: Average node switching activity
  - GE: Gate equivalents
  - C_{avg}: Average gate capacitance

- Hypothesis
  - Can D_{avg} be estimated only from knowledge of inputs and output behavior?

- Answer: Yes!

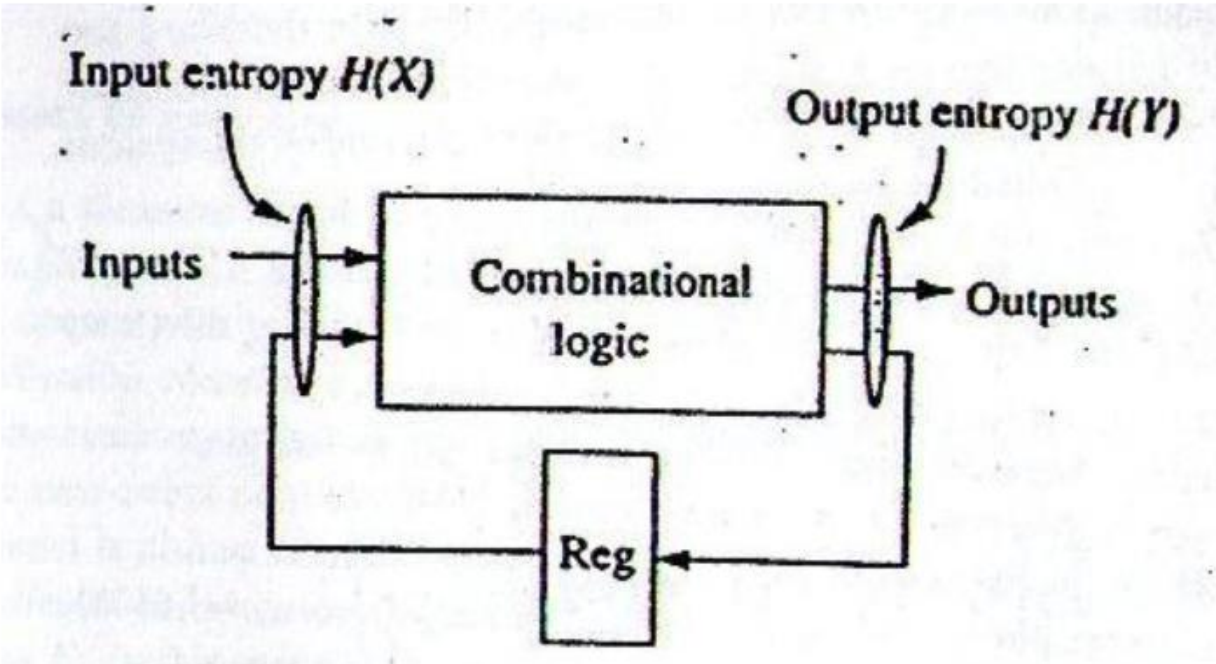
$$P_{avg} \propto H.GE.C_{avg}$$

- Entropy H is given by

$$H \approx \frac{2/3}{n+m}(H(X)+H(Y))$$

- H(X) and H(Y) are respectively the input and output entropies

Entropy analysis of a sequential circuit



Entropy

- Entropy Based Power Estimation

Methodology:

– Run a structural RTL simulation to measure input/output entropies

– Using input/output entropies, estimate Pavg for the combinational block

– Use other techniques to estimate latch and clock power