Low Power VLSI Design

↳ need for low power VLSI chips

VLSI Chip types
→ semi custom
→ Full custom
→ ASIC - Application specific IC.

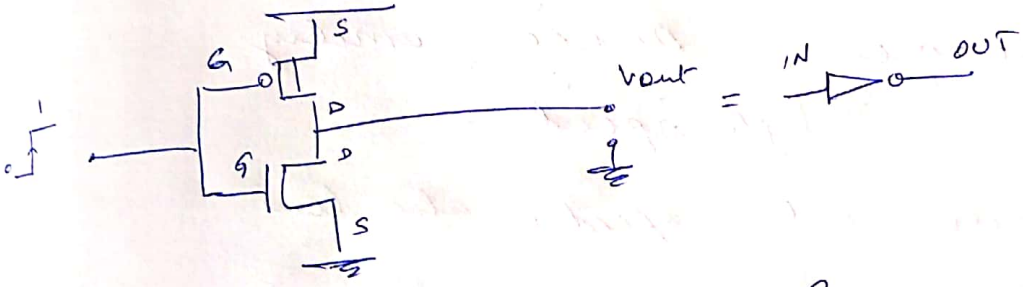
full customised → starting from scratch level.

semi custom.
↳ already predefined library available

ASICC : EX: μcontroller, μP.

EX: CMOS inverter

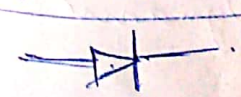
schematic :-



Q. why do we need Low Power?
↳ demand by applications (more features)
↳ low cost
↳ portability
↳ circuit complexity (has to be minimum)
↳ Power
↳ Area (has to be MIN) (area ∝ cost of manufacturing wafer)

* 80nm technology
* when the tech is scaled down (say from 180nm → 80nm)
some problems arise.
dominant problem → "interconnect problem"
→ interconnect b/w device to device
→ when devices are cascaded, more delay and make consume more power, ckt becomes complex, as interconnect becomes more.

*leakage current - exists in diode / transistor (mosfet)



when V > Vth, ⇒ Reverse saturation I actually as its very small.

S/D of MOSFET → also results in leakage current.

* Static Power → always represents leakage P

Static P = $V_{dd} I_{dd}$ → it is MAXIMUM when MAX I (Current) occurs in the circuit

* Low power ckt is mainly concentrated on _____ power

* Leakage I = Reverse biased current

* Power, Area and speed

Reduce the area - Device geometry
→ high speed.

Low power, but speed is also low.

* Device parameter

→ Technology → what is Requirement? (depends on)
→ Power supply requirement
→ Area
→ metal interconnects layers.

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* Different technologies levels :-

→ ckt level → logic level → software level
→ system level / architectural level

→ Adiabatic Power

Power analysis tools - SPICE tool
Probabilistic model

Power dissipated = Static P + Dynamic P

$P = P_{dc} + P_{dissipation}$ → only based on device → dynamic power → ckt behaviour

$P_{dis} \propto Cout\ V_{dd}^2\ f$

$P_{dc} = V_{dd}\ I_{dd}$.

Power planning ⟹ Power has to be ~~pre~~ predefined at the top level. and designed for that power in the back end.

19/1/2020

→ "Moore's law".

→ Low power design at the front end.

→ As channel length (L) decreases, the threshold voltage starts varying. (when L is large, the V_{th} remains constant).

→ ~~Less~~ P consumption may affect the environment as it draws energy.

→ computer requires more energy → electricity

→ Identification of the Power is imp for optimization (Power source)

→ Power analysis tools are available.

→ MAX Power dissipated → short ckt

→ Power consumption is due to: → s/w event → capacitance → short circuit → logic swing

Static

→ Sources of Power consumption

$P = P_{dc}$ (static) $+ P_{dyn}$ ← dynamic Power ← More dominant

$P = V_{DD}\ I_{DD}$.

P_{DC}

$P_{dyn} = Cout\ V_{DD}^2\ f$

due to switching event → $P_{dyn} \propto Cout\ V_{DD}^2\ f$.

* Speed, Power & Frequency :-

Circuit delay ⟷ Device performance.

delay ↑ ⟷ ↓ freq ↓

delay ↓ ⟷ ↑ freq ↑

→ delay ↓ speed ↑ frequency ↑ power ↑ performance ↓

* $\boxed{P \propto \text{speed}}$

* area ∝ density ∝ integration ∝ Power consumption

R_n, R_p

β_n, β_p

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{TP}|)}$$

$$R_n = \frac{1}{\beta_n (V_{DD} - (V_{Tn}))}$$

$C_{out} = C_{FET} + C_{load}$ ← internal FET contribution

↓ can be reduced by increasing the 'd'. $\left(C \propto \frac{1}{d}\right)$

$\boxed{C = \frac{\epsilon A}{d}}$ ← d: thickness b/w the metal plates.

Technology scaling :-

180 μm ——— 1.2 V

18 nm ——— 0.2 V

(Specific technology is designed for specific power)

* Problems occured due to scaling :-
→ Leakage P is also called as ~~I_GPO~~ I_{CBO} //.
→ Gate induced drain leakage current - I_{GIDP}
→ Punch through effect
→ sheet channel effect

~~2a~~ ~~Explain~~ ~~Read~~

* Levels of abstraction :-

EXPECTED

system	- partitioning, power driven power state
Algorithm	complexity, concurrency, regularity, locality
Architecture	- Parallelism, pipelining, redundancy, data encoding
circuit/logic	- logic state + manipulation transistor sizing energy recovery
Technology	- threshold reduction, double ~~threshold~~ device, energy recovery

* I C low power methodology requires optimization at all levels of abstraction.

① Technology. → V_{DD}
→ Threshold Reduction

0.12 μm — 6 Metal (1.2V, 2.2V)
0.18 μm - 6 Metal (0.8V, —)

② Ckt/Logic
→ Transistor resizing, ordering, logic in ckt,

③ Architecture.
→ H/l operation, synchronisation

④ Algorithm
→ key to reduce complexity of algorithm

⑤ System → fully functional
Subsystem → parts of the system

β_n } device transconductance.
β_p }

$$\beta_n = K'_n \left(\frac{W}{L}\right)_n$$

$$\beta_p = K'_p \left(\frac{W}{L}\right)_p$$

$K_n = \mu_n C_{ox}$
$K_p = \mu_p C_{ox}$ } processing parameter

(mobility factor depends on concentration)
K_n, K_p → processing parameters
↳ keep it constant
μ_n μ_p →
$\left(\frac{W}{L}\right)$ is varied according to requirement

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21/2/2020 Physics of power dissipation :-

Technology
Si based technology — semiconductor
- crystalline structure
- mobility related to device physics

current voltage relation of the device
V_{gs} - gate to source voltage
eq^n → physics of device → mobility
→ temp
→ current
→ power

How do you optimise the power ?
→ device structuring
→ -"- preordering
→ -"- prestructuring

note :
device architecture/ structure has an impact on device power

device modelling → related to physics
↳ linear
↳ parallel.

FET is always modelled as.

$V_m \propto \frac{V_{dd}}{2}$ ← mid pt voltage.

$V_m \propto \frac{\beta_n}{\beta_p}$ = device transconductance

power consumption also depends on - device geometry

aspect ratio = $\left(\frac{W}{L}\right)$ ratio

size ↓es → channel length ↓es. → dominant issue: leakage current ↑es

→ ultra-deep (deep ↑) sub-micron technology

→ [long channel and short channel effect]

what factors affect? →

→ orientation of the device → also matters.

Dynamic power dissipation in CMOS:-

$P_{dyn} = C_{out} V_{DD}^2 f$

P_{dyn} — arbitrary gate

dynamic power depends on the logic transitions of the CMOS devices.

when the C_{out} is connected to the inverter:

→ allows the current to charge.
(for a path for)

→ keeps on charging & discharging

⇒ there is a short ckt from Vdd → Gnd.

$C_{out} = C_{fo} + C_L$

C_{out} ↑. → more delay.

* So power consumption is min if we ↓ the C_{out}

* Power → 1st concern
Speed → 2nd concern.
Cost → 3rd concern.

→ As freq ↑es. P_{dyn} ↑es.

→ Also depends on input logic Transitions.

→ Area.
→ Temperature
→ Vdd
→ Gate sizing
→ selections of the insulating layer
→ Transistor sizing & gate oxide thickness

issues related to power (dynamic)

→ Transistor sizing and gate oxide thickness
t_{ox} (called as t_{ox})

→ device geometry
$\left(\frac{W}{L}\right)$

→ parasitic R ↑, delay ↑; P_{dyn} ↑
→ parasitic C
→ mosfet sizing/resizing

channel L ↑ ⇒ area ↑ es. ⇒ Tran cat area ↑ ⇒ P consumption ↓

* short channel
t_{ox} ↓ ⇒ more leakage prob & Vth Starts charging

t_{ox} → defined during manufacture
↳ affects $C_{ox} = \frac{A\varepsilon_0\varepsilon_R}{t_{ox}}$

→ change the dielectric to improve operational P
*OLED. → high cost → delicate → high resolution
→ high quality
OTFT → organic tin field effect transistor

Impact of tech scaling :- (nm scaling)
μm → nm (Moore's law)
32 → 12nm.

"autosound" → connected to app → for doctors → diagnosis check
↳ uses higher end processor.

2/2020

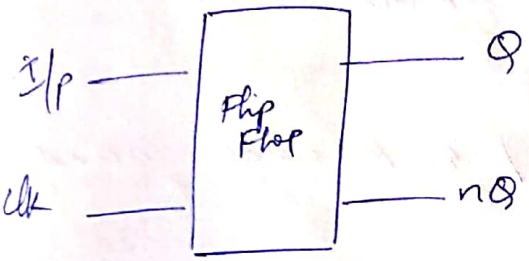
UNIT-2

Low power design at Circuit & logic level

Latches and Flip flop

Latch → not synchronised clock. **FlipFlop** → mem ckt / reg synchronised with clock.

Latch → It is a mem element.



→ Feedback → makes sure to hold the information
→ Low power memory is in demand.

→

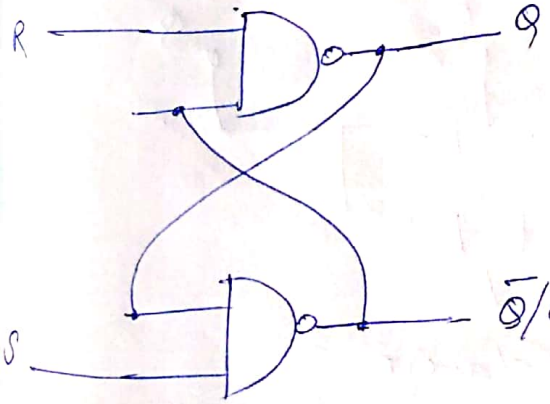
* RS Latch :-

Truth table :-

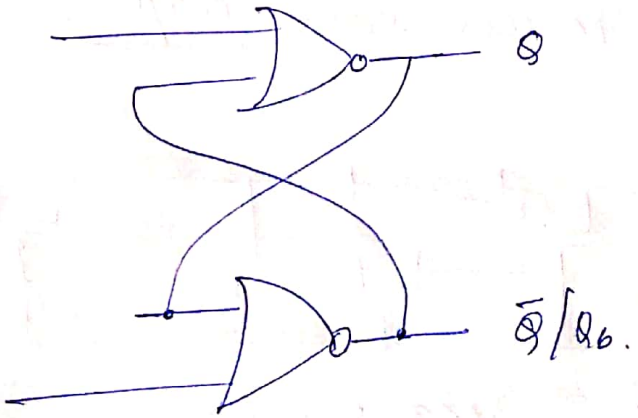
R	S	Q_{n+1}
0	0	Q
0	1	1
1	0	0
1	1	X

Q_n	Q_{n+1}	R	S
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

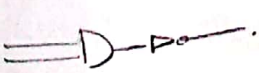
RS latch using NAND gate :-



NOR GATE :-



Gate level description



* Switch level / Fab level. ⟶ 'IC'

→ Placement and routing, planning ⇒ cmp → determine consumption

* Gate & Transistor

Gate → build from transistor

→

D F/F

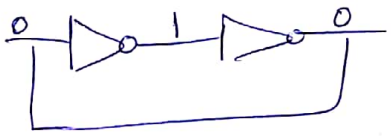
Q. Diff b/w Gate & Transistor

→ switch level

SR latch using MOSFETS.

↳ requires 8 Transistor [4 for each nand gate]

~~design a memory ele~~.



← stores some information

← using cascaded not gates

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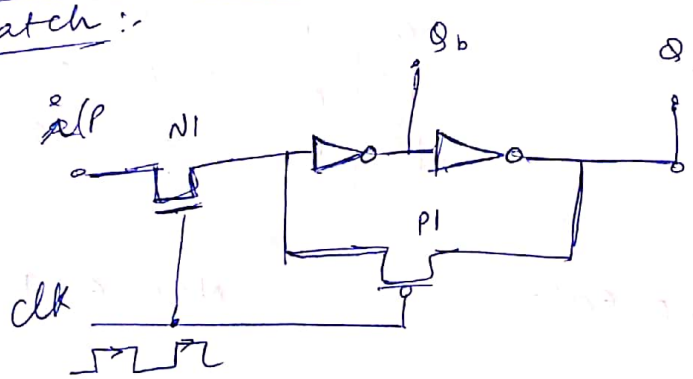
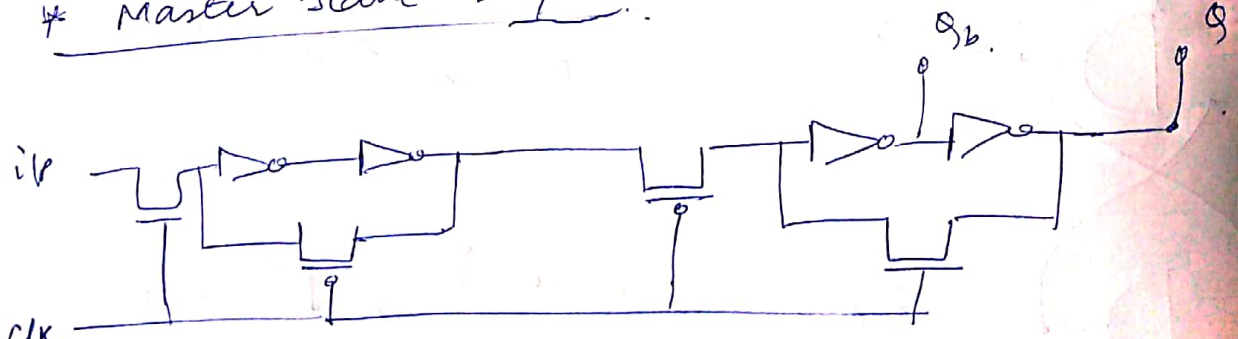
* D latch :-



* Master-slave D F/F :-



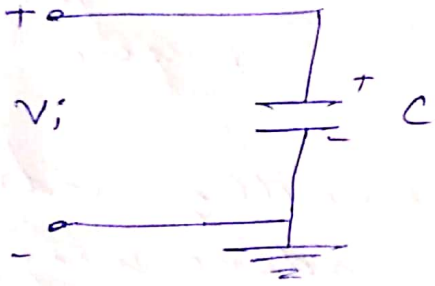
D F/F (master) & (slave)

12 Tran required

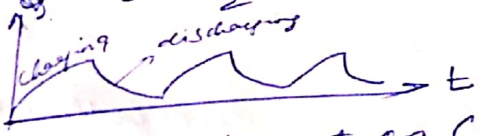
$Y = \overline{A(B+C)} + D$

→ AOI } 2 styles → also determines Power Consumption
→ OAI }

* ASIC
  → Tools used
  Cadence/etc.
* Power simulation tools
→ analog design is more complicated than digital design
* High capacitance nodes :-



fn of C :
stores charge
$Q = CV$
$E = \frac{1}{2}CV^2$



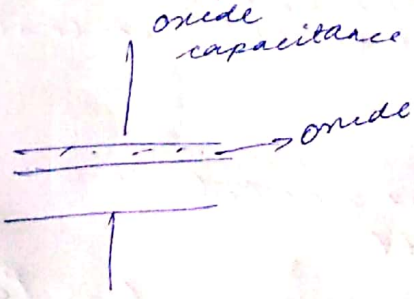
→ Power consumption → more dominant on C.

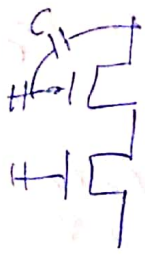
Battery
→ life → depends on Technology & usage.

Capacitor → Parasitic capacitance
→ electrolytic -n
→ Intrinsic (intermode) n.
→ Ceramic -n
→ Bulk capacitance
→ Node capacitance

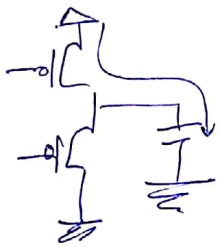
Node capacitance → comes based on structuring of the mosfets

C_{GS} (gate, source) C_{DN} (drain, n channel) C_{GP} (gate, p channel) C_{DP} drain, p channel (sub)

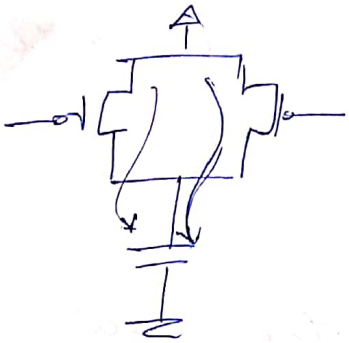




* Intra node capacitance



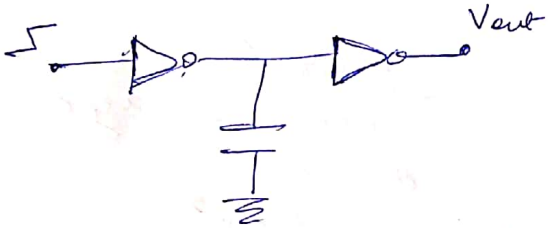
in series



in parallel

$C = \frac{A \epsilon_0 \epsilon_r}{d}$

ϵ - permittivity
A - Area
d = distance b/w the plates



capacitor coupling is required for isolation purpose.

* device sizing & modelling introduces capacitance
* Analysis of capacitance → done using Elmore's delay model

per 1st interval.

15/2/2020

Low Power digitised library :-

AOI → Basic circuitary
OAI

PLA - Programmable logical array.
customised application → for specific appl.
designed at certain low power design.

Reordering (Reorganisation) of cells → placement of cells (placement of Vdd, Vss, consumes more P)
& restructuring → next to cell dimensions (scattered dimension)
(not same)

Reordering of cell :
→ sometime multiple Vdds are needed.
→ placement of Vdd, Vss, matters.
→ if properly done, can consume less Power.

* Signal gating
  - basically it is an input source
  - very imp for output response.
  - 'power spikes' → power consumption
  - The style of connecting the input → P Conc

* Types of sig gating → also imp as determining P consumption

Ex: *ALU
- data synchronisation → using clock.
- sig transfer from 1 stg to another stage.

* Threshold voltage (V_{th}) → sig gating (i/p) depends on V_{th}
  - effects Power consumption

* Role of sig gating :-
  - Reduce Noise
  - Reduce Power consumption

} P also depends on noise

* In opam → even if i/p = 0 V, the o/p will have noise to correct it → offset voltage is given

* Logic/signal encoding :-

FSM
- no of states ∝ Power consumption
- Graphical method → demonstrates opn of on the ckt
- optimization → logical methods to optimise.
  - TT, Kmap are used to reduce no of states