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SEMINAR REPORT ON
(EC0201)

VLSI implementation of a novel sensor architecture for Industrial Wireless Sensor Networks

Submitted to the partial fulfillment for the award of the degree of

Bachelor of Engineering
In

Electronics and Communication Engineering

Submitted by:

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VIII Semester B.E

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2019-20

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CERTIFICATE

This is to certify that Mr. ADARSH S SRIVATSA bearing USN 4NI16EC002 has given a technical seminar presentation on the topic "VLSI implementation of a novel sensor architecture for Industrial Wireless Sensor Networks" in partial fulfillment of curriculum prescribed for the VIII semester of B.E course in Electronics and Communication Engineering during the year 2019-20.

Signature of Guide

Signature of Examiner 1

Signature of Examiner 2

ACKNOWLEDGEMENT

With immense please I, Adarsh S Srivatsa presenting “VLSI implementation of a novel sensor architecture for Industrial Wireless Sensor Networks” seminar report as part of the curriculum of Electronics and Communication Engineering. I wish to thank all the people who gave me unending support.

I would like to express my gratitude towards **Dr. Rohini Nagapadma**, The Principal, NIE for extending all necessary facilities.

I would like to express my gratitude towards **Dr. Narasimha Kaulgud,** Head of the Department, ECE, NIE for providing all necessary facilities.

I wish to express my sincere gratitude to my seminar guide **Dr. Vijay B T**, Assistant Professor, Department of ECE, NIE, Mysuru for constant guidance and encouragement in every stage of preparation. Her careful monitoring of the complete process helped in improving in presentation of the ideas. I take this opportunity to sincerely acknowledge her for performing all evaluation studies.

Finally, I thank all my professors, non-teaching stuff and my parents, for their constant support and guidance.

Adarsh S Srivatsa

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ABSTRACT

Wireless Sensor Networks (WSNs) are distributed sensing ecosystems equipped with computational intelligence and radio communication capabilities. The ‘neurons’ of a typical WSN referred to as Sensor Nodes or Motes are tiny, low-cost, resource-efficient modules with embedded intelligence facilitating ultra-fast deployment, flexibility and energy-efficiency in their operations. Industrial Wireless Sensor Networks or IWSNs feature hundreds and thousands of sensors placed in and around the plant to enable remote monitoring, maintenance and troubleshooting. In this article, we present a full custom design of a sensor node for Industrial Wireless Sensor Networks with the primary focus on the architectural aspects of the implementation. The proposed sensor architecture consists of a 4-channel 12-bit Delta-Sigma ADC, a controller subsystem with SPI Master-Slave interfaces and an OFDM RF Transmitter subsystem. The architecture outlined in this article is a novel modular design characterized by an OFDM baseband processing RF subsystem facilitating reliable monitoring of plant variables which is a crucial parameter in Industrial Wireless Sensor Networks. The proposed system has been subjected to Front-end RTL simulation and synthesis using an array of EDA tools.

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1. INTRODUCTION

Wireless Sensor Networks (WSNs) are distributed sensing ecosystems equipped with computational Intelligence and radio communication capabilities. The ‘neurons’ of a typical WSN referred to as Sensor Nodes or Motes are tiny, low-cost, resource-efficient modules with embedded intelligence facilitating ultra-fast deployment, flexibility and energy-efficiency in their operations. Industrial Wireless Sensor Networks or IWSNs feature hundreds and thousands of sensors placed in and around the plant to enable remote monitoring, maintenance and troubleshooting.

As WSN architectures and protocols evolved, their tasks extended beyond sheer reporting. Their complexity expanded many folds in the events to be detected, redundancy in reporting required, density of deployments, quality of data, coverage span and reliability. Significant control overhead resulted from mandating coordination, especially when driven by attempts to synchronize sensor node operation. More importantly, the advent of real-time sensing applications mandated that WSNs operate reliably under significant constraints of time and power consumption. A comprehensive survey on synchronization problems in WSNs is presented in and highlights how a single requirement can significantly impact operational mandates of a WSN and increase its overhead without improving the quality of the data collected.

However, manipulating sink and node locations resulted in significant work on WSN deployment and mobility. Researchers attempted to study the effect of relocating nodes for improving coverage and connectivity, and the impact of error on each. In support of dense deployments cited the value of redundancy in reports to achieve higher reliability, improving failure mitigation schemes as nodes are prone to faults, and prolonging network lifetime as we employ advanced duty cycling schemes. However, researchers have argued that improving the quality of nodes and ensuring minimalistic operational mandates – in addition to reducing the overhead of synchronizing duty cycles – would yield more efficient WSNs, especially as we avoid unnecessary contention over an already strained medium. Simply put, what we gain in reliability we lose in MAC contention and synchronization efforts, not to mention the cost of all the extra nodes.

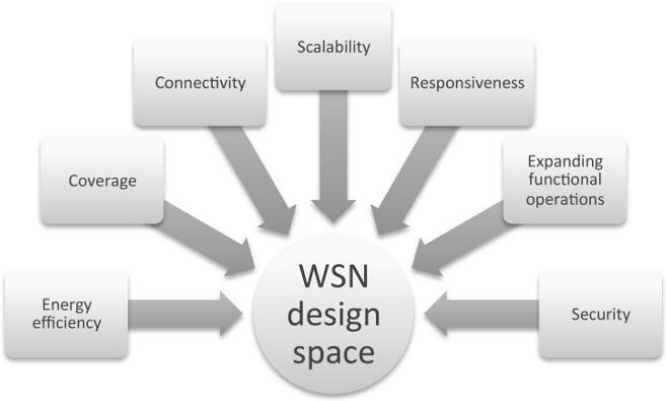

Fig. 1.1 ***The fundamental design space of WSNs***

Orthogonal Frequency Division Multiplexing (OFDM) is a digital multi-carrier modulation scheme that extends the concept of single subcarrier modulation by using multiple subcarriers within the same single channel. Rather than transmit a high-rate stream of data with a single subcarrier, OFDM makes use of large number of closely spaced orthogonal subcarriers that are transmitted in parallel. Each subcarrier is modulated with a conventional digital modulation scheme (such as QPSK, 16QAM, etc.) at low symbol rate. However, the combination of many subcarriers enables data rate similar to conventional single-carrier modulation schemes within equivalent bandwidths.

OFDM is based on the well-known technique of Frequency Division Multiplexing (FDM). In FDM different streams of information are mapped onto separate parallel frequency channels. Each FDM channel is separated from the others by a frequency guard band to reduce interference between adjacent channels.

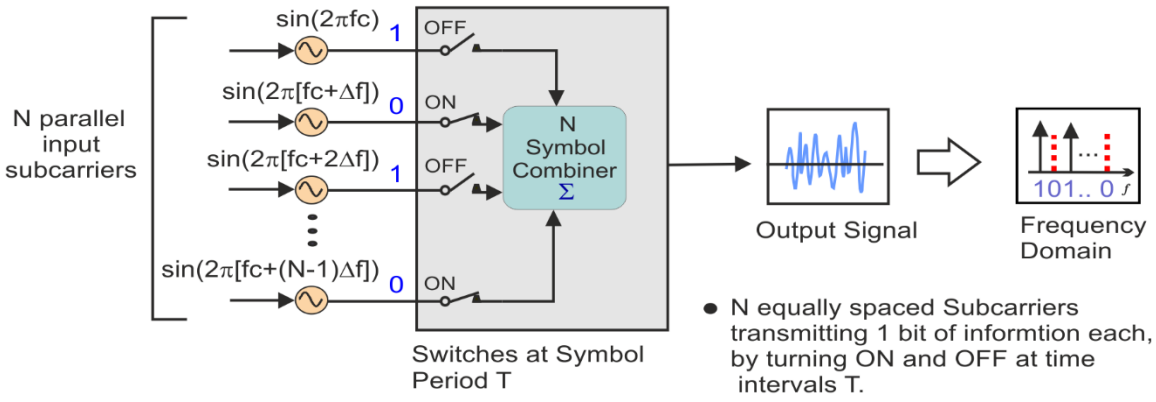

Fig. 1.2 ***Working principle of OFDM***

2. ARCHITECTURE

Wireless Sensor Networks constitute a group of spatially distributed autonomous sensors used to monitor various parameters such as temperature, pressure, acoustics, velocity images, etc. which has to cooperatively pass the data along to the central monitoring station. These autonomous modules termed 'sensor nodes' typically consist of the following parts: A radio transceiver, a microcontroller, an electronic circuit to interface the sensor with a suitable energy source and some form of preprocessing capabilities to acquire the data in the required format.

The data acquired is processed by the node and transmitted to the adjoining node in the network. The nodes in the network then cooperatively pass along the data to the Gateway Node which then forwards it to the central monitoring station. The features of a typical sensor node include, Resilience, Minimum power consumption, Mobility and Heterogeneity, Scalability and Low cost.

The most common WSN architecture follows the OSI architecture Model. The architecture of the WSN includes five layers and three cross layers. Mostly in sensor network we require five layers, namely application, transport, network, data link & physical layer. The three cross planes are namely power management, mobility management, and task management.

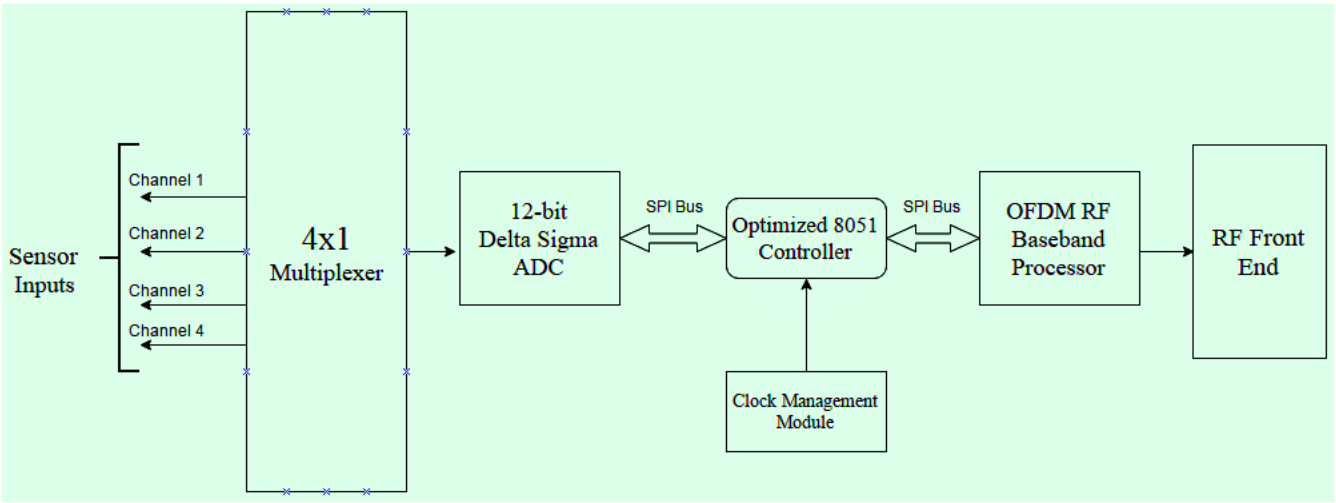

Fig. 2.1 ***The architecture of the senor node***

3. METHODOLOGY

The sensor node consists of three subsystems namely sensor subsystem which collects data from the sensors and it is followed to the processor subsystem which serialize the data and control the rate of flow of data to the radio transmitter subsystem which modulates the original signal and mapped to suitable carrier using OFDM techniques which has advantages of its own, later the signal is transformed back to analog signal by digital to analog convertor which is radiated by antennas from transmitter end to gateway node.

3.1 The sensor subsystem

The Analog-to-Digital Converter (ADC) constitutes the primary component of this subsystem tasked with converting the data obtained from the generic sensor modules into their equivalent digital representation and transferring them into the processing subsystem for further operations. The sensor subsystem also consists of an Analog multiplexer (4x1) employed to enable a 4-channel 12-bit ADC operation in order to facilitate a variety of sensors to be interfaced with the node and thus enhancing the versatility of its application.

Delta-Sigma ADC consists of delta-sigma modulator, digital filter and decimator which facilitates low pass configuration, best suited for high accuracy and high-resolution applications.

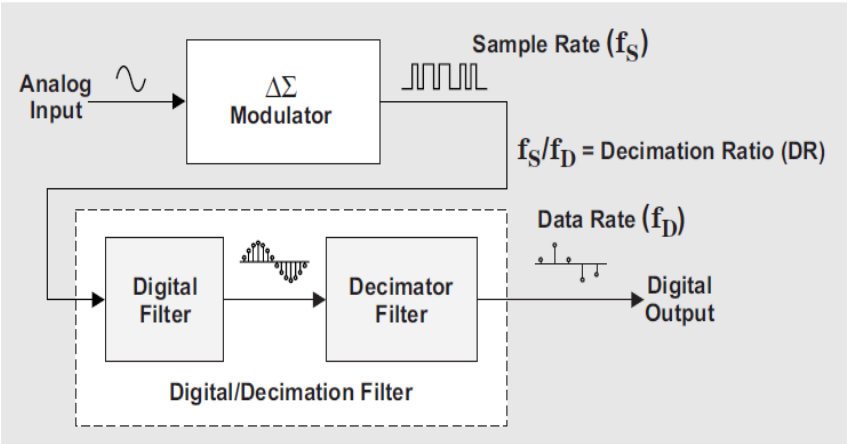

Fig. 3.1 ***Delta Sigma ADC Block Diagram***

3.1.1 Delta Sigma modulator

The DS modulator is the heart of the DS ADC. It is responsible for digitizing the analog input signal and reducing noise at lower frequencies. In this stage, the architecture implements a function called noise shaping that pushes low frequency noise up to higher frequencies where it is outside the band of interest. Noise shaping is one of the reasons that DS converters are well-suited for low frequency, high accuracy measurements.

In a DS converter, the analog input voltage signal is connected to the input of an integrator, producing a voltage rate-of-change, or slope, at the output corresponding to input magnitude. This ramping voltage is then compared against ground potential (0 volts) by a comparator. The comparator acts as a sort of 1-bit ADC, producing 1 bit of output ("high" or "low") depending on whether the integrator output is positive or negative.

This is the delta-sigma concept in action: the first comparator senses a *difference* (Δ) between the integrator output and zero volts. The integrator *sums* (Σ) the comparator's output with the analog input signal. Functionally, this results in a serial stream of bits output by the flip-flop. If the analog input is zero volts, the integrator will have no tendency to ramp either positive or negative, except in response to the feedback voltage.

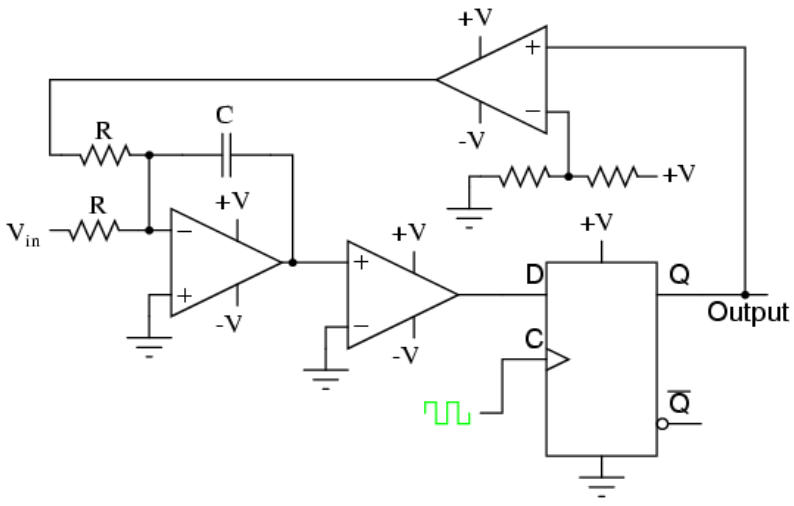

Fig. 3.2 ***Delta Sigma Modulator***

3.1.2 Digital-filter function

The digital-filter function implements a low-pass filter by first sampling the modulator stream. An averaging filter is the most common filter technique used in DS converters. Almost all DS ADCs incorporate a class of averaging filters called sinc filters.

3.1.3 Decimator function

The Decimator reduces the output data rate by discarding redundant data samples in order to bring the output to a more manageable data rate. The parameter of interest in Decimator configuration is the Decimation Ratio (DR).

Decimation Ratio (DR) = fs/fd

Where, fs = Delta Sigma Modulator's sampling rate and fd= Decimator's output data rate.

The stream of 1's and 0's is subsequently digitally filtered to produce a slower stream of multi-bit samples. The sigma-delta modulator loop typically runs at a much higher frequency than the final output rate of the digital filter. For example, a converter with a 2kHz output data rate may have a modulator loop frequency of over 2.5MHz.

3.2 The processor subsystem

The processor subsystem is the 'brains' of the sensor node comprising a general-purpose controller tasked with maintaining the data transfer functionalities between the sensor subsystem and the radio transmitter subsystem.

A conventional 8051-microcontroller core is optimized to incorporate a minimum number of I/Os, SPI Master-Slave interface support, interrupts, pipelining strategies and low-power sleep modes. The Serial Peripheral Interface (SPI) is a de-facto serial synchronous communication interface consisting of a single master driving one or more slaves. The SPI bus constitutes four logic signals namely, Serial Clock (SCLK), Slave Select (SS), Master-Out Slave-In (MOSI) and Master-In Slave-Out (MISO).

The Clock Management Unit is another significant part of the node categorized under the processor subsystem. This module constitutes a PLL-based clock distribution logic which is the norm in modern high-performance digital circuits.

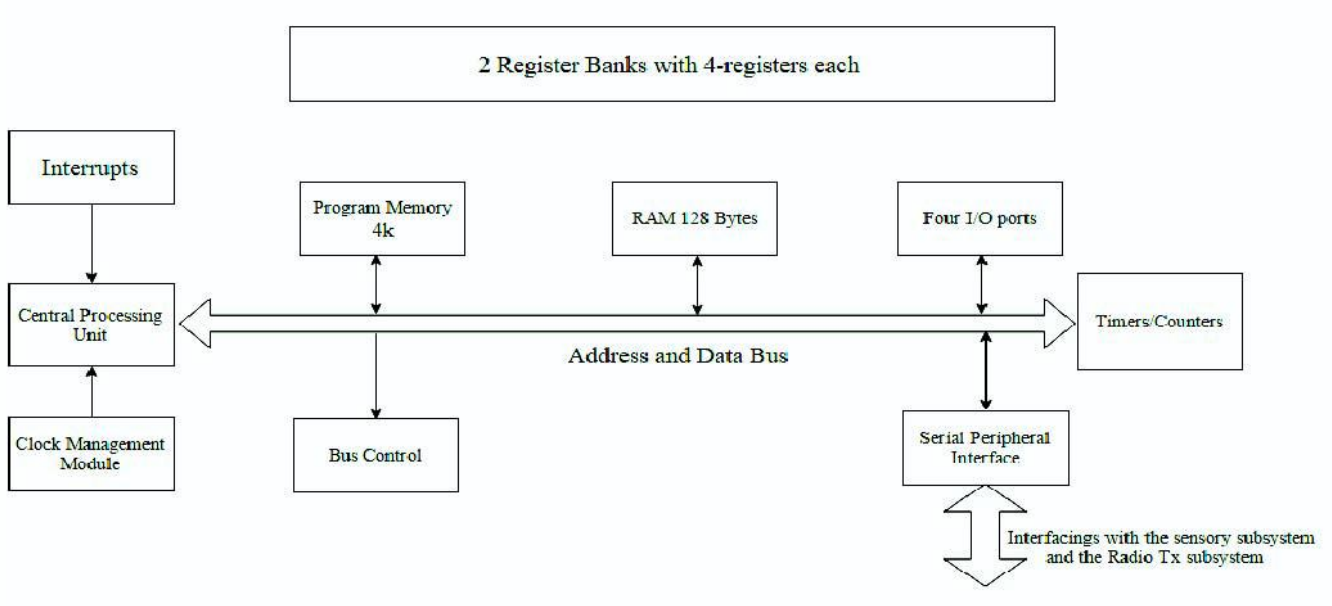

Fig. 3.3 Optimized 8051 Microcontroller Architecture

Here we can employ two kinds of wake-up strategies. First, synchronous protocols are needed to periodically activate the radio front ends. At regular time instants, the nodes probe the radiofrequency channel to determine whether another node wants to establish a communication, and the activation decision is taken at the node level. Such method supposes that global synchronization across all nodes in the wireless network is guaranteed. Second, remote nodes request a node to activate its main radio-frequency interface, auxiliary radio is needed in this case.

Some of the commonly adopted 'Battery-Aware Scheduling' methodology for periodically arriving task graphs with real time deadlines and precedence constraints. Scheduling of even a single task graph while minimizing the weighted sum of a cost function has been shown to be NP-Hard. First, a good DVS algorithm dynamically determines the minimum frequency of execution. Then, a greedy algorithm allows a near optimal priority function to choose the task which would maximize slack recovery.

3.3 The radio transmitter subsystem

Orthogonal Frequency Division Multiplexing (OFDM) is a digital multi-carrier modulation scheme which synthesize an infinite band-limited orthogonal time functions in a limited frequency band. This method of digital signal modulation involves a single data stream is split across several separate narrowband channels at different frequencies to reduce interference and crosstalk.

OFDM is the most prominent waveform in current wireless communications, and it is characterized by the orthogonality between subcarriers, which eliminates inter-carrier interference Currently, 4G LTE systems improve the frequency response of Cyclic Prefix OFDM (CP-OFDM) by applying time-domain windowing of the CP-extended OFDM symbols and overlapping the edge transition of adjacent symbols: Weighted Overlap and Add (WOLA).

The distance in signal space between any two sets of received signals is the same as if the signals of each AM channel were transmitted through an independent medium and inter symbol interference in each channel were eliminated by reducing data rate the input high rate data stream is divided into many low-rate streams that are transmitted in parallel. The data is transmitted in parallel across the various carriers within the overall OFDM signal. Being split into several parallel "sub streams" the overall data rate is that of the original stream, but that of each of the sub streams is much lower, and the symbols are spaced further apart in time, thereby increasing the symbol duration and reducing the inter symbol interference. With reduction in the interference among symbols and makes it easier to receive each symbol accurately while maintaining the same throughput.

The data is then passed to a modulation mapper, which is commonly Phase Shift Keyed (PSK) or Quadrature Amplitude Modulation (QAM) depending on the type of communication system. The modulator thus concurrently and separately modulates a set of tones in the OFDM spectrum. The output of the modulator is then converted from serial to parallel form and the complex frequency domain data is thus transformed to time domain using Inverse Fast Fourier Transform (IFFT). The time varying data is then cyclically extended with a cyclic prefix to reduce inter-symbol interference between successive OFDM symbols. Finally, the output of the cyclic prefix block is fed to the digital to analog converter, and then sent to the antenna for transmission.

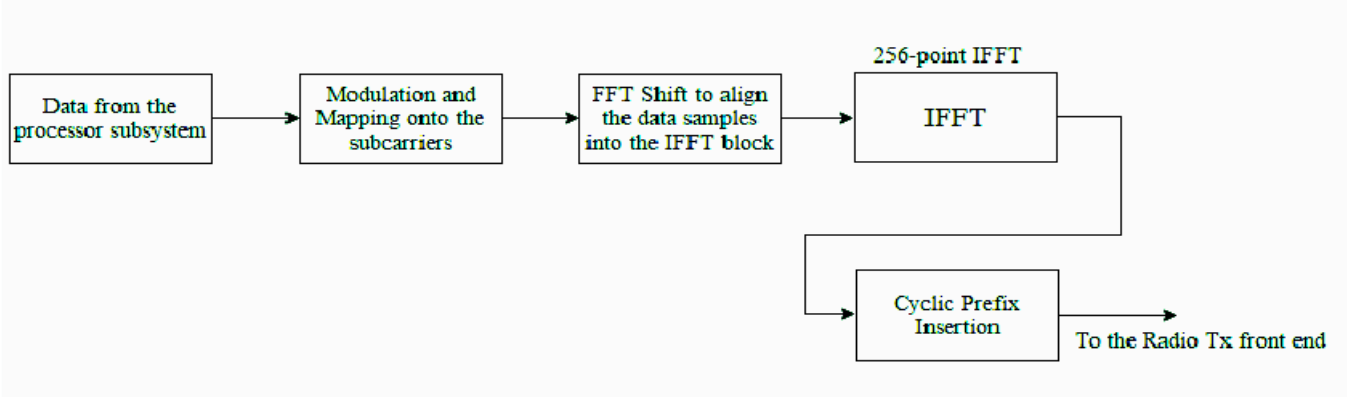

Fig. 3.4 Radio subsystem block diagram

3.3.1 Mapper

The mapper converts input data into complexed valued constellation points, according to a given constellation. Typical constellations for wireless applications are, BPSK, QAM, and 16 QAM,

3.3.2 IFFT

The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain. The discrete-time representation of the signal using N sub-carriers.

3.3.3 Cyclic prefix

In order to combat the inter-symbol interference, OFDM uses guard interval or a cyclic prefix before each symbol. The cyclic prefix is a copy of the last n samples from the IFFT, which are placed at the beginning of the OFDM frame. Every OFDM symbol is prepended with a Cyclic Prefix (CP), which mitigates inter-symbol interference, but contributes to the degradation of spectral efficiency.

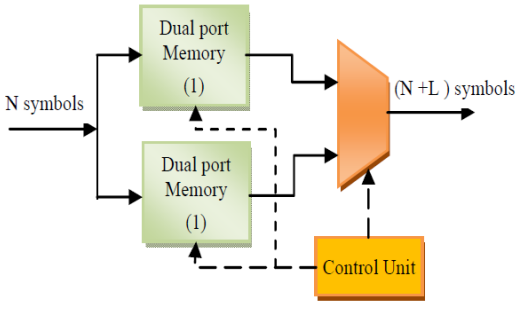

Fig. 3.5 Cyclic extension internal architecture

4. RESULTS AND CONCLUSION

The proposed architecture is described with the simulation tools and functionalities are getting verified with the observation. The sensor subsystem which consists of 4 channel 12-bit ADC is decribed using Verilog AMS in the Cadence AMS Design suite (Cadence Virtuoso design environment and Spectre simulator) and simulation results in Fig. 4.1 . The general purpose controller configuration is described in Verilog HDL and the corresponding simulation results are presented in Fig. 4.2 . The radio subsystem consisting of OFDM baseband processor employ QPSK modulation and 256-point IFFT is modelled using Verilog HDL in Fig. 4.3 . The RTL description of the design is simulated for functional verification. Before synthesizing actual hardware, the designs are modelled in MATLAB and Simulink softwares for the validation of the functional correctness of the chosen parameters.

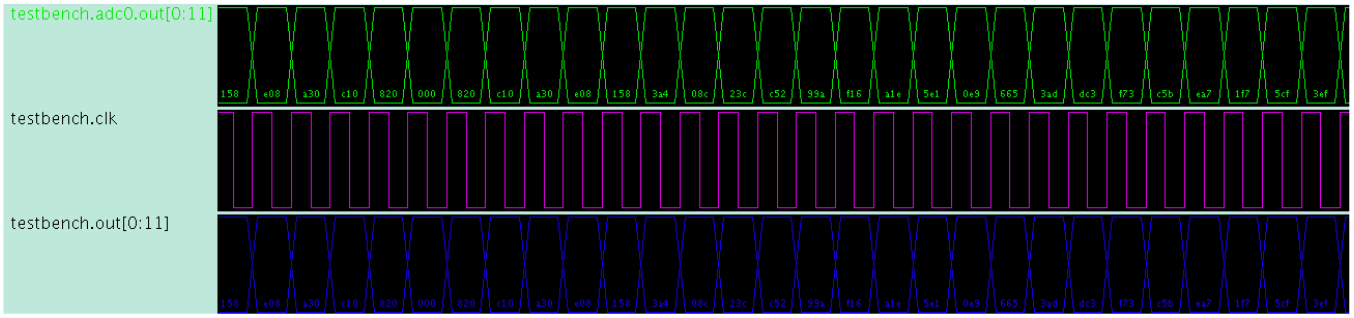

Fig. 4.1 Simulation results of the ADC subsystem

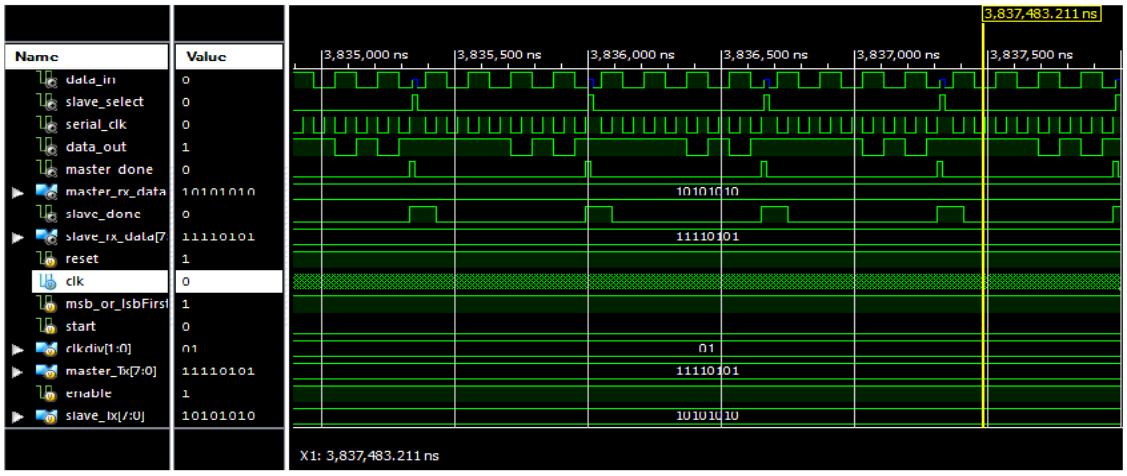

Fig. 4.2 Simulation results of the SPI communication in processor subsystem

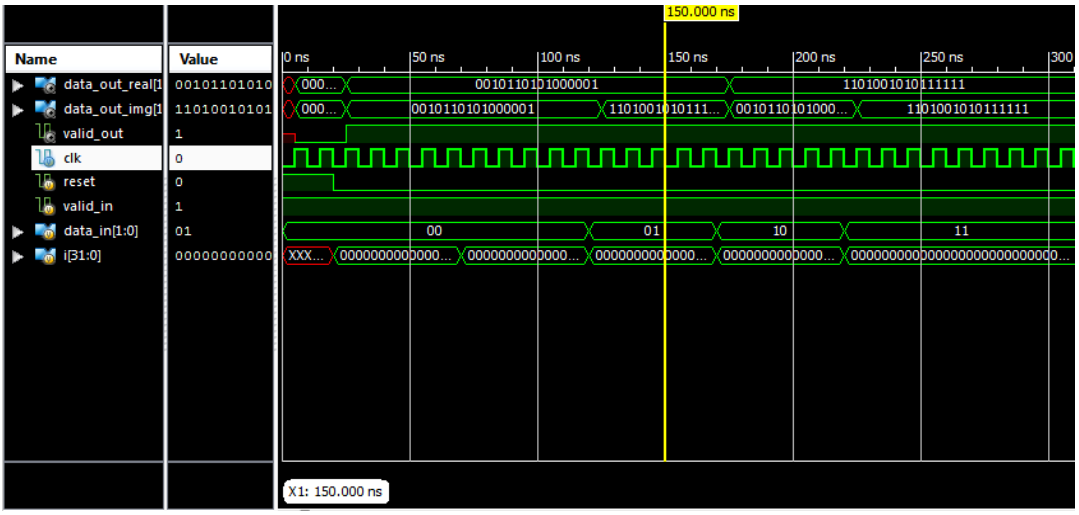

Fig. 4.3 Simulation results of the QPSK block in radio transmitter subsystem

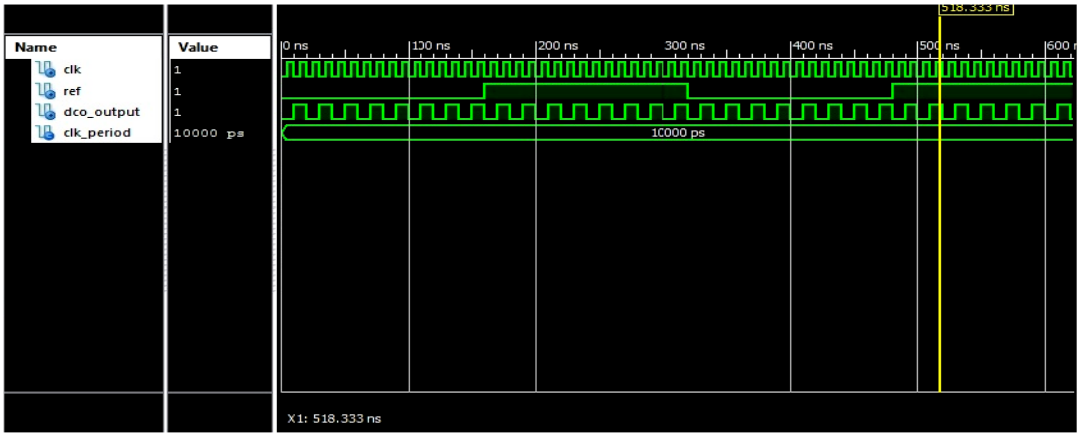

Fig. 4.4 Simulation results of the Clock management module

OFDM technology facilitates multi-channel baseband transmission over band limited frequencies which gives advantage for establishing communication over the network of sensor nodes. Optimized microcontroller offers reduction in energy footprint with adoption of various application specific techniques such as Battery Aware Task Scheduling (BATS) and wake-up architecture for the radio front-end, using an OFDM frequency footprint which enables activation of only the required components.

The proposed novel architecture of WSN addresses the constraints of low power requirements, limited bandwidth, scalability and mobility. With the usage of better algorithm energy requirement is minimal and with different techniques of clock and power gating in the design reduces the losses.

5. FUTURE SCOPE

Future works on the system include the design of the RF front end which provides details of antenna specifications and radiation properties, System Verilog based Verification for formal verification of the working designs, Synthesis of design to ensure the behavioral and system considerations , Physical Design to generate a working model and perform test validation to check for industrial standards and more importantly enabling energy efficiency of the node through system-level strategies facilitating reduced energy consumption. The advent of recent energy harvesting technology provides roadmap for battery free networks.

6. APPLICATIONS

Wireless sensor networks may comprise of numerous different types of sensors like low sampling rate, seismic, magnetic, thermal, visual, infrared, radar, and acoustic, which are clever to monitor a wide range of ambient situations. Sensor nodes are used for constant sensing, event ID, event detection & local control of actuators. The applications of wireless sensor network mainly include health, military, environmental, home, & other commercial areas.

- In health care monitoring, Body-area networks can collect information about an individual's health, fitness, and energy expenditure.
- In environmental sensing, it can be used for Air pollution metrics, landslide detection, forest fire detection, water quality monitoring and seismic activity.
- In military domain, it is used for Surveillance, security and Area monitoring like geo-fencing applications.

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***Abstract*—Wireless Sensor Networks (WSNs) are distributed sensing ecosystems equipped with computational intelligence and radio communication capabilities. The 'neurons' of a typical WSN referred to as Sensor Nodes or Motes are tiny, low-cost, resource-efficient modules with embedded intelligence facilitating ultra-fast deployment, flexibility and energy-efficiency in their operations. Industrial Wireless Sensor Networks or IWSNs feature hundreds and thousands of sensors placed in and around the plant to enable remote monitoring, maintenance and troubleshooting. In this article, we present a full custom design of a sensor node for Industrial Wireless Sensor Networks with the primary focus on the architectural aspects of the implementation. The proposed sensor architecture consists of a 4-channel 12-bit Delta-Sigma ADC, a controller subsystem with SPI Master-Slave interfaces and an OFDM RF Transmitter subsystem. The architecture outlined in this article is a novel modular design characterized by an OFDM baseband processing RF subsystem facilitating reliable monitoring of plant variables which is a crucial parameter in Industrial Wireless Sensor Networks. The proposed system has been subjected to Front-end RTL simulation and synthesis using an array of EDA tools and the subsequent results have been critically examined in this article.**

Keywords—IWSNs; Delta Sigma ADC; SPI; PLL; OFDM.

I. INTRODUCTION

The domain of Wireless Sensor Networks (WSNs) has quickly turned out to be a highly sought after field primarily due to the plethora of research opportunities embedded in it. Wireless Sensor Networks constitute hundreds and thousands of sensors (if not more), deployed in and around the facility of interest in order to monitor, maintain and troubleshoot critical operations. The inherent complexities of WSNs arise from the fundamental fact that Sensor Design and associated Networking involve design constraints in Wireless Communication Methodologies, Networking Techniques, Security Protocols and System Design & Manufacture, prompting engineers and researchers to examine various tradeoffs involved in their large-scale deployment. However, recent advances in semiconductor technology and wireless communications have led to significantly efficient, robust and cheap sensor nodes facilitating a much-needed global outreach enabling ubiquitous deployment, further accelerating potential applications of WSNs.

The popularity of WSNs can be traced back to their origin in the 1950s: The US Military's Sound Surveillance System (SOSUS) which was used to track and detect Soviet submarines. The SOSUS consists of an interconnected network of acoustic sensors on the ocean bottom, a system still used today by NOAA (National Oceanic and Atmospheric Administration) for monitoring and recording seismic activity. Later, in the 1960s and 1970s, the US Defense Advanced Research Projects Agency (DARPA) in association with Carnegie Mellon University and MIT Lincoln Labs [3] enabled progressive advancements in the Distributed Sensor Networks (DSN) which subsequently led to the penetration of the concept of wireless sensor networking into the commercial and industrial arena. Numerous initiatives such as the Zigbee Alliance, the UCB PicoRadio program, the NASA Sensor Webs and the UCLA Wireless Integrated Network Sensors were aimed at analyzing the tradeoffs involved in WSNs thereby facilitating faster deployment scenarios with a significant performance increase. The advancements in Sensing technologies, Semiconductor devices, Networking protocols and Energy Harvesting techniques [3] are the primary driving forces behind the popularity of WSNs in the industrial, academic and commercial space.

Realizing the importance of WSNs, the Ministry of Communication and Information Technology, Government of India published a detailed roadmap outlining the implications of WSNs to the industries in India and abroad. The research article "Wireless Sensor Networks: Technology Roadmap" brought out by the MCIT, DIT, Govt. of India in association with IIT-Bombay [4] talks about the Current R&D trends, WSN Hardware, Investments in R&D, Potential applications and Survey results detailing the objectives and promises of this lucrative field.

Understanding these facets of WSNs, the research presented in this paper revolves around the design and development of a sensor node for Industrial WSNs while analyzing the numerous tradeoffs inherent in it.

The sensor node architecture detailed in this article constitutes a 4-channel 12-bit Delta Sigma ADC, a controller subsystem with SPI Master-Slave interfaces and an OFDM RF Transmitter subsystem. The 4-channel ADC enables connecting and configuring four different sensors (Temperature sensors, Pressure sensors, etc.) in order to provide a holistic approach to the monitoring capabilities of the node. The sensor node design focusses on remote monitoring of plant parameters, for instance, the sensor node can be used to gather information regarding the temperature and pressure within a

978-1-5090-0612-0/16/$31.00

gas turbine and report these parameters to a monitoring station for further actions, if needed. The controller subsystem serves as the 'Brains' of the operation facilitating data transfer between the ADC and the RF Tx subsystem. The RF Transmitter subsystem enables digital baseband processing of the collected data from the controller and forwards it to the Analog front-end module for transmission toward the remote monitoring station.

Although a whole lot of research exists in the domain of Wireless Sensor Networks, there is a lack of literature on the end-to-end design of a comprehensive sensor node for IWSNs. In this article, we present the design and development of an Analog-to-Digital Converter, an 8051-controller based processing subsystem along with its associated interfaces and an OFDM Baseband processing subsystem for reliable communications between the node (which is deployed in the industrial ecosystem) and the remote monitoring station. This article details a modular architecture characterized by three major features which are extremely relevant in today's WSN landscape. Firstly, the provision of a multiplexer in the ADC subsystem facilitating a 4-channel operation of the Delta-Sigma ADC accounts for the versatility of our design, i.e. a wide array of sensors can be connected to the system enabling simultaneous monitoring of various performance indices of the industrial ecosystem. Secondly, the RF subsystem of the proposed design constitutes an OFDM Baseband processing module which accounts for the reliability and efficiency of communications between the sensor node and the monitoring station. Finally, the processing subsystem based on the 8051-controller core is advantageous to our design primarily because of its smaller physical size and smaller program and data space.

The next section of the article gives an overview of the Architecture and Characteristics of the proposed design while the subsequent sections detail individual subsystems and their implementation. Section III talks about the design and implementation of the ADC, Controller and RF Tx subsystems. Section IV details the design parameters and simulation results of the proposed architecture and Section V presents a concluding argument validating the research perspective presented in this article.

II. Design Overview: Architecture and Features

Wireless Sensor Networks constitute a group of spatially distributed autonomous sensors used to monitor various parameters such as temperature, pressure, acoustics, velocity, images, et cetra and to cooperatively pass the data along to the central monitoring station. These autonomous modules termed 'sensor nodes' typically consist of the following parts: A radio transceiver, a microcontroller, an electronic circuit to interface the sensor with a suitable energy source and some form of pre-processing capabilities to acquire the data in the required format (for instance, we employ an ADC to gather data from analog sensors monitoring the plant environment and convert them into their equivalent digital representation for further processing). The data acquired is processed by the node and transmitted to the adjoining node in the network. The nodes in the network then cooperatively pass along the data to the Gateway Node which then forwards it to the central monitoring station. Some WSNs exhibit a bi-directional architecture which enables remote access and control of sensor activity. The size and cost constraints involved in sensor node design imposes corresponding constraints on other design features such as memory, energy consumption, computational speed and bandwidth. The features of a typical sensor node include, Resilience, Minimum power consumption, Mobility and Heterogeneity, Scalability and Low cost. Along with these generic characteristics, a sensor node should cope with harsh environmental conditions, should be easy to deploy and maintain and above all the transmission capabilities should feature security measures, especially in the military and industrial environments.

Wireless sensor nodes generally constitute a sensor subsystem, a general-purpose microcontroller and a wireless transceiver, with an event-based operating system such as TinyOS. The design of a sensor-node for WSN-based applications requires deep insight into the Hardware and Software development aspects. The methodologies adopted in their design can either be application-specific or generalized. For instance, [2] details a VLSI architecture for a sensor node employed in a Wireless Image Sensor Network (WiSN). The SoC-based design methodology outlined in [2] consists of a general-purpose embedded microcontroller along with dedicated hardware accelerators for image processing and wireless communication. In contrast to this, [5] talks about a customizable modular event-driven architecture facilitating the addition or removal of event dispatchers and event handlers in order to suit the corresponding WSN application, thereby presenting a more generalized topology of sensor-node design. However, both emphasize on the use of hardware-based functionalities to facilitate faster and more-efficient execution of computationally intensive tasks.

The energy harvesting and consumption aspects of sensor nodes in Wireless Sensor Networks have recently drawn in significant research from both the industry and academia. Low Power VLSI design techniques are of primary importance in this arena where everyone is trying to reduce the 'energy footprint' of their node. While the low-power modular VLSI implementations have their advantages, an energy-efficient design at the top-level facilitates a relatively higher improvement. For instance, a Battery Aware Task Scheduling (BATS) technique detailed in [6] enables 60mW maximum power consumption in full-working mode (180nm technology node). Reference [7] outlines a 'Wake-up' architecture for the radio front-end, using an OFDM frequency footprint which enables activation of only the required components. The novelty of the research presented in [7] lies in its simplicity: It employs two multi-band filters to facilitate specific wake-up calls while avoiding complex processor-based decision techniques, thereby enabling a reduction in energy-consumption of the node. Looking further into the small-size, low-power comprehensive designs, [13] talks about the development of hardware prototypes of Multimedia sensor nodes for smart farming applications. Furthermore, [13] discusses the benefits of integrating all the required hardware components on a single, compact PCB thereby facilitating the development of sensor nodes with small form factors.

Considering the state-of-the-art in the arena of Wireless Sensor Networks, this article focusses on the VLSI front-end

description of the above-mentioned subsystems and their relevant interfaces. Fig. 1 depicts the proposed architecture of the sensor node. The next section of the article talks about the three major subsystems of the proposed design while Section IV lays down the results by means of simulations and obtained performance metrics.

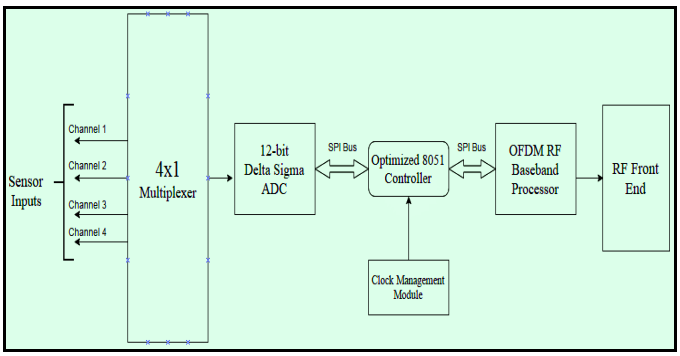

Fig. 1. Proposed Architecture of the Sensor Node.

III. DETAILED DESCRIPTION OF THE PROPOSED DESIGN

A. *The sensor subsystem*

The Analog-to-Digital Converter (ADC) constitutes the primary component of this subsystem tasked with converting the data obtained from the generic sensor modules into their equivalent digital representation and transferring them into the processing subsystem for further operations. The sensor subsystem also consists of an Analog multiplexer (4x1) employed to enable a 4-channel ADC operation in order to facilitate a variety of sensors to be interfaced with the node and thus enhancing the versatility of its application. The 12-bit Delta-Sigma ADC presented in Fig. 2 consists of a Delta-Sigma Modulator and a Digital/Decimation filter. The advantages of the Delta-Sigma ADC include better noise shaping capabilities making it best suited for low-frequency, high-accuracy applications; a high resolution output stream and a wide frequency range of conversion [8].

The Delta-Sigma modulator (DSM) constitutes a Difference Amplifier, an Integrator, a Comparator and a 1-bit DAC. The input to the DSM is a time-varying analog signal from the sensor(s) connected to the sensor subsystem. The DSM is responsible for digitizing the analog input and reducing the noise at low frequencies by pushing the noise to higher frequencies wherein they are removed by the subsequent digital filter stage. The time-varying input and the output of the DAC are differentiated as shown in Fig. 3 and this output is fed into the Integrator whose output possesses either a positive or a negative slope based on the sign and magnitude of its analog input. If the output of the integrator is equal to the reference signal, the comparator output switches (either from positive to negative or from negative to positive) depending on its previous state. The comparator output is progressed onto the Digital/Decimation filter stage along with feeding it back to the 1-bit DAC whose output changes accordingly thereby prompting the integrator output to progress in the opposite direction and hence causing a corresponding switch in the output of the comparator. Thus, the output of the DSM constitutes a pulse-wave representation of the analog input signal at a sampling rate of '*fs*'. This pulsed-representation of the time-varying input is then averaged to obtain a digital equivalent of the analog input. The high speed 1-bit output of the DSM containing noise at higher frequencies is passed through the Digital Filter/Decimator block. The Digital Filter functionality in a low-pass configuration attenuates the high frequency noise while the Decimator functionality slows down the high output data rate. The Digital filter implementation constitutes a weighted averaging filter configuration commonly found in numerous industrial applications [9]. The Decimator reduces the output data rate by discarding redundant data samples in order to bring the output to a more manageable data rate. The parameter of interest in this Digital filter/Decimator configuration is the Decimation Ratio (DR) defined as shown in (1).

$$\text{Decimation Ratio (DR)} = fs/fd \quad (1)$$

where, fs = Delta Sigma Modulator's sampling rate and

fd= Decimator's output data rate.

B. *The processor subsystem*

The processor subsystem is the 'brains' of the sensor node comprising a general-purpose controller tasked with maintaining the data transfer functionalities between the sensor subsystem and the radio transmitter subsystem. Standard SPI Master-Slave interfaces are employed to define data transfer protocols between the concerned subsystems. A conventional 8051-microcontroller core is optimized to incorporate a minimum number of I/Os, SPI Master-Slave interface support, interrupts, pipelining strategies and low-power sleep modes. The 8051-microcontroller core is an advantageous choice for sensor node design primarily because of its smaller program and data space and also because of its smaller physical size [6].

The SPI module forms the interface for data transfer between the sensor subsystem and the radio transmitter subsystem. The Serial Peripheral Interface (SPI) is a de-facto serial synchronous communication interface consisting of a single master driving one or more slaves. The SPI bus constitutes four logic signals namely, Serial Clock (SCLK), Slave Select (SS), Master-Out Slave-In (MOSI) and Master-In Slave-Out (MISO). The design metrics and implementation results are presented in the Section IV of this article.

The Clock Management Unit is another significant part of the node categorized under the processor subsystem. This module constitutes a PLL-based clock distribution logic which is the norm in modern high-performance digital circuits. The implementation details of an All-Digital Phase Locked Loop (ADPLL) are discussed in Section IV of this article.

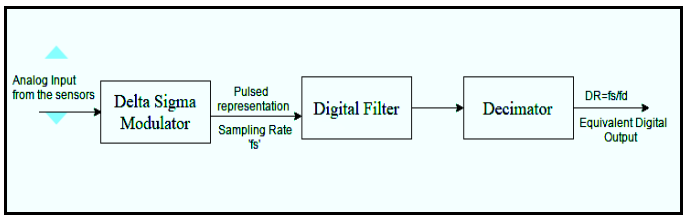

Fig. 2. Block Diagram of the Delta Sigma ADC.

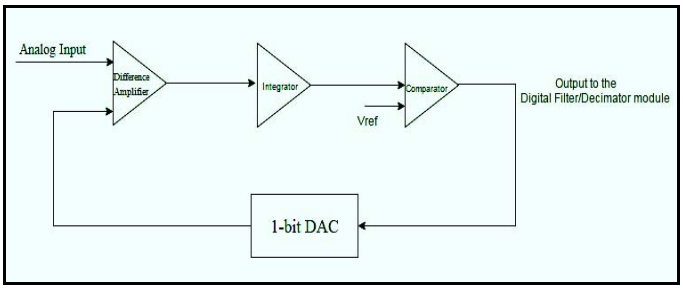

Fig. 3. A First Order Delta Sigma Modulator.

C. The radio transmitter subsystem

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier transmission scheme in which data is carried over several parallel streams by orthogonal sub-carriers, each sub-carrier modulated by conventional modulation schemes such as QAM or QPSK. The wideband channel is divided into overlapping yet orthogonal narrowband sub-channels thereby eliminating the need for guard intervals between the channels and hence rendering OFDM highly spectrally efficient. This orthogonal multicarrier technique offers numerous advantages over conventional single-carrier schemes such as the ability of OFDM systems to cope with Multipath Fading, Inter-Symbol Interference (ISI) and Inter-Carrier Interference (ICI). The sub-carriers are spaces in such a way that they can be easily separated at the receiving end- a boon for the constraint-heavy WSN domain. The first OFDM patent was filed by R. Chang of Bell Labs which proposed an analog implementation employing arrays of signal generators and demodulators [10]. The application of Discrete Fourier Transform (DFT) realized using the WFT or FFT techniques allowed research on the potential applications of OFDM to really take off. A significant amount of research has been dedicated to the VLSI design of OFDM transceiver architectures including numerous FPGA-based generic implementations as presented in [1]. Reference [1] details a flexible OFDM baseband transmitter architecture presented with system modelling, simulation, synthesis and its subsequent mapping onto an FPGA. Similarly, [11] and [12] talk about the FPGA-based implementation of an OFDM digital baseband transmitter. However, we present the OFDM baseband strategy in the perspective of sensor nodes and their application in Industrial Wireless Sensor Networks (IWSNs). Looking into environments similar to IWSNs, [14] lays down the design of a high-speed OFDM modem for high-speed underwater acoustic communications. The use of OFDM enables high-speed reliable communication capabilities making it highly suitable for numerous aquatic applications as detailed in [14].

In the OFDM transmitter subsystem (as shown in Fig. 4), the input data stream is Serial to Parallel converted onto M subcarriers which are independently modulated using QPSK (or 16QAM). These M-modulated sub-carriers are the inputs to the N-point IFFT module to generate N-complex time-domain samples. The output of the IFFT block is fed to a Cyclic Prefix module in order to add a guard band at the starting point of each OFDM symbol to mitigate any residual impact of Inter-Symbol Interference that may arise due to Multi-Path propagation. These parallel data streams are then converted to a serial output stream for propagation into the RF front-end. The design description and simulation results of the OFDM-baseband processing of the data stream are depicted in the next section of the paper.

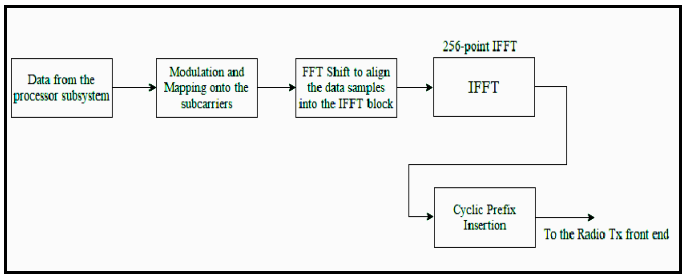

Fig. 4. Architecture of the OFDM Baseband Processor.

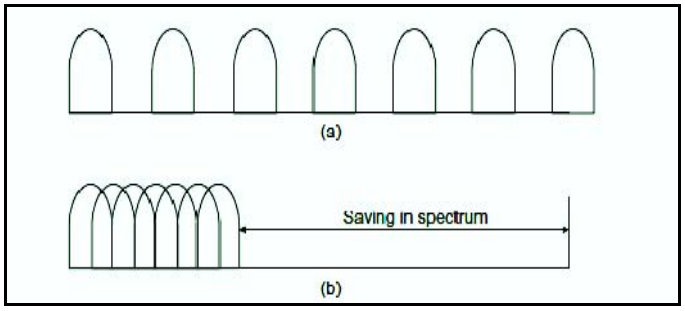

Fig. 5. Spectral Efficiency of OFDM (*b*) as opposed to conventional multicarrier modulation (*a*).

In OFDM, as hinted at earlier, the frequency-selective wideband channel is divided into non-frequency selective narrowband sub-channels. These sub-channels are overlapping and orthogonal, which removes the need for guard bands, thereby making it spectrally efficient when compared to conventional multi-carrier techniques, as portrayed in Fig. 5. High data rate streams typically encounter problems of ISI because the symbol duration '*Ts*' is smaller than the channel delay spread '*Td*'. The presence of ISI calls in the need for complex equalization procedures at the receiving end. Moreover, the complexity of the equalization process at the receiver increases with the square of the channel impulse response length. In order to mitigate ISI and the subsequent receiver equalization complexity, the high data rate stream is Serial-to-Parallel converted onto M subcarriers. This process ensures that the symbol duration on each subcarrier is much greater than the channel delay spread, i.e. $Ts>Td$, thereby simplifying the receiver implementation. The mathematical representation of processes involved in the OFDM RF Tx subsystem are detailed below.

The M parallel data streams of the input serial high data rate stream are defined as shown in (2).

$$S[k] = [S_0[k], S_1[k], S_2[k]....., S_{M-1}[k]]^T \quad (2)$$

$$X[k] = [X_0[k], X_1[k], X_2[k]....., X_{M-1}[k]]^T \quad (3)$$

$$x[k] = [x_0[k], x_1[k], x_2[k]....., x_{N-1}[k]]^T \quad (4)$$

where, 'k' is the index of the OFDM symbol.

These M parallel data streams are independently modulated using QPSK (Quadrature Phase Shift Keying) resulting in a complex vector defined as shown in (3). The vector depicted in (3) is then subjected to N-point IFFT processing (256-point IFFT in the architecture presented in this paper) which results in a vector of N complex time-domain samples as shown in (4). Cyclic prefix addition forms the next crucial operation in a typical OFDM system which includes copying the last 'G' samples of the Inverse FFT output and adding them to the beginning of $x[k]$. The purpose of doing this is to mitigate any remaining impacts of ISI due to multipath propagation (Fading due to the reception of signals from a variety of paths in any typical terrestrial environment).

At the receiver, the inverse procedures are carried out subject to time and frequency synchronization in order to optimally recover the 'message' signal (data stream from the controller subsystem). The FFT-IFFT algorithmic pair incorporated in OFDM is a faster and a simpler alternative to computing the DFTs or IDFTs directly. If $x_0, x_1, x_2, \ldots\ldots, x_{N-1}$ is a complex time domain sequence, the Discrete Fourier Transform (DFT) is given by (5) and intuitively it's inverse: the Inverse Discrete Fourier Transform (IDFT) is depicted in (6).

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi nk/N}, \text{ for } k=0 \text{ to } N-1 \quad (5)$$

$$x_n = \sum_{k=0}^{N-1} X_k e^{j2\pi nk/N}, \text{ for } n=0 \text{ to } N-1 \quad (6)$$

We can deduce from (5) and (6) that the direct computation of DFT/IDFT is slow and laborious. FFT-IFFT bring down the complexity of computing DFT from $O(n^2)$ to O(nlog n). Hence, computerized implementations where speed and processing power are of primary importance, incorporate FFT and IFFT-based approaches of DFT computation.

IV. Results and Discussions

The architecture presented in this article encompasses a comprehensive modular design methodology with the entire system divided into three major subsystems. The sensor subsystem constituting a 4-channel 12-bit Delta Sigma ADC is described using Verilog AMS in the Cadence AMS Design suite (Cadence Virtuoso design environment and Spectre simulator). The simulation results of the sensor subsystem are depicted in Fig. 6 and Fig. 7. The processor subsystem architectural metrics are portrayed in Fig. 8. The general-purpose controller configuration is described in Verilog HDL and the corresponding simulation results are presented in Fig. 9 and Fig. 10.

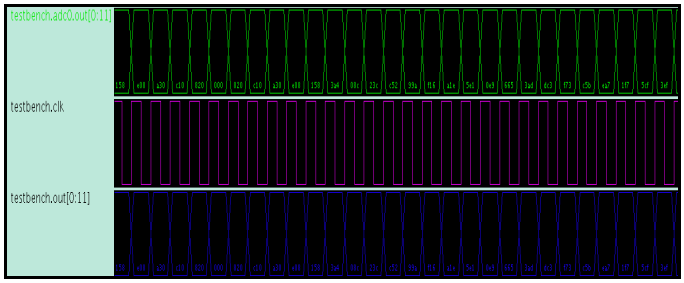

Fig. 6. Simulation results of the ADC subsystem (*12-bit Output of the ADC*).

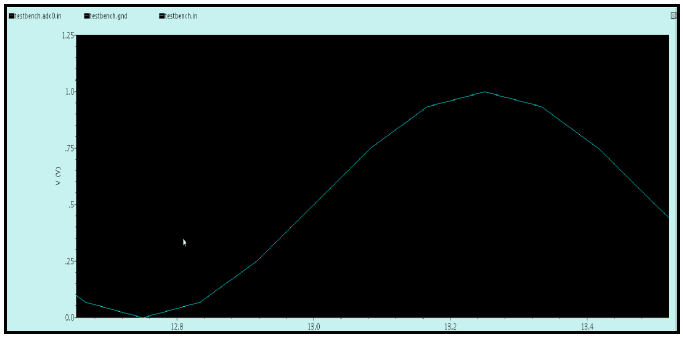

Fig. 7. Simulation results of the ADC subsystem (*Analog input*)

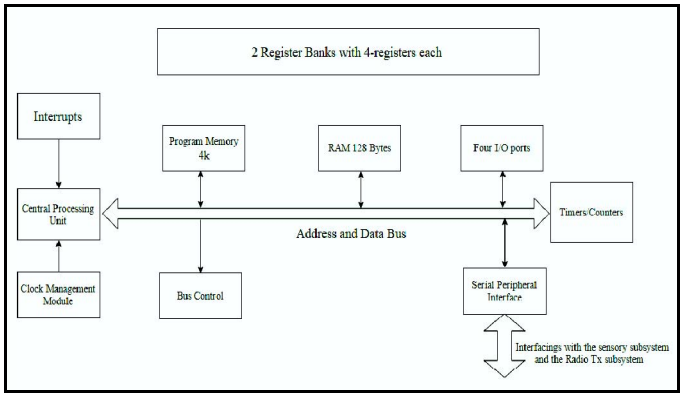

Fig. 8. An 8051-controller based processing subsystem.

The radio transmitter subsystem consists of an OFDM based baseband processor employing QPSK modulation schemes and a 256 point IFFT module described in Verilog HDL. The RTL description of the design is simulated for functional verification. Prior to the actual hardware description of the radio transmitter subsystem, the design is modelled in Matlab and Simulink for the validation of the functional correctness of the chosen parameters. The corresponding results are depicted in Fig. 11.

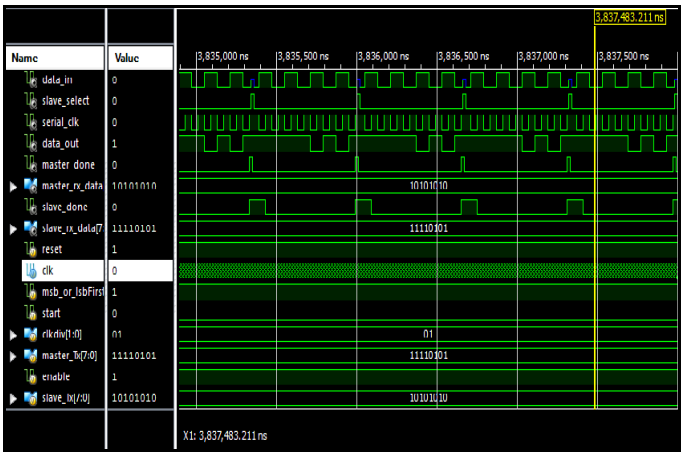

Fig. 9. Simulation results of the SPI Master-Slave module.

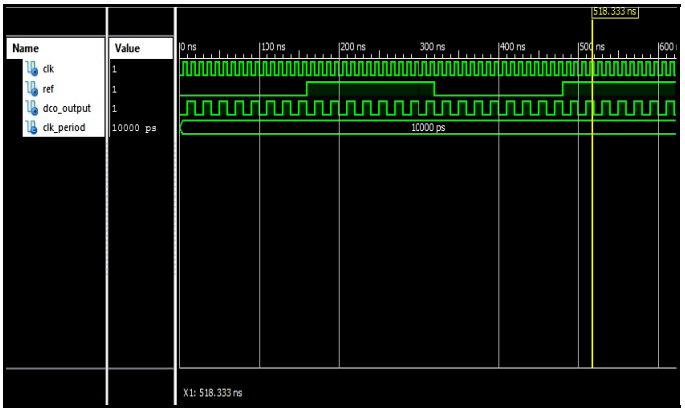

Fig. 10. Simulation results of the Clock Management module.

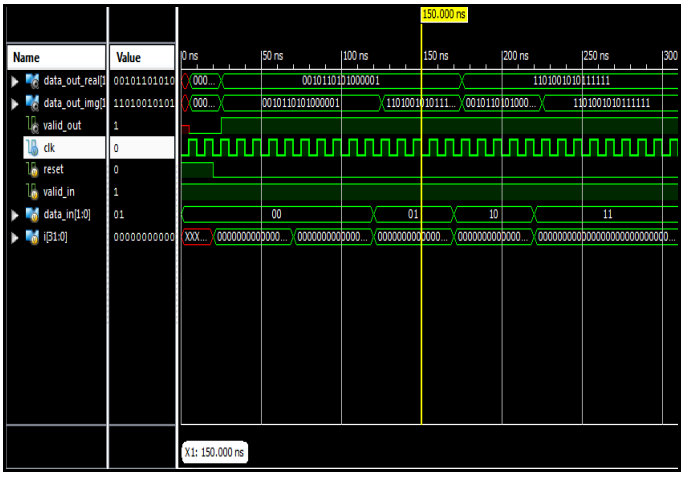

Fig. 11. Simulation results of the QPSK constellation mapping block.

V. Conclusion

The proposed architecture of a sensor node for application in Industrial Wireless Sensor Networks (IWSNs) constitutes three major subsystems: a sensor subsystem, a processor subsystem and a radio transmitter subsystem. The optimized 8051 controller core serves as the general-purpose processor coupled with SPI Master-Slave interfaces with the other two subsystems. The sensor subsystem constitutes a four channel 12-bit Delta-Sigma ADC allowing interfaces with a variety of sensors employed to monitor key parameters in the industrial ecosystem. The radio transmitter subsystem consists of an OFDM baseband processor providing numerous advantages over other communication strategies, as described in Section III of this article. Future works on the system include the design of the RF front end, System Verilog based Verification, Synthesis, Physical Design and more importantly enabling energy efficiency of the node through system-level strategies facilitating reduced energy consumption.

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