CMOS INVERTER DESIGN USING CADENCE VIRTUOSO

Tool Used : Cadence virtuoso

Technology Library : gpdk180nm

1.Theory:

A CMOS inverter is a basic building block in digital electronics, particularly in complementary metal-oxide-semiconductor (CMOS) technology. It is a logic gate that implements the NOT function, meaning it inverts the input signal.

1.1 Structure

A CMOS inverter consists of two MOSFETs:

1. PMOS (P-channel MOSFET): Connected to the power supply (VDD).
2. NMOS (N-channel MOSFET): Connected to ground (VSS).

These two transistors are connected in series:

- The drain of the PMOS is connected to the drain of the NMOS.
- The source of the PMOS is connected to VDD, and the source of the NMOS is connected to ground.

The input signal is applied to the gates of both transistors simultaneously.

1.2 Operation Modes:

The CMOS inverter operates in different modes depending on the input voltage (VIN):

- Case 1: VIN = 0V (Logic 0)
  - PMOS Transistor: Gate-source voltage VGS is negative (since VIN is 0), so the PMOS is in saturation mode and fully on, connecting the output to VDD .
  - NMOS Transistor: Gate-source voltage VGS is 0, so the NMOS is off, disconnecting the output from ground.
  - Output: The output voltage VOUT is pulled up to VDD_{DD}DD, representing a logic 1.
- Case 2: VIN = VDD (Logic 1)
  - PMOS Transistor: VGS is 0, so the PMOS is off, disconnecting the output from VDD .

- NMOS Transistor: VGS is positive, so the NMOS is fully on, connecting the output to ground.
- Output: The output voltage VOUT is pulled down to 0V, representing a logic 0.

1.3 Voltage Transfer Characteristics (VTC):

The voltage transfer characteristic (VTC) of a CMOS inverter shows the relationship between the input voltage (VIN) and the output voltage (VOUT):

- Regions of Operation:
  1. Cutoff Region: Both transistors are off. This occurs when the input is slightly above 0 but below the threshold voltage of the NMOS.
  2. Transition Region: The input voltage is in a range where both transistors are partially on. The output switches from high to low. This region is where the inverter's gain is high.
  3. Saturation Region: Either the NMOS or PMOS is fully on while the other is fully off. The output is either VDD or 0V.

1.4 Static and Dynamic Behavior:

- Static Power Dissipation: Ideally, CMOS inverters dissipate almost no power when in a steady state (either logic 0 or 1) because one transistor is always off. Power is only consumed during the transition between states due to the brief overlap of both transistors conducting, causing a short current spike.
- Dynamic Power Dissipation: Occurs due to charging and discharging the capacitance at the output node during transitions. This is the primary source of power consumption in CMOS circuits.

1.5. Noise Margins:

CMOS inverters have high noise margins, which measure the tolerance to noise in both the high and low logic levels. The noise margin is derived from the VTC and indicates how much noise the circuit can handle without affecting the logic levels.

1.6. Propagation Delay:

The delay between the change in input and the resulting change in output is known as the propagation delay. It is influenced by factors like load capacitance, transistor sizes, and supply voltage. Lower delays are crucial for high-speed digital circuits.

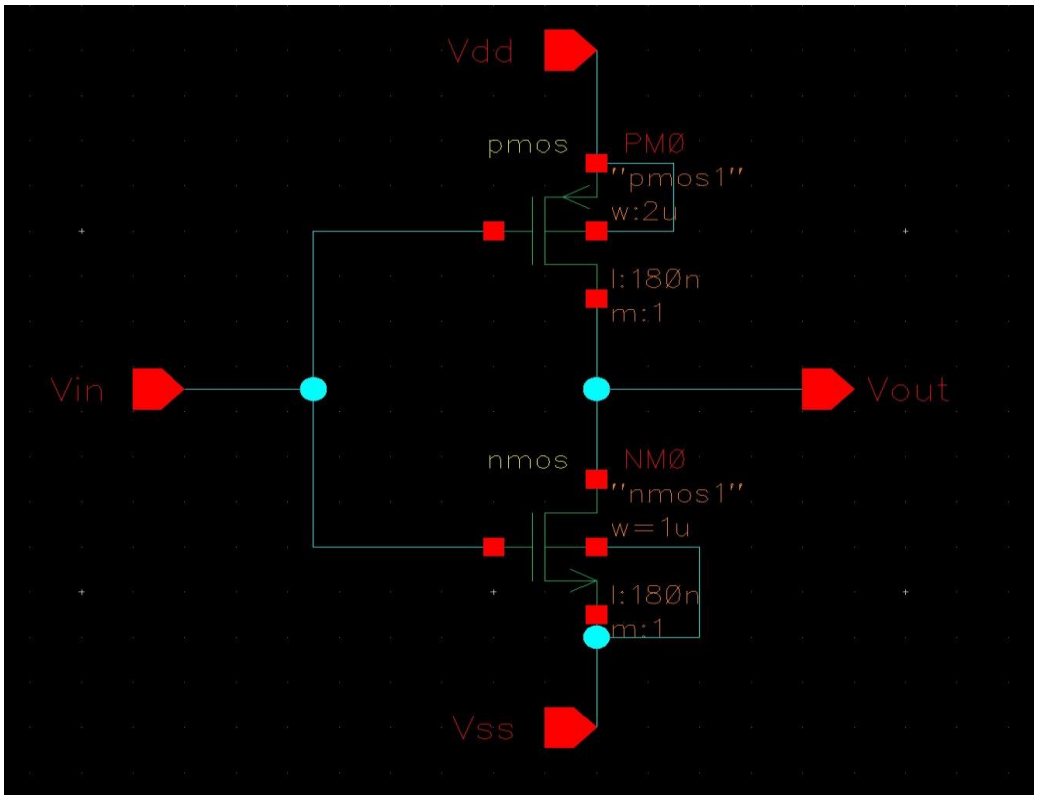
1.7 Applications:

CMOS inverters are fundamental in creating more complex logic gates and circuits, such as NAND, NOR, and flip-flops. They are used in almost all digital electronic devices, including microprocessors, memory chips, and integrated circuits (ICs).

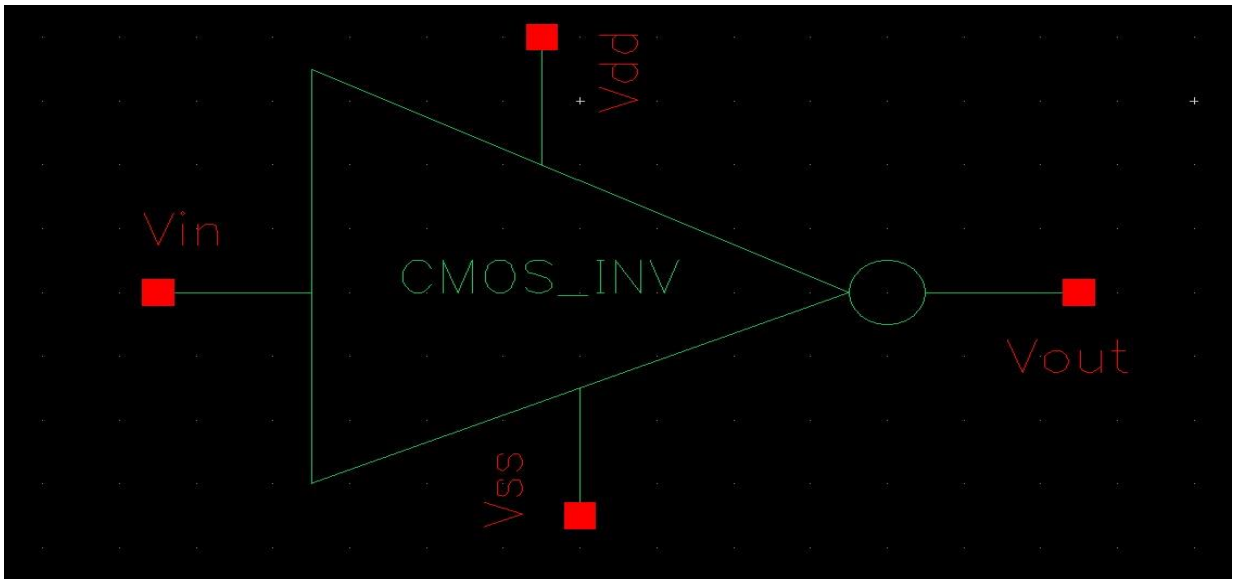
2. Simulation in Cadence Virtuoso:

- Step 1: Open the Cadence Virtuoso Design tool.
- Step 2: Create a new library using the CIW window (File -> New -> Library). Attach this library to the gpdk180nm technology node, or any other technology node.
- Step 3: Create a new cell view using the library manager window (File -> New -> Cell View).
- Step 4: Start placing the components from the built-in analoglib component library. Components in the schematic:
    - NMOS [nmos2v] (gpdk180)
    - PMOS [pmos2v] (gpdk180)
    - Voltage source VDD [vdd] = 1.8V (analoglib)
    - Voltage source Vin [vin] = 0.9V DC + 1mV 1KHz SineWave or Square wave(analoglib)
    - Ground [gnd] (analoglib)

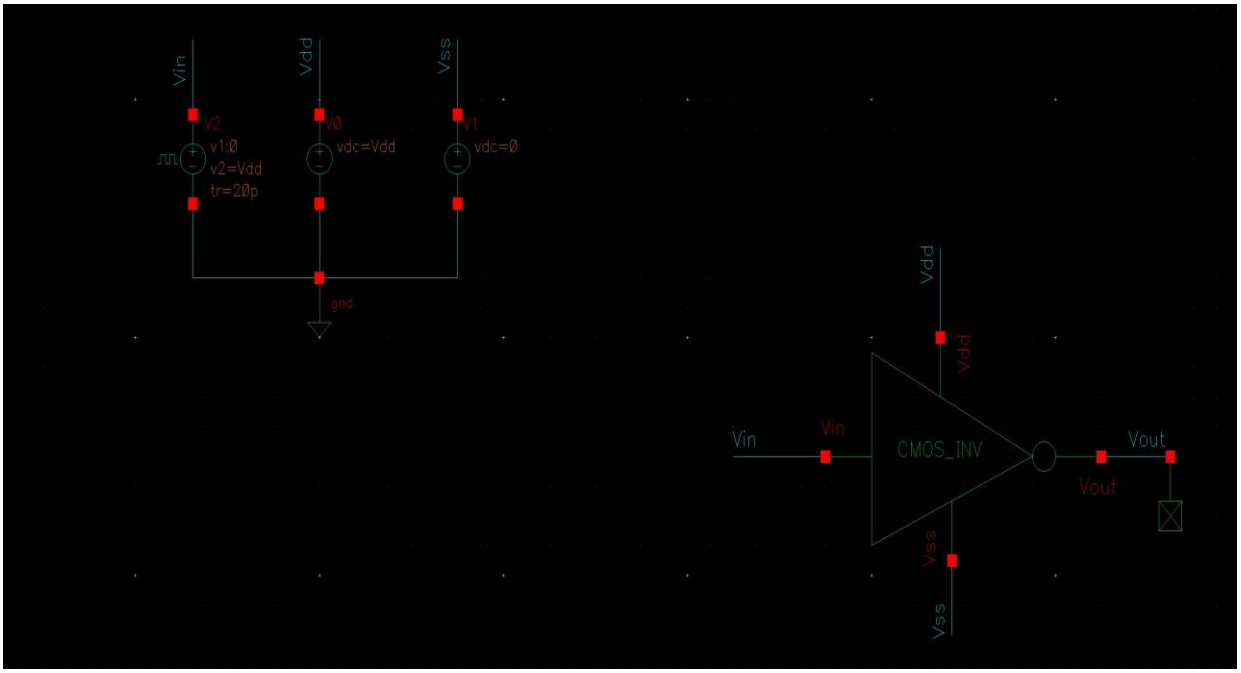
▪ Create a schematic of CMOS Inverter:



- Create a symbol of CMOS Inverter :



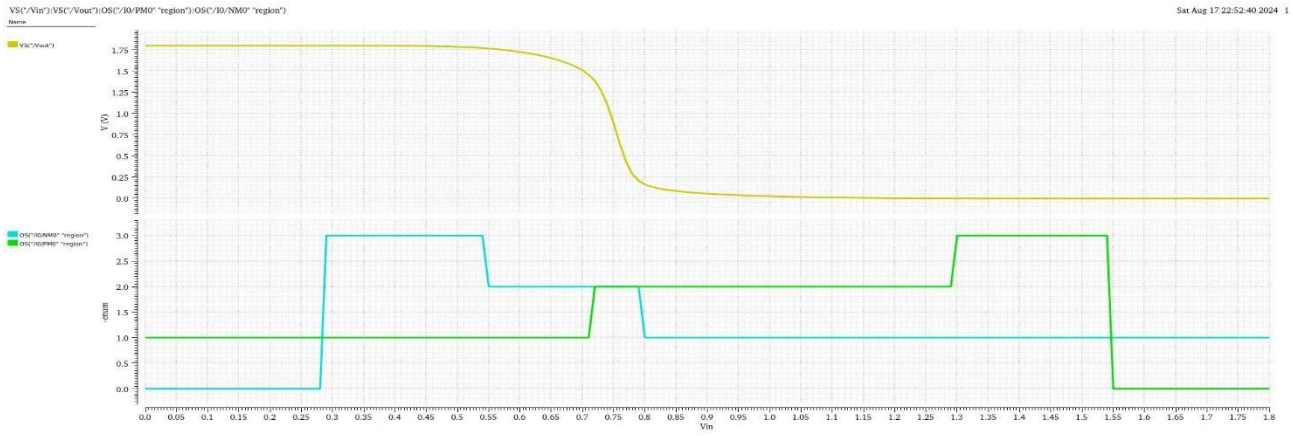
- Create a Test bench using symbol



3.Simulation Result:

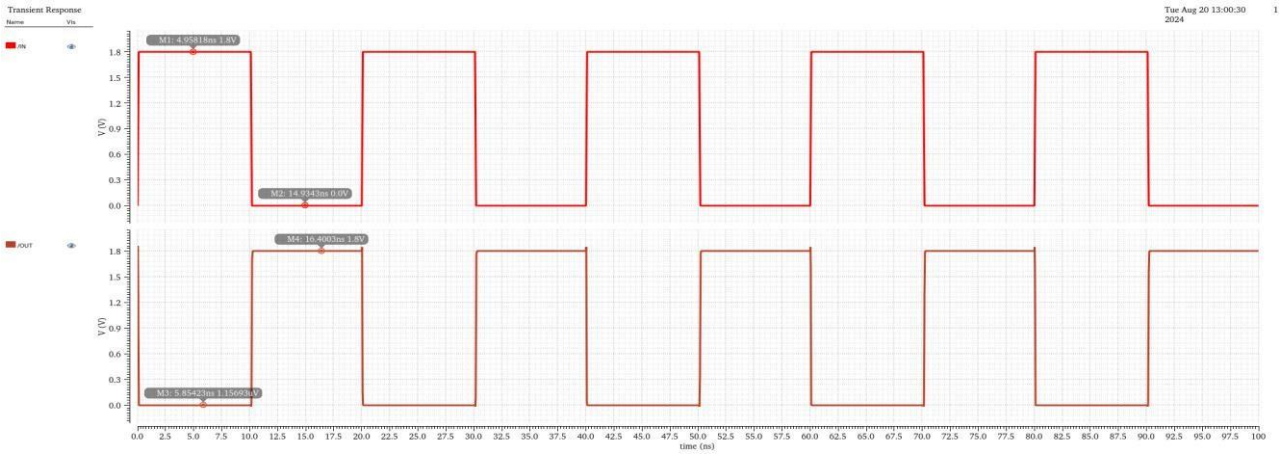
3.1 DC Analysis:

- VTC (voltage transfer characteristics) & Region of PMOS NMOS



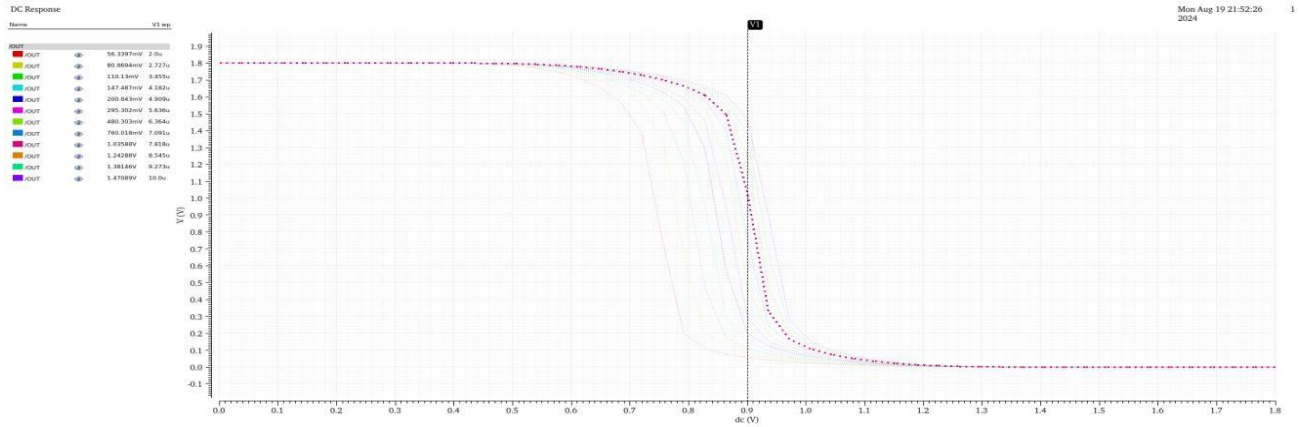
3.2 Transient Analysis:

Transient simulation [0-100ns] (VinDC = 1.8V, Pulse input Period = 20ns, Rise & Fall time = 20ps; Pulse width= 10n):



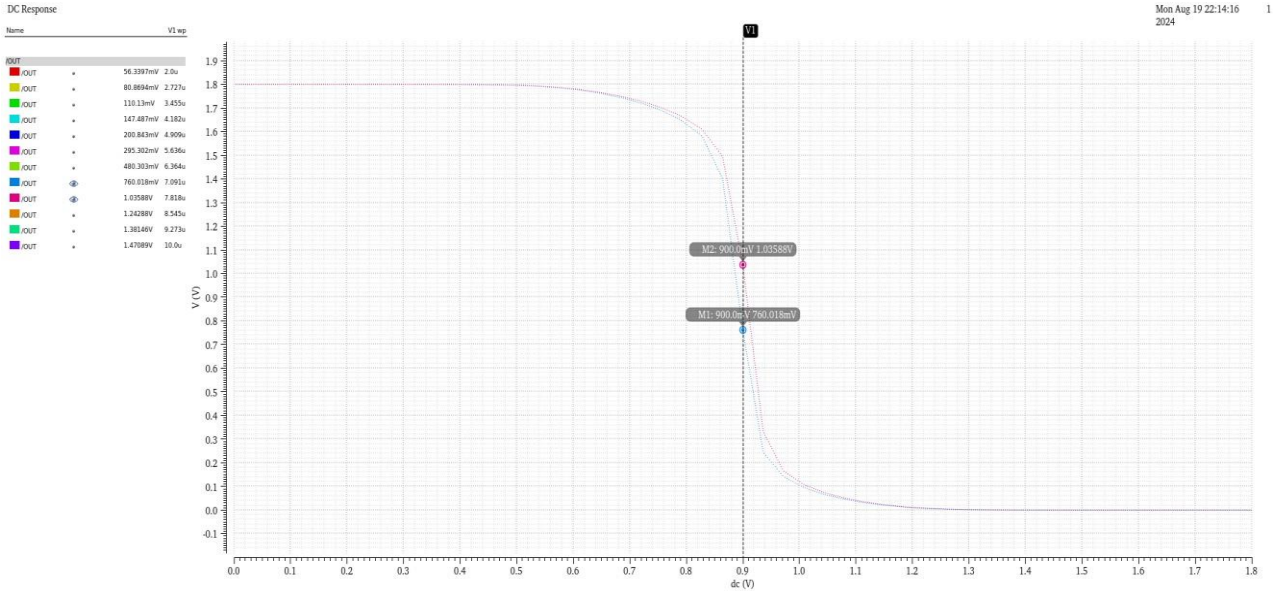
3.3 Switching Threshold:

Switching Threshold to obtain midpoint voltage (Vin=Vout=Vdd/2)

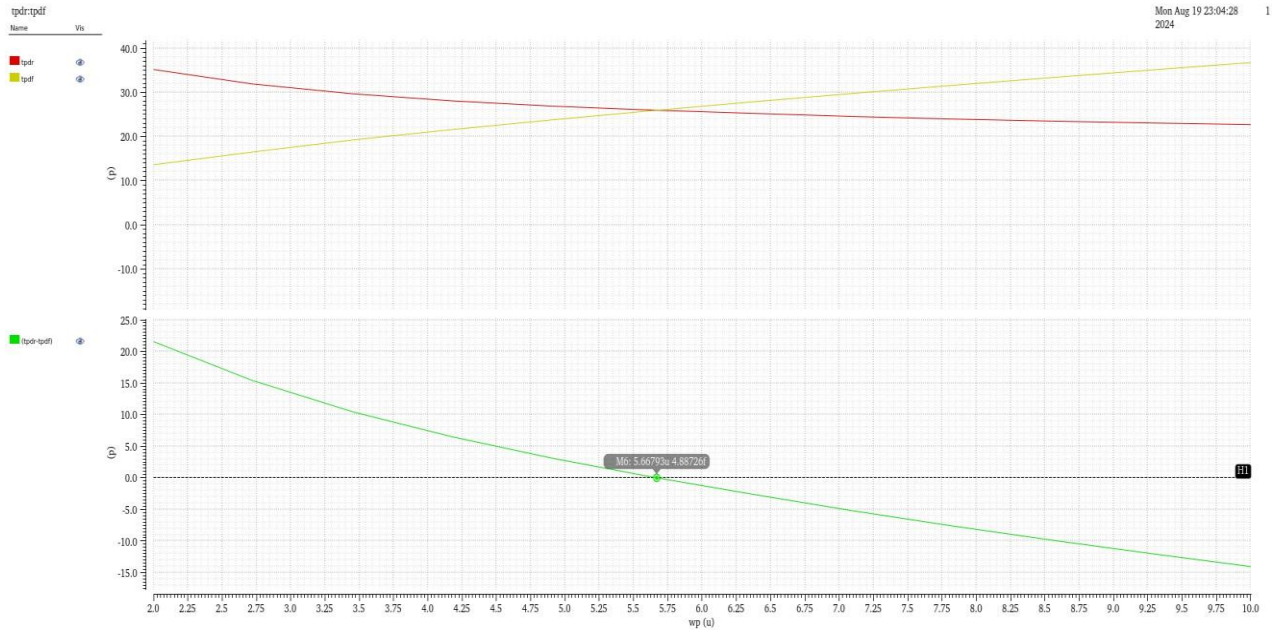


Obtaining proper sizing of the transistor with the help of switching threshold analysis

At Vin=Vout=Vdd/2 the PMOS size is Wp=7.476µm & NMOS size is Wn=2µm



3.4 Rise time & Fall time:



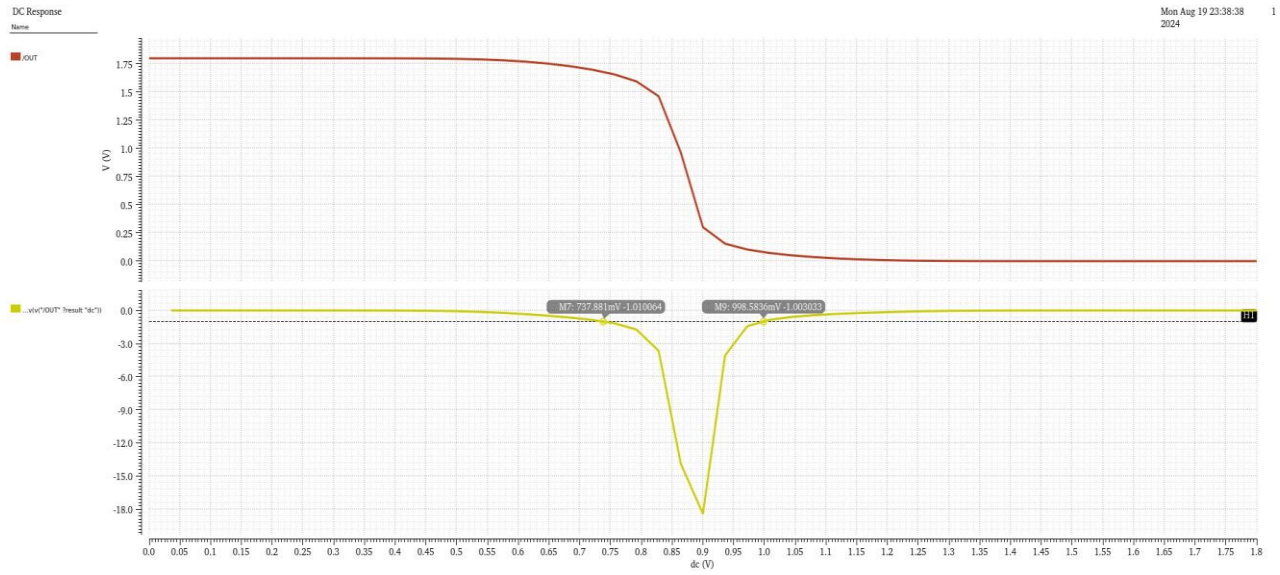
To obtain the proper sizing of the transistor rise time and fall time must be equal.

From the plot, Tplh=Tphl=25.94 psec at which PMOS size Wp=5.6693µm

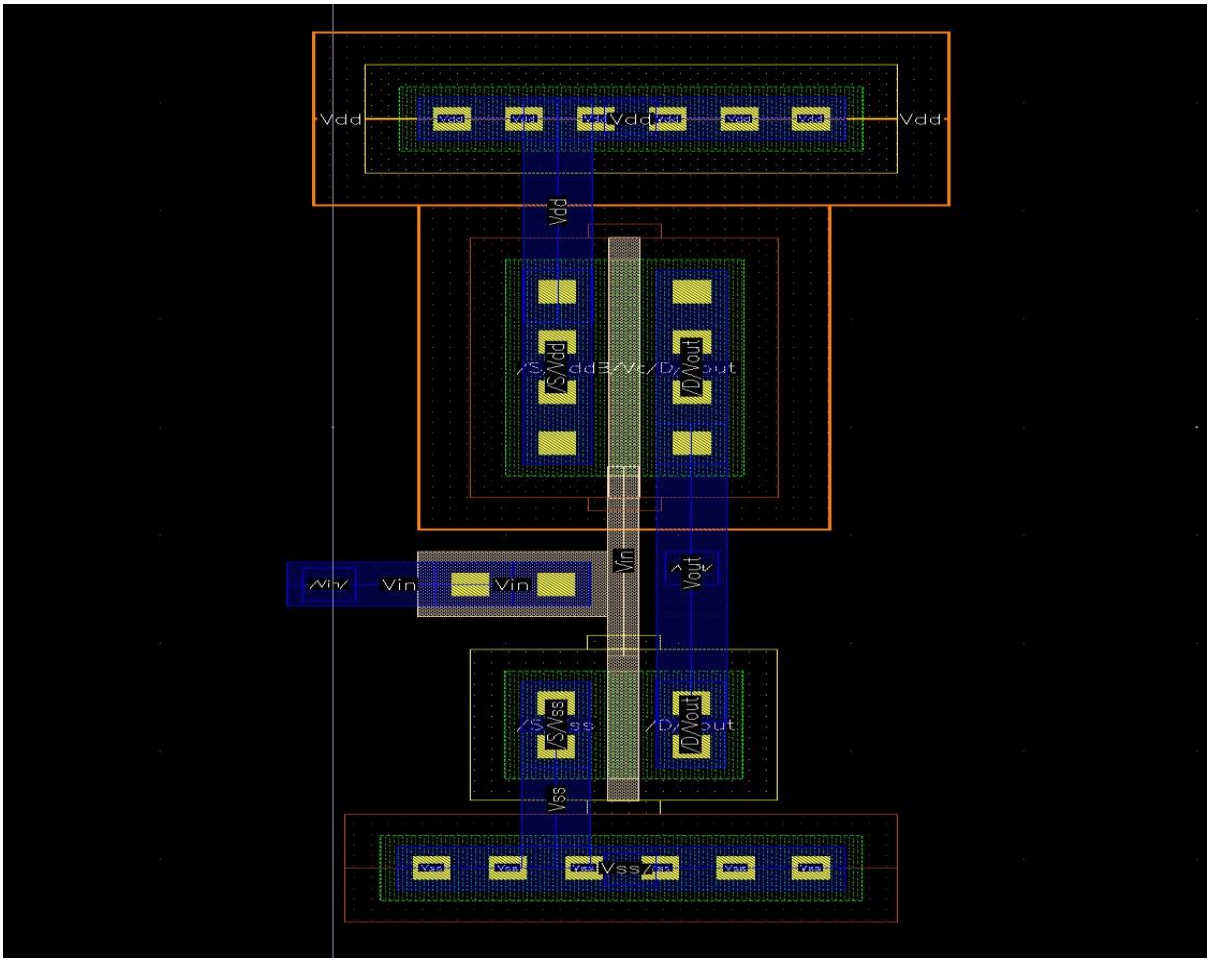
3.5 Noise Margin:

$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$, $NM_L = V_{IL} - V_{OL} = V_{IL}$

$NM_H = 1.8 - V_{IH}$ = 1.8v – 998.6mv = 0.801v , $NM_L = V_{IL}$ = 737.88mv



3.6 Layout:



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