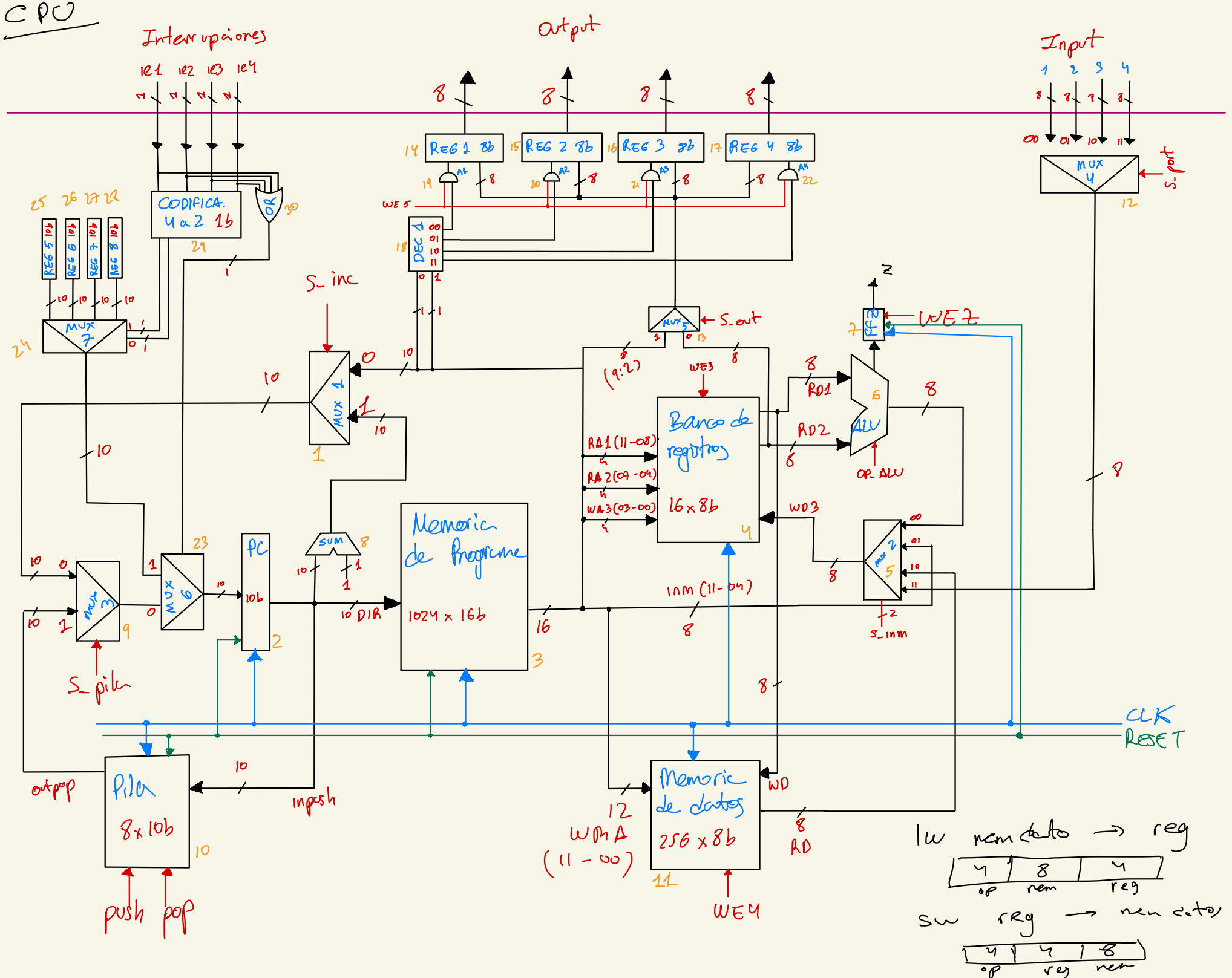
CPU
Interrupciones
int1 int2 int3 int4
Output
Input
REG 1 8b
REG 2 8b
REG 3 8b
REG 4 8b
CODIFICA. 4 a 2 1b
OR
DEC 1
WE 5
MUX 4
S_port
REG 5 10b
REG 6 10b
REG 7 10b
REG 8 10b
MUX 7
S_inc
MUX 1
S_out
MUX 5
WE7
FF
Banco de registros
16 x 8b
RA1 (11-08)
RA2 (07-04)
WA3 (03-00)
RD1
RD2
WD3
WE3
ALU
OP_ALU
Memoria de Programa
1024 x 16b
PC
SUM
MUX 3
MUX 6
S_pila
DIR
inm (11-04)
MUX 2
S_inm
Pila
8 x 10b
outpop
inpush
push
pop
Memoria de datos
256 x 8b
WD
RD
WMA (11-00)
WE4
CLK
RESET
lw rem dato → reg
op rem reg
sw reg → rem dato
op reg rem