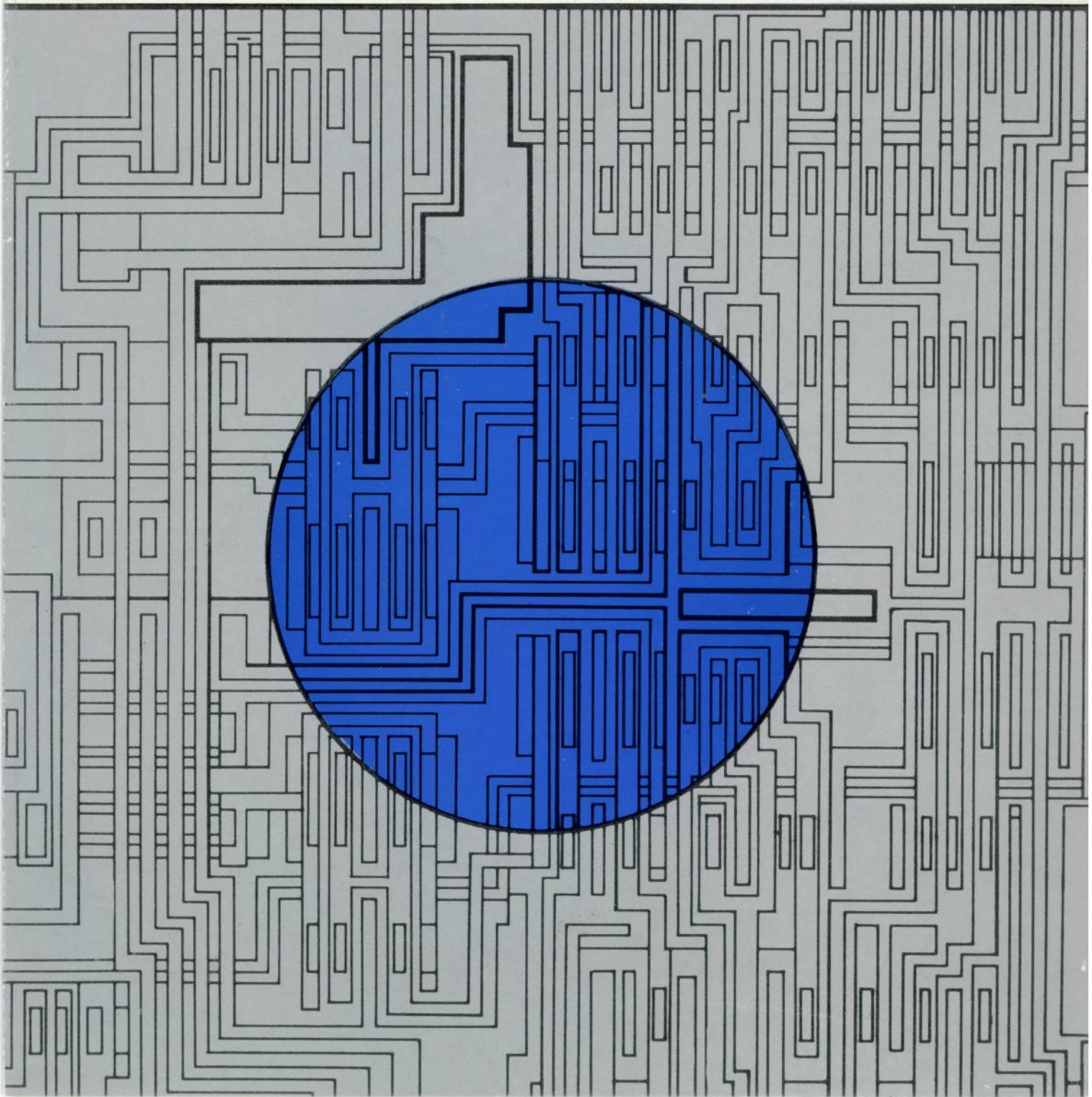


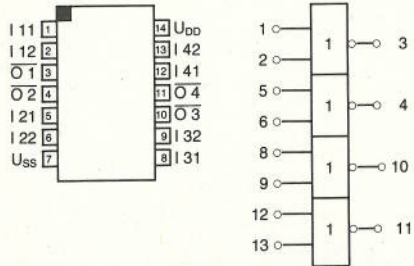
Übersicht CMOS-Schaltkreise CMOS-IC's



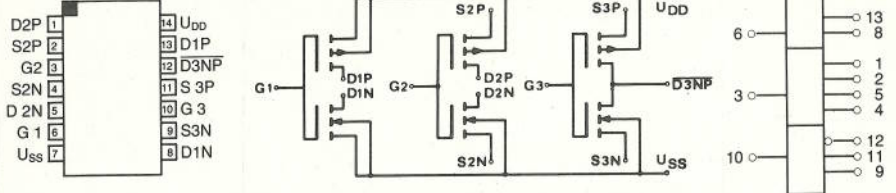
Übersicht CMOS-Schaltkreise – CMOS-IC's

V 4001 D	4 NOR-Gatter mit je 2 Eingängen	quadruple 2-input NOR gates
V 4007 D	2 Transistorpaare und 1 Inverter	2 transistor pairs and 1 inverter
V 4011 D	4 NAND-Gatter mit je 2 Eingängen	quadruple 2-input NAND gates
V 4012 D	2 NAND-Gatter mit je 4 Eingängen	dual 4-input NAND gates
V 4013 D	2 x D-Flip-Flop	dual 'D'-Type flip-flop
V 4015 D	2 x 4bit Schieberegister	dual 4-bit shift register
V 4017 D	Dekadischer Zähler mit 10 dekodierten Ausgängen	decade counter with 10 decoded outputs
V 4019 D	4 AND/OR-Auswahlgatter	4 AND/OR selection gates
V 4023 D	3 NAND-Gatter mit je 3 Eingängen	triple 3-input NAND-gates
V 4027 D	2 Master-Slave-JK-Flip-Flop	dual Master-slave-JK-flip-flop
V 4028 D	BCD-zu-Dezimal-Dekoder	BCD-to-decimal decoder
V 4029 D	Synchroner 4stufiger binärer/BCD-Vor-/Rückwärtszähler mit Voreinstellung	synchronous 4-digit binary/BCD-forwards/backwards counter with pre-set control
V 4030 D	4 Exklusiv-OR-Gatter mit je 2 Eingängen	quadruple 2-input exclusive OR gates
V 4034 D	8stufiges bidirektionales paralleles/serielles Busregister	8-stage, bi-directional, parallel/serial bus register
V 4035 D	4bit Schieberegister mit synchroner Paralleleingabe	4-bit shift register with synchronous parallel input
V 4042 D	4bit Auffangregister	4-bit latch
V 4044 D	4 RS-Flip-Flop	4 RS-flip-flop
V 4046 D	PLL-Schaltung (Phasenregelkreis)	phase-locked-loop
V 4048 D	Multifunktionsgatter	multi-function gate
V 4050 D	6 nichtinvertierende Treiberstufen	six not inverting drivers
V 4051 D	8-Kanal-Analog-Multiplexer/Demultiplexer	analog multiplexers/demultiplexers
V 4066 D	4 bilaterale Analogschalter	quad bilateral switch
V 4093 D	4 NAND-Gatter mit je 2 Eingängen mit Schmitt-Trigger-Verhalten	quadruple 2-input NAND Schmitt-triggers
V 40098 D	6 invertierende Treiber mit Tri-state-Ausgängen	six inverter-drivers with tri state outputs
V 40511 D	BCD-zu-7 Segment-Dekoder	BCD to 7 segment decoder
V 4520 D	2 binäre 4bit Vorwärtszähler	dual binary up-counter
V 4531 D	13bit Paritätsprüfer	13-bit parity tree
V 4538 D	2 x Monoflop	dual precision monostable multivibrator
V 4585 D	4bit Größenkomparator	4-bit magnitude comparator

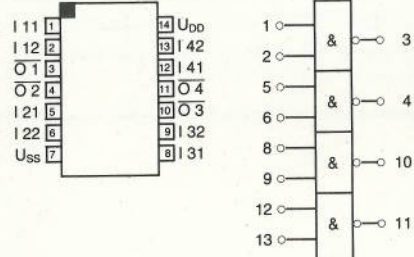
V 4001 D 4 NOR-Gatter mit je 2 Eingängen



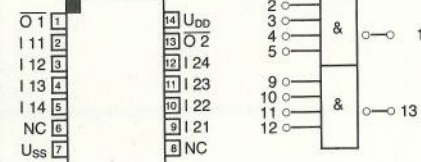
V 4007 D 2 Transistorpaare und 1 Inverter



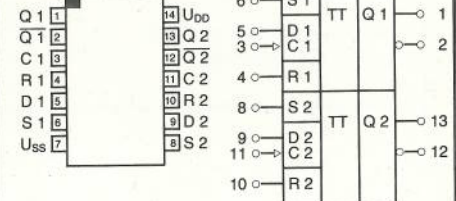
V 4011 D 4 NAND-Gatter mit je 2 Eingängen



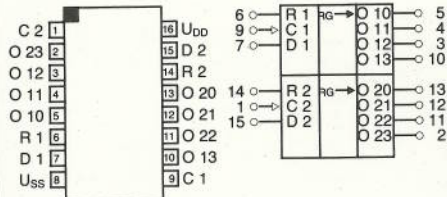
V 4012 D 2 NAND-Gatter mit je 4 Eingängen



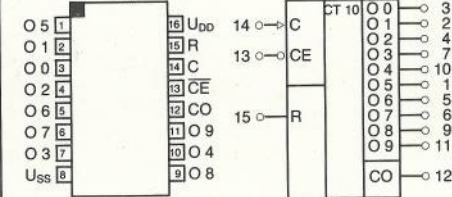
V 4013 D 2x D-Flip-Flop



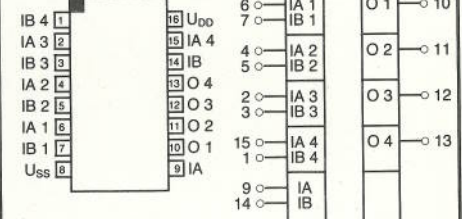
V 4015 D 2x 4bit Schieberegister



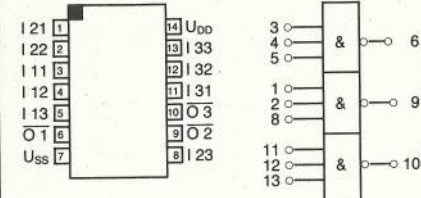
V 4017 D Dekadischer Zähler mit 10 dekodierten Ausgängen



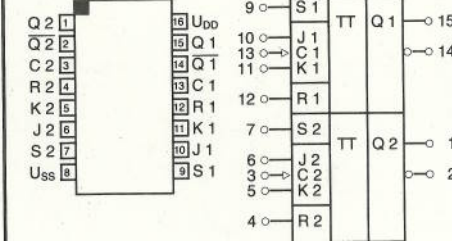
V 4019 D 4 AND/OR-Auswahlgatter



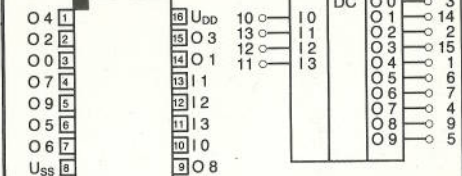
V 4023 D 3 NAND-Gatter mit je 3 Eingängen



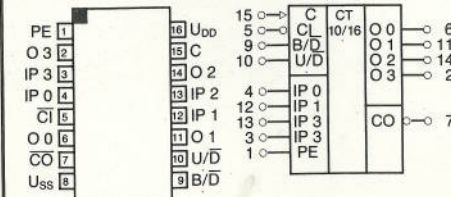
V 4027 D 2x JK-Flip-Flop



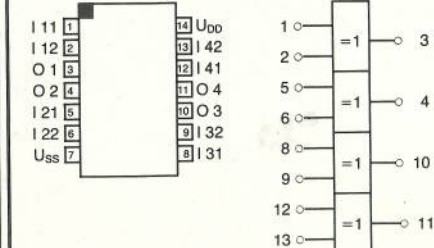
V 4028 D BCD/Dezimal-Dekoder



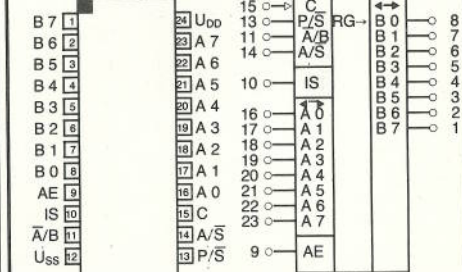
V 4029 D Synchrone 4stelliger binärer/BCD-Vor-/Rückwärts-zähler



V 4030 D 4 Exklusiv-OR-Gatter mit je 2 Eingängen



V 4034 D 8stufiges bidirektionales paralleles/serielles Busregister



Pin diagram of the 74VHC04 hex inverters. The chip has 14 pins. Pin 1 is GND, Pin 14 is VDD. Pins 2, 4, 6, 8, 10, 12 are inputs. Pins 3, 5, 7, 9, 11, 13 are outputs. The internal logic consists of six inverters, each with a propagation delay of 15 ns. The output of each inverter is labeled with a number 1 through 6.

Pin diagram of the 74VHC04 hex inverters. The diagram shows a 16-pin package with pins 1 through 16. Pins 1, 4, and 8 are VDD (power supply). Pins 2, 5, and 9 are VSS (ground). Pins 3, 6, and 10 are inputs. Pins 7, 11, and 14 are outputs. The diagram shows the internal logic of the inverters, with each input pin connected to an inverter circuit. The output of each inverter is connected to the input of the next inverter in the chain. The diagram is labeled with pin numbers and logic symbols.

Pinout diagram for the 74VHC04 hex inverters. The diagram shows a 14-pin package with pins 1 through 8 on the left and pins 16 through 9 on the right. Pin 16 is labeled U_{DD}, pin 15 is S₄, pin 14 is R₄, pin 13 is Q₁, pin 12 is R₃, pin 11 is S₃, pin 10 is Q₃, and pin 9 is Q₂. On the right side, pins 4, 3, 6, 7, 12, 11, 14, 15, and 5 are labeled R₁, S₁, R₂, S₂, R₃, S₃, R₄, S₄, and Q_E respectively. A 'T' symbol is placed between the two columns of pins. On the far right, there are four output pins labeled Q₁, Q₂, Q₃, and Q₄ with their respective logic levels (13, 9, 10, 1).

Pin diagram of the 74VHC04 hex inverters. The chip has 14 pins. Pins 1, 2, 3, 4, 5, 6, 7, 8 are on the left side, and pins 16, 15, 14, 13, 12, 11, 10, 9 are on the right side. Pin 14 is VDD, pin 9 is Uss, and pin 16 is UDD. Pins 1, 2, 3, 4, 5, 6, 7, 8 are labeled PCP 1, PCP 1, IC, OV, VE, CX 1, CX 2, Uss. Pins 16, 15, 14, 13, 12, 11, 10, 9 are labeled UDD, IZ, IS, PCP2, RX 2, RX 1, DEM, IV. Pins 14, 13, 12, 11, 10, 9 are also labeled IS, IC, IV, CX 1, CX 2, RX 1, RX 2, IZ, VE. Pins 1, 2, 3, 4, 5, 6, 7, 8 are also labeled PCP1, PCP2, PCP, OV, DEM. Pins 14, 13, 12, 11, 10, 9 are also labeled PLL, PCP1, PCP2, PCP, OV, DEM.

Pinout diagram for the 74VHC04 hex inverters. The diagram shows a 14-pin package with pins 1 through 14. Pins 1, 2, 3, 4, 5, and 6 are on the left side, and pins 14, 13, 12, 11, 10, and 9 are on the right side. The pins are labeled as follows: Pin 1: U_{DD} , Pin 2: O1, Pin 3: I1, Pin 4: O2, Pin 5: I2, Pin 6: O3, Pin 7: I3, Pin 8: U_{SS} , Pin 9: 14, Pin 10: O4, Pin 11: I5, Pin 12: O5, Pin 13: I6, Pin 14: NC. The diagram also shows the internal logic structure of the inverters, with each input pin connected to an inverter symbol.

Pin diagram of the 74VHC04 hex inverters. The diagram shows a 14-pin package with pins 1 through 7 on the left and pins 14 through 8 on the right. The left side has inputs Y0, Z0, Z1, Y1, X1, X2, and Uss. The right side has outputs SW, SW, SW, SW, SW, and SW, with corresponding inputs X0, X1, X2, X3, and Z0, Z1, Z2, Z3. Pin 14 is labeled UDD and pin 8 is labeled Y2.

Pin diagram of the 74VHC04 hex inverters. The diagram shows a 14-pin package with pins 1 through 14. Pins 1, 2, 3, 4, 5, and 6 are inputs, and pins 7, 8, 9, 10, 11, and 12 are outputs. Pins 13 and 14 are VDD and VSS respectively. The diagram shows the internal logic of the inverters, with each input pin connected to an inverter circuit. The output of each inverter is connected to the next input pin, forming a chain of inverters. The output of the last inverter is connected to pin 12. The diagram also shows the internal logic of the inverters, with each input pin connected to an inverter circuit. The output of each inverter is connected to the next input pin, forming a chain of inverters. The output of the last inverter is connected to pin 12.

Pin diagram of the 74VHC04 hex inverters. The diagram shows two 14-pin packages. The left package has pins 1 through 8 labeled: CE 4, 11, O1, 12, O2, 13, O3, and Uss. Pins 16, 15, 14, 13, 12, 11, 10, and 9 are labeled: UDD, CE 2, 15, O5, 16, O6, 14, and O4. The right package has pins 2, 4, 6, 10, 1, 14, 12, and 15 labeled: CE 4, CE 2, and CE 2. Pins 3, 5, 7, 9, 13, and 11 are labeled: 3, 5, 7, 9, 13, and 11. The diagram shows the internal logic of the inverters.

Pin diagram of the 74VHC04 hex inverters. The package is shown with pins 1 through 16. Pin 1 is VDD, pin 16 is VSS, and pin 14 is GND. The output pins are labeled 1 through 14. The input pins are labeled 1 through 14. The output pins are labeled 1 through 14. The input pins are labeled 1 through 14.

Figure 1 shows the pin connections for the 74VHC04. The left package has pins 1 through 8 labeled: C11, C12, O10, O11, O12, O13, R1, and Uss. The right package has pins 1 through 8 labeled: UDo, R2, O23, O21, O20, C22, R2, and C21. Connections are shown between the two packages: C11 to UDo, C12 to R2, O10 to O23, O11 to O21, O12 to O20, O13 to C22, R1 to R2, and Uss to C21. The right package also has additional pins 9 through 14 labeled: CT16, O10, O11, O12, O13, CT16, O20, O21, O22, O23, and R2.

Pin diagram of the 74VHC04 hex inverters. The chip has two rows of pins. The left row (pins 1-6) includes V_{ss} (pin 6), and pins 1-5 are numbered 1 through 5. The right row (pins 7-12) includes V_{DD} (pin 7), pins 12-10 are numbered 12 through 10, and pin 9 is an open circle. A power supply symbol is shown connected to pin 9.

Pin diagram of the 74VHC04 hex inverters. The diagram shows a 14-pin package with pins 1 through 14 labeled. Pins 1, 2, 3, 4, 5, and 6 are inputs for inverters 1 through 6. Pins 7 and 8 are Vss and VDD respectively. Pins 9, 10, 11, 12, 13, and 14 are inputs for inverters 7 through 12. The outputs are labeled Q1 through Q6. The diagram is a schematic representation of the physical pin connections.

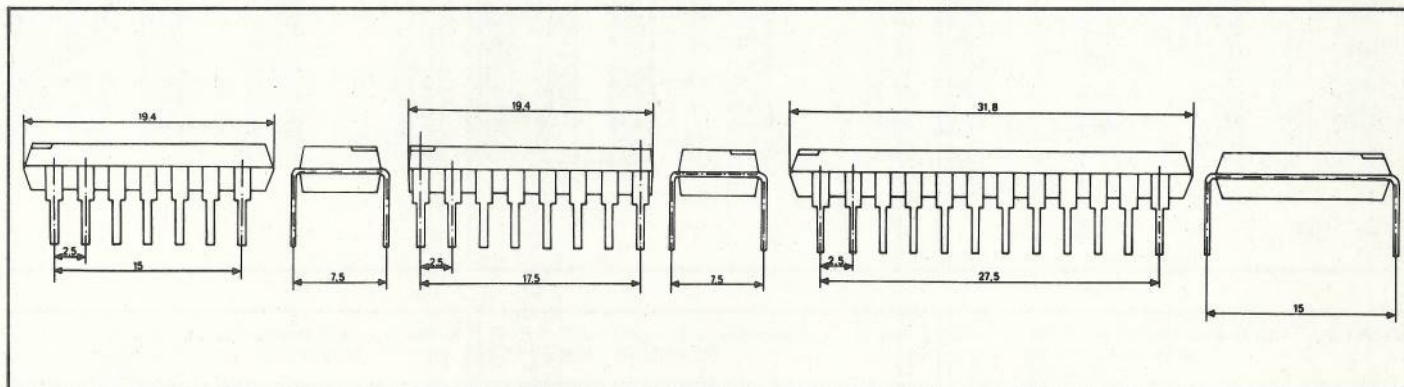
B 2	1	18	U _{DD}	10	A 0	=	A>B	Q 13
A 2	2	15	A 3	7	A 1		A=B	Q 3
A=B	3	14	B 3	2	A 2		A<B	Q 12
IA>B	4	13	A>B	15	A 3			
IA<B	5	12	A<B	11	B 0			
IA=B	6	11	B 0	9	B 1			
A 1	7	10	A 0	1	B 2			
U _{SS}	8	9	B 1	14	B 3			
		4			IA>B			
		5			IA=B			
		6			IA<B			

Lfd. Nr.	veb mikro-elektronik „karl marx“ erfurt -stammbetrieb-	National Semi-conductor	Fairchild	RCA	SGS ATEs	Motorola	Toshiba
1	V 4001 D	CD 4001 BCN	F 4001 BPC	CD 4001 BE	HCF 4001 BP	MC 14001 BCP	TC 4001 BP
2	V 4007 D	CD 4007 CN	F 4007 UBC	CD 4007 UBE	HCF 4007 UBE	MC 14007 UBCP	TC 4007 UBP
3	V 4011 D	CD 4011 BCN	F 4011 BPC	CD 4011 BE	HCF 4011 BE	MC 14011 BCP	TC 4011 BP
4	V 4012 D	CD 4012 BCN	F 4012 BPC	CD 4012 BE	HCF 4012 BE	MC 14012 BCP	TC 4012 BP
5	V 4013 D	CD 4013 BCN	F 4013 BPC	CD 4013 BE	HCF 4013 BE	MC 14013 BCP	TC 4013 BP
6	V 4015 D	CD 4015 BNC	F 4015 BPC	CD 4015 BE	HCF 4015 BE	MC 14015 BCP	TC 4015 BP
7	V 4017 D	CD 4017 BCN	F 4017 BPC	CD 4017 BE	HCF 4017 BE	MC 14017 BCP	TC 4017 BP
8	V 4019 D	CD 4019 BCN	F 4019 BPC	CD 4019 BE	HCF 4019 BE	—	TC 4019 BP
9	V 4023 D	CD 4023 BCN	F 4023 BPC	CD 4023 BE	HCF 4023 BE	MC 14023 BCP	TC 4023 BP
10	V 4027 D	CD 4027 BCN	F 4027 BPC	CD 4027 BE	HCF 4027 BE	MC 14027 BCP	TC 4027 BP
11	V 4028 D	CD 4028 BCN	F 4028 BPC	CD 4028 BE	HCF 4028 BE	MC 14028 BCP	TC 4028 BP
12	V 4029 D	CD 4029 BCN	F 4029 BPC	CD 4029 BE	HCF 4029 BE	MC 14029 BCP	TC 4029 BP
13	V 4030 D	CD 4030 BCN	F 4030 BPC	CD 4030 BE	HCF 4030 BE	—	TC 4030 BP
14	V 4034 D	CD 4034 BCN	F 4034 BPC	CD 4034 BE	HCF 4034 BE	MC 14034 BCP	TC 4034 BP
15	V 4035 D	CD 4035 BCN	F 4035 BPC	CD 4035 BE	HCF 4035 BE	MC 14035 BCP	TC 4035 BP
16	V 4042 D	CD 4042 BCN	F 4042 BPC	CD 4042 BE	HCF 4042 BE	MC 14042 BCP	TC 4042 BP
17	V 4044 D	CD 4044 BCN	F 4044 BPC	CD 4044 BE	HCF 4044 BE	MC 14044 BCP	TC 4044 BP
18	V 4046 D	CD 4046 BCN	F 4046 BPC	CD 4046 BE	HCF 4046 BE	MC 14046 BCP	TC 4046 BP
19	V 4048 D	CD 4048 BCN	—	CD 4048 BE	HCF 4048 BE	MC 14048 BCP	TC 4048 BP
20	V 4050 D	CD 4050 BCN	F 4050 BPC	CD 4050 BE	HCF 4050 BE	MC 14050 BCP	TC 4050 BP
21	V 4051 D	CD 4051 BCN	F 4051 BPC	CD 4051 BE	HCF 4051 BE	MC 14051 BCP	TC 4051 BP
22	V 4066 D	CD 4066 BCN	F 4066 BPC	CD 4066 BE	HCF 4066 BE	MC 14066 BCP	TC 4066 BP
23	V 4093 D	CD 4093 BCN	F 4093 BPC	CD 4093 BE	HCF 4093 BE	MC 14093 BCP	TC 4093 BP
24	V 40098 D	—	F 40098 BPC	—	—	—	—
25	V 40511 D	(CD 4511 BCN)	(F 4511 BPC)	(CD 4511 BE)	(HCF 4511 BE)	(MC 14511 BCP)	(TC 4511 BP)
26	V 4520 D	CD 4520 BCN	F 4520 BPC	CD 4520 BE	HCF 4520 BE	MC 14520 BCP	TC 4520 BP
27	V 4531 D	—	F 4531 BPC	—	HCF 4531 BE	MC 14531 BCP	TC 4531 BP
28	V 4538 D	CD 4538 BCN	F 4538 BPC	CD 4538 BE	HCF 4538 BE	MC 14538 BCP	—
29	V 4585 D	—	—	CD 4585 BE	HCF 4585 BE	MC 14585 BCP	TC 4585 BP

Die in Klammern angegebenen Vergleichstypen sind nicht in jedem Fall äquivalent.

The equivalent types in parentheses are not any case pin compatible.

Gehäusebauform Packages



Diese Übersichtsinformation gibt keine Auskunft über Liefermöglichkeiten und enthält keine Verbindlichkeiten zur Produktion. Die gültigen Vertragsunterlagen beim Bezug der Bauelemente sind die Typenstandards. Rechtsverbindlich ist jeweils die Auftragsbestätigung. Änderungen im Zuge der technischen Weiterentwicklung vorbehalten.

This publication furnishes no information on availability of the devices and implies no liabilities for production. Solely the type standards and the confirmation of order shall be binding upon the contractor for the supply of components. Modifications caused by continual technological advance are reserved.



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stammbetrieb

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