Official Pin Map: CPLD Hardware Debugger

This document maps the Verilog ports in `top_level.v` to the physical pins on the **Helium v1.1** board. This is the "source of truth" for the Quartus Pin Planner.

Reference: Helium User Manual, Pages 5-6.

Function	Verilog Port Name	Helium Board Label	CPLD Pin #
Clock	clk_1hz	Onboard Clock	43
Global Reset	reset_button	SW3	6
Mode Switch	mode_switch	SW1	4
FSM Input [0]	fsm_input_x[0]	SW2	5
FSM Input [1]	fsm_input_x[1]	SW4	8
Step Button	step_button	SW8	14
FSM Output [0]	fsm_output_z[0]	LED8	33
FSM Output [1]	fsm_output_z[1]	LED7	31
7-Seg 'a'	segments_out[0]	External I/O	16
7-Seg 'b'	segments_out[1]	External I/O	18
7-Seg 'c'	segments_out[2]	External I/O	19
7-Seg 'd'	segments_out[3]	External I/O	34
7-Seg 'e'	segments_out[4]	External I/O	37
7-Seg 'f'	segments_out[5]	External I/O	39
7-Seg 'g'	segments_out[6]	External I/O	40
(Unused)	–	SW5, SW6, SW7	(9, 11, 12)
(Unused)	–	LED1 - LED6	(24-29)

-
-
-
-
-
-
-
-