

CPT

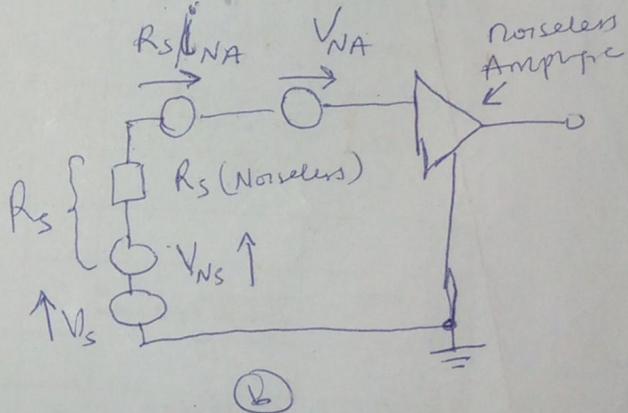
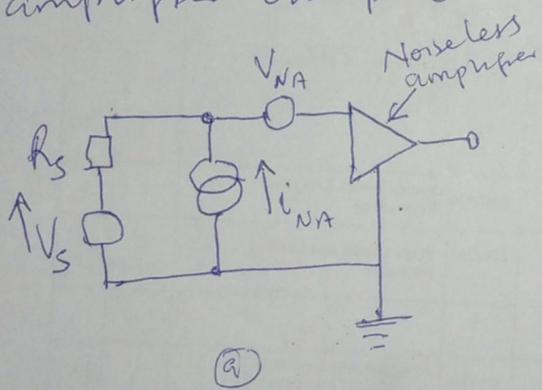
24-04-19 (b)

(E)

Noise in Amplifiers

345

The resistors and Transistors in amplifiers all contribute noise to the amplifiers output. Resistors generate Johnson or thermal noise and transistors generate shot noise and flicker noise. The concept of equivalent input noise voltage and equivalent input noise current is used to ease the calculation of the total noise power and the signal to noise ratio at the amplifier output.



Equivalent Input Noise Source: (a) At amplifier input
 b) equivalent noise generator replaced by V_s there
 are no equivalent.

We use the concept of equivalent input noise voltage and equivalent input noise current as in figure above. The noisy amplifier is represented in figure (a) by a noiseless amplifier with the same characteristics, except-

Noise in Amplifiers

- for the noise, together with equivalent noise sources at its input.

The equivalent input noise voltage is the noise voltage which when connected across the input of the noiseless amplifier, would cause the same noise at the output as the noisy amplifier with its input shorted to earth.

The equivalent input noise current is the noise current which when connected in parallel with the (noiseless) source resistance and across the input of the noiseless amplifier, would cause the same noise at the output as the noisy amplifier with an equal (noiseless) source resistance across its input.

1 Noise Factor

$$F = 1 + \frac{P_{NA}}{P_{NI}}$$

Where P_{NA} is the noise added by the amplifier, referred to the input. $F = 1 + \frac{\sqrt{V^2_{NA}}}{\sqrt{V^2_{NI}}}$

$\sqrt{V^2_{NA}}$ = mean square value of the noise voltage added by the amplifier, referred to the input, and $\sqrt{V^2_{NI}}$ is the mean square value of the input noise voltage.

In figure (a), the input noise arises in the source resistance, and is

$$\overline{V_{NI}^2} = 4R_s K T \Delta f$$

The noise voltage added by the amplifier, referred to the input, is represented by the equivalent input noise voltage and current sources V_{NA} & i_{NA} .

In figure (b) the noise current generator is replaced by its Thevenin equivalent voltage generator $i_{NA} R_s$. The total mean square value of V_{NI} and $i_{NA} R_s$ is $\overline{V_{NI}^2} + \overline{i_{NA}^2 R_s^2}$, if the two noise sources are not correlated. If they are correlated the sum becomes

$$\overline{V_N^2} = \overline{V_{NA}^2} + \overline{i_{NA}^2 R_s^2} + 2\gamma V_{NA\text{rms}} i_{NA\text{rms}} R_s$$

Where γ = correlation coefficient with a value between -1 and +1. The noise figure can now become

$$F = 1 + \frac{\overline{V_N^2}}{\overline{V_{NI}^2}}$$

$$= 1 + \frac{\overline{V_{NA}^2} + \overline{i_{NA}^2 R_s^2} + 2\gamma V_{NA\text{rms}} i_{NA\text{rms}} R_s}{4R_s K T \Delta f}$$

$$F = 1 + \frac{\overline{V_{NA}^2} + \overline{i_{NA}^2 R_s^2}}{4R_s K T \Delta f}$$

Noise figure reduces γ

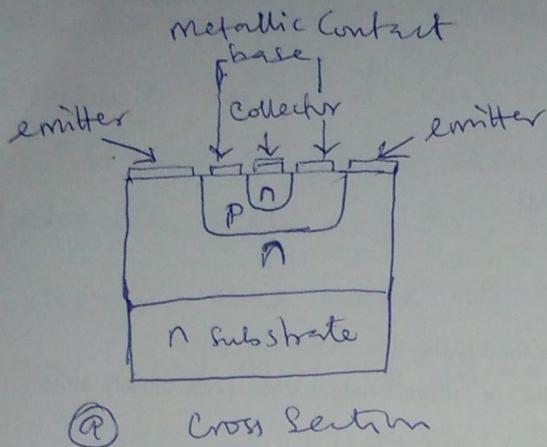
} Noise mechanism are not correlated
In many cases but correlates in few.

Bipolar Junction Transistors (BJTs)

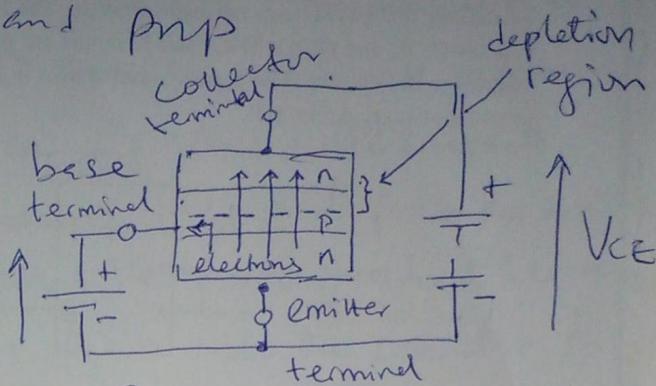
BJT's have three layers of semiconductor material

The two types are NPN and PNP

Silicon Planar BJT



(A) Cross Section



(B) enlarged view active
area of (A)

Figure above shows the essential features of construction of an NPN type. Figure (A) is a cross section through a transistor made by the planar process, in which the semiconductor dopants are diffused into a thin silicon crystal wafer.

Figure (B) shows an enlarged view of the active part of figure (A). The layer of the P-type material forms the base region, sandwiched between the two N-type layers forming the emitter and collector regions. The normal biasing arrangement is with the base-emitter PN junction forward biased as shown. The forward bias across the base-emitter junction causes electrons to flow from emitter to base, and holes to flow from base to emitter. The emitter is heavily doped than the base, so majority of current carriers are electrons from emitter to base.

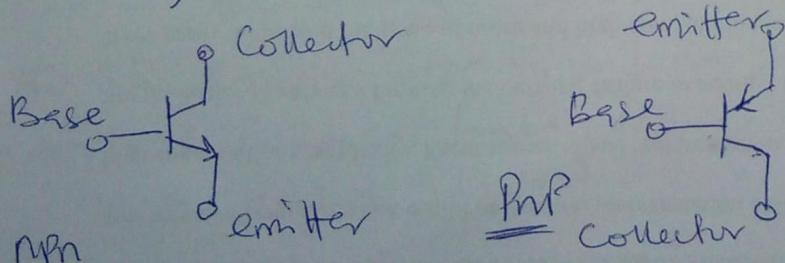
The positive bias on the Collector Causes a positive Electric field gradient across the collector base Junction so that, if opened alone, the junction will become depleted of current carriers and will act as a reverse biased diode carrying very little current

However, when electrons are injected from the emitter into the base region, the positive field gradient between collector and base attracts them into the collector region, and most of them flow the collector terminal

This flow constitute conventional current from the V_{CE} supply into the collector. Meanwhile a much smaller hole current flows from base to emitter, constituting a small current into the base terminal. The ratio of the collector current to the base current is called the current gain β or h_{FE} .

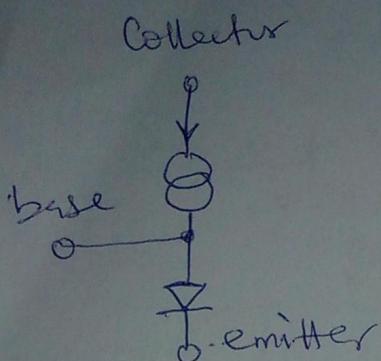
$$\beta = I_C / I_B$$

Typical values range from 100 to 400 in low-power transistors, but can be as low as 20 in power transistors



Note that the transistors are drawn so that current flows from top to bottom, the usual convention in circuit diagrams. In BJT, current flow is in the direction of the arrow from the emitter symbol.

Non Linear Model of an NPN Transistor



This figure shows an equivalent circuit model of the n-p-n transistor under normal bias conditions.

The base-emitter junction is forward biased, and is represented by a diode.

The relationship between the

Voltage across the diode, V_{BE} , and the emitter current through it, I_E , is the same as that in an ordinary diode.

recalling the diode equation $I = I_s \exp(V_D/V_T)$

with V_D replaced by V_{BE} , and I replaced by I_E

then

$$I_E = I_s \exp(V_{BE}/V_T)$$

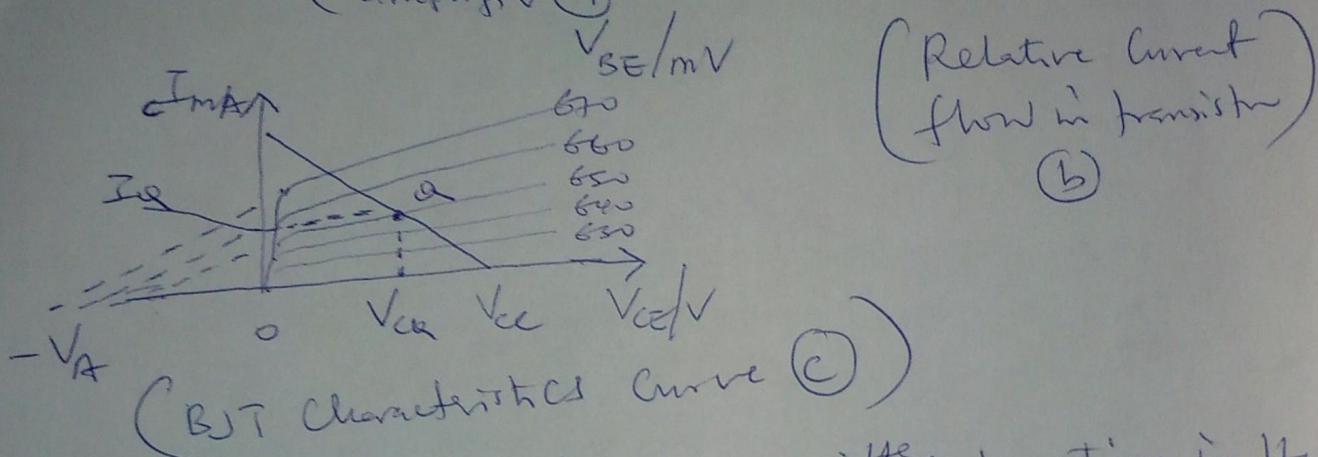
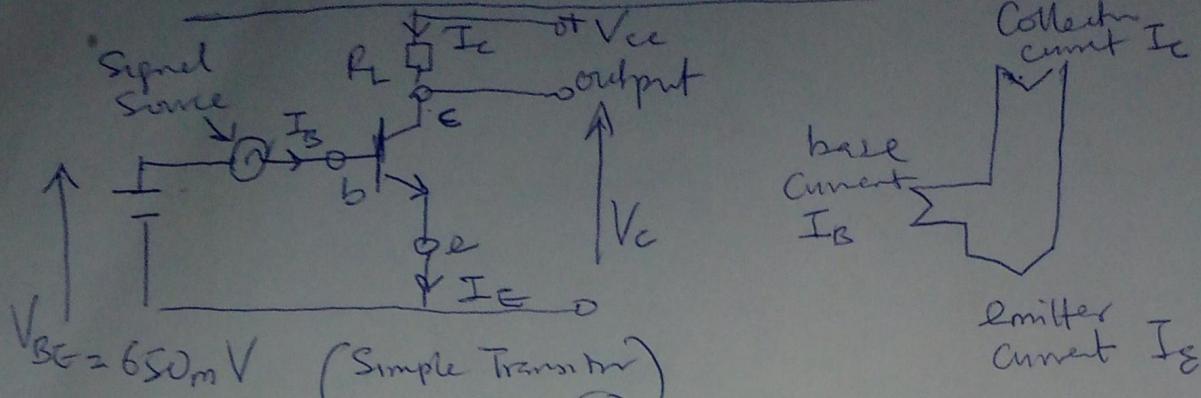
thus the emitter current is determined by the base-emitter voltage. In the case of a silicon planar transistor V_T has the value 25mV at room temperature.

The collector-base junction is reverse biased, and carries the collector current which is almost equal to the emitter current; and largely independent of the applied collector-base voltage. This is represented with a current generator with a value of

$$I_C = I_E - I_B,$$

$$= I_E - I_C/\beta = \left(\frac{\beta}{\beta + 1}\right) I_E$$

A Simple Amplifier Circuit



The 650mV dc biases the base-emitter junction in its forward direction and determine the amount of emitter current I_E which flows through the base-emitter junction. Thus, the same current I_E flows from the collector to the emitter, the small base current I_B is the difference.

If the collector voltage is held constant (zero load resistance) and the input voltage is increased by a small amount ΔV_B , the collector current increases by an amount ΔI_C . The ratio of the increase in collector current to the increase in base voltage which caused it is called Mutual Conductance g_m .

$$g_m = \frac{\Delta I_C}{\Delta V_B}, \text{ under approximations, } \Delta V_c = -\Delta I_C R_L$$

$$= -\frac{g_m}{g_m} \Delta V_B R_L$$

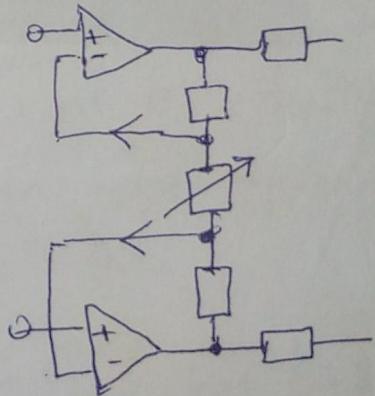
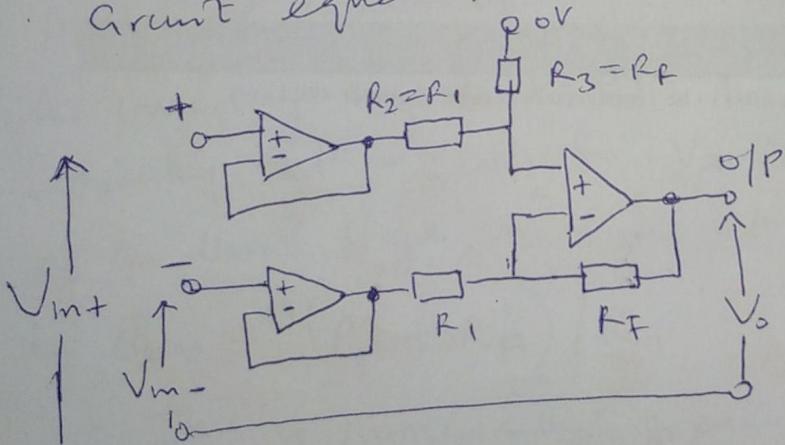
ΔV_B and $\Delta V_C = V_o$ and V_o .

$$\frac{V_o}{g_m} = \frac{\Delta V_C}{\Delta V_B} = -g_m R_L$$

Signal Processing with Operational Amplifiers

Instrumentation Amplifiers

The specification of the amplifier includes a high input impedance at both inverting and non-inverting inputs; with a well defined gain set by negative feedback. This is impossible to achieve with one op-amp because the virtual earth at the inverting input of the op-amp makes the input impedance of the circuit equal to the value of the input resistor.



An Instrumentation Amplifier

The two inputs, inverting and non-inverting are buffered by voltage followers from the rest of the circuit, so these inputs have very high input impedances. The outputs of the voltage followers V_1 and V_2 are amplified by the third stage.

To calculate the differential gain starting with V_2 ,
 the input voltage from the Inverting Input of the overall
 amplifier. This is to be inverted, so it goes to the
 Inverting Input of the third stage. Imagine the non
 -inverting input voltage of the overall amplifier is
 set temporarily to zero, so V_1 and the non-inverting
 input to the third stage, are held at 0V. The
 gain from the Inverting Input of the overall
 amplifier is - $G_{inv} = \frac{V_o}{V_{in-}} = \frac{V_o}{V_2} = -\frac{R_f}{R_1}$

Next consider V_1 , the Input voltage from the non
 Inverting Input of the overall amplifier. Imagine
 the Inverting Input voltage of the overall amplifier tem-
 -porarily set to zero, so V_2 is held at 0V. The gain
 of the third stage, measured at its non Inverting Input,
 is thus - $(R_1 + R_f) / R_1$.

This is numerically greater than G_{inv} , but the two
 gains should be numerically equal. So the signal V_1
 is reduced appropriately, by the potential divider
 R_2, R_3 before reaching the third stages non Inv-
 -erating Input. The signal at this Input is

$$\left\{ \frac{R_3}{R_2 + R_3} \right\} V_1$$

So the overall gain, from the non inverting input of the overall amplifier is then-

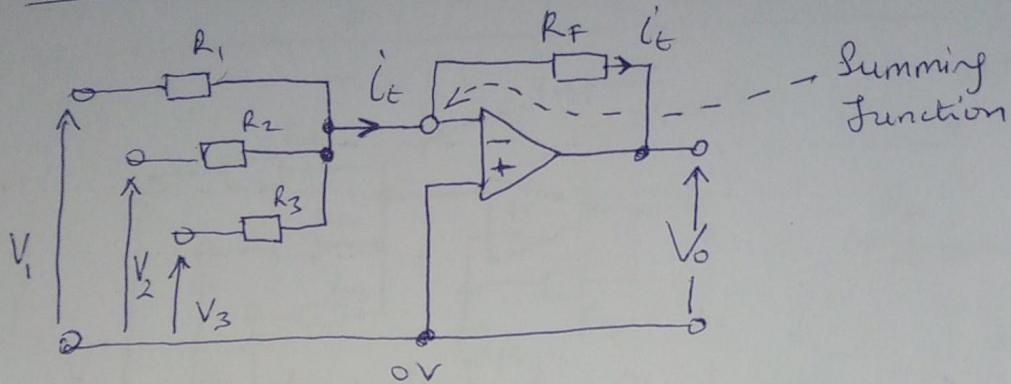
$$G_{ni} = \left\{ \frac{R_3}{(R_2 + R_3)} \right\} \left\{ \frac{(R_1 + R_F)}{R_1} \right\}$$

But R_2 is made equal to R_1 , and R_1 made equal to R_F , so G_{ni} becomes

$$\begin{aligned} G_{ni} &= \left\{ \frac{R_F}{(R_1 + R_F)} \right\} \left\{ (R_1 + R_F) / R_1 \right\} \\ &= \frac{R_F}{R_1} \end{aligned}$$

This makes G_{ni} equal and opposite to G_{in} as required.
Instrumentation amplifiers are available in IC form, with the three opamps and associated resistors all integrated in one chip.

Inverting Summing Amplifier



Inverting Summing Amplifier:

Providing the circuit operates within its limits of linearity
the inverting input of the op amp is a virtual earth
So the total input current from all linear inputs

$$\text{is simply } I_E = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

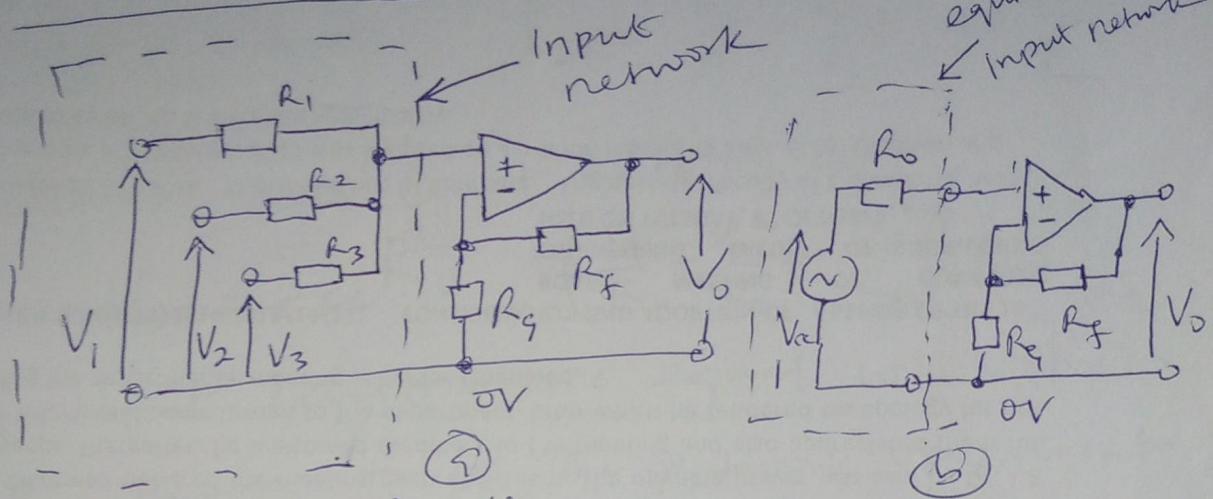
In this circuit, the virtual earth is called Summing Junction
because all the input currents are added at this point.
This same total current flows through the feedback
resistor R_F , so the output voltage is

$$V_o = -I_E R_F = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) R_F$$

When all input resistors are equal, ~~to R_F~~

$$V_o = -(V_1 + V_2 + \dots + V_n)$$

Non Inverting Summing Amplifiers



(a) A non Inverting Summing Amplifier (b) Input network equivalent

The op amps non inverting input imposes negligible loading on the input network, since its input impedance is very high due to the series negative feedback, so the Op amps output voltage is -

$$V_o = V_{oc} \left(1 + \frac{R_f}{R_g} \right)$$

Where V_{oc} is the open circuit output voltage of the thevenin equivalent circuit of the input network. To find V_{oc} , we first find the output resistance of the network : Short circuiting all the input generators with one source, the output resistance becomes all the input resistors in parallel.

$$R_o = R_1 \parallel R_2 \parallel R_3 \parallel \dots \parallel R_n$$

Calculating from output conductance i.e $G_o = 1/R_o$

$$G_o = G_1 + G_2 + \dots + G_n$$

With the network output shorted to earth, the
Short Circuit Current $I_{SC} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n}$

The network open circuit voltage is

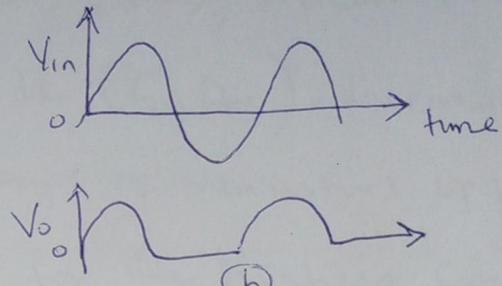
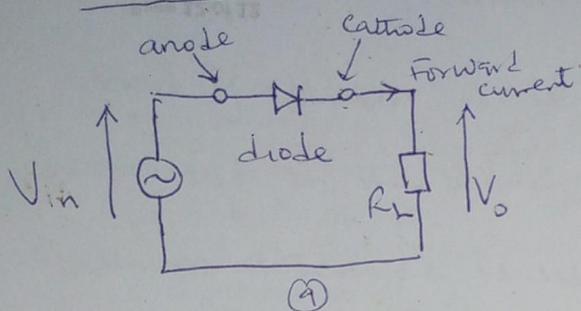
$$V_{OC} = I_{SC} R_o = \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n} \right) R_o$$

When Input resistors are equal with value
 R_m , R_o becomes R_{in}/N , the Network open circuit
output voltage is: $V_{OC} = I_{SC} R_o$

$$= \left(\frac{V_1}{R_{in}} + \frac{V_2}{R_{in}} + \dots + \frac{V_N}{R_{in}} \right) \frac{R_m}{N}$$

$$= (V_1 + V_2 + \dots + V_N)/N$$

Diode and Transistor Circuits



A simple rectifier circuit, Using an Ideal diode.

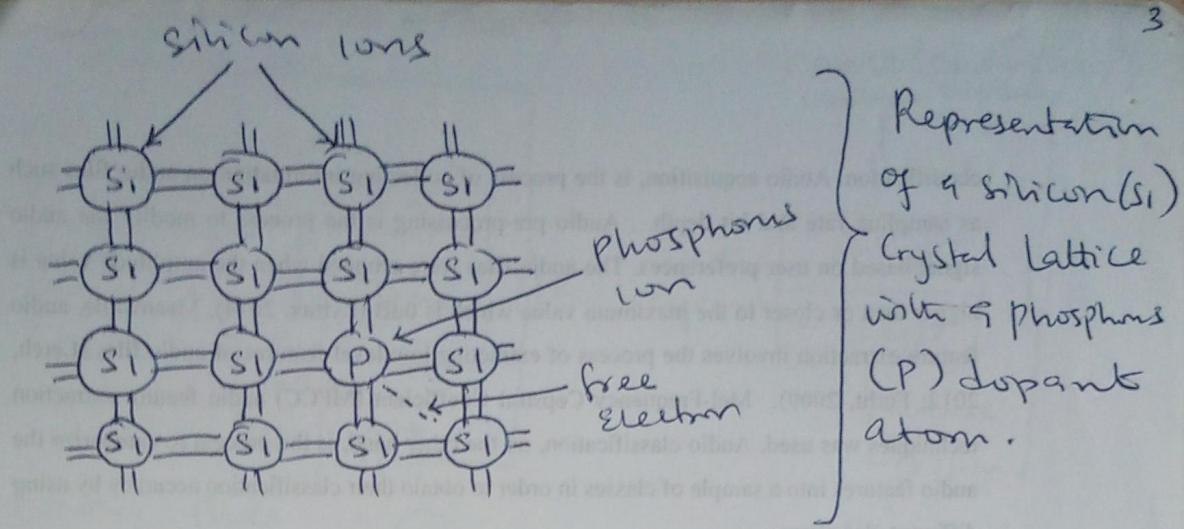
The figure above Shows current flows from anode to Cathode when the anode voltage is positive with respect to the cathode voltage. Very little current flows when the polarities are reversed. So the diode acts like a one-way valve in a pump. Diodes are used in electronic circuits to rectify A.C. supplies and signals as Show in figure (b) above, only the positive half cycles of AC supply are allowed to appear at the output of the circuit. Thus the output is always Positive.

With the aid of a Capacitor, this waveform can be turned into a close approximation of a DC voltage for use as a DC supply for analog or digital circuits.

~~Typical Se~~

Typical Semiconductors used for diodes and transistors are Germanium (Ge), Silicon (Si) and gallium arsenide (GaAs). Germanium was used in the early days of transistors up till now. Gallium arsenide is used for the highest frequency transistors in microwave applications such as mobile phones, and in high speed digital circuits; But silicon is by far the most widely used semiconductor.

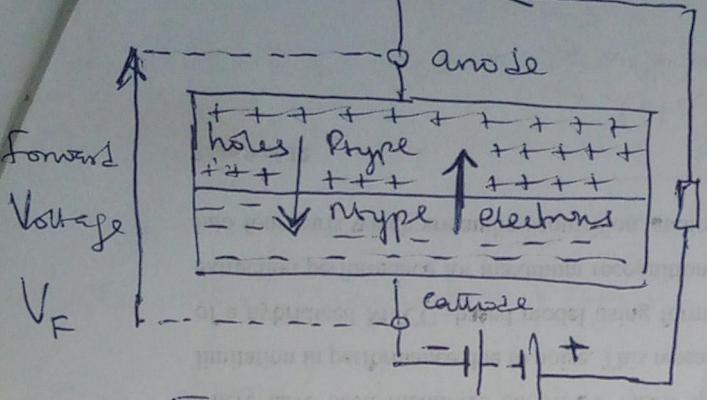
A pure Intrinsic Semiconductor is an almost perfect insulator at absolute zero temperature. As the temperature is increased the conductivity increases. At room temperature, the conductivity lies between that of an insulator and a good conductor, such as a metal. Hence the term Semiconductor. The conductivity can be increased by doping the pure semiconductor with impurities, so creating an extrinsic Semiconductor. In silicon, two dopants are used; Phosphorus and Boron.



The figure shows a silicon crystal lattice whose atoms are effectively held together by covalent bonds. A small amount of phosphorous dopant is represented in the diagram by one atom phosphorus. Silicon is a group 4 element but phosphorus is group 5, so when a phosphorus atom is introduced in the lattice, it bonds with the adjacent silicon atoms leaving one electron free to wander through the lattice. Electrons have negative charge, so the free electrons gives the semiconductor a free carrier of negative charge. For this reason, silicon doped with phosphorus is called an n-type semiconductor.

The other used dopant is boron which is a group 3 element, so one of the bonds to the adjacent atoms in the silicon lattice is short of one electron. This deficiency is called a hole. It is possible for an electron of adjacent atom to fall into the hole, thus moving the hole with a positive charge. This is P-type Semiconductor.

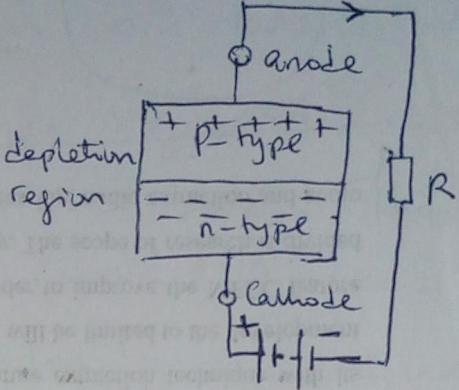
Forward (Conventional) current I_F



Forward Bias Supply

(a)

Reverse (Conventional) leakage current



Reverse Bias Supply

(b)

Semiconductor diode action (a) Forward bias

(b) Reverse bias

Figure above shows a diode structure; a silicon crystal of which part has been doped to make n-type, and part is p-type. The area of transition between this two is called a PN junction.

* Figure (a) Shows the effect of applying a voltage to the diode with anode positive with respect to the cathode making the P-type region positive with respect to the n-type. The free electrons in the n-type region are attracted, by the potential gradient to the positively biased P-type region and flow from cathode to anode.

Note: A flow of electrons in one direction is regarded as a flow of conventional current in the opposite direction. So, conventional current flows from anode to cathode in the diode. At the same time, the holes in the P-type material are effectively attracted towards the anode and also constitute a conventional current from anode to cathode. So the diode conduct in one direction.

Figure ⑥ shows the situation with reverse bias, the free electrons in the P-type region are attracted towards the positively biased cathode. This depletes the junction region of current carriers of both types (electrons and holes), and reduces the current to just a small leakage current due to thermally generated electrons. So, for practical purposes, the diode does not conduct in the reverse direction.

Diode Characteristics

The current through a PN junction varies exponentially with voltage across it : $I = I_s \{ \exp(V_D/V_T) - 1 \}$

I_s = Current at absolute zero temperature (dope Semiconductor)

V_D = forward Voltage across the diode

V_T = constant Voltage at a given temperature ($V_T = kT/q$)

k = Boltzmann constant ($1.38 \times 10^{-23} \text{ J/K}$)

q = electron charge ($1.6 \times 10^{-19} \text{ C}$)

T = absolute temperature of device 17°C (290K)

$V_T = 25\text{mV}$ or 28mV at room temperature.

For diode forward voltage greater than about 100mV , the exponential factor is greater than one by far - thus : $I \approx I_s \exp(V_D/V_T)$, $\ln(I/I_s) = V_D/V_T$

$V_D = V_T \ln(I/I_s)$. For initial & final current and voltage (I_1, V_1, I_2, V_2)

$V_2 = V_T \ln(I_2/I_1)$, $V_1 = V_T \ln(I_1/I_s)$, $\Delta V = V_2 - V_1 = V_T \ln(I_2/I_1)$

* Transistor Operation

Transistors are semiconductor devices that exhibit the properties of amplification. There a small time varying voltage (or current) can be increased (Amplified) to a larger voltage (or current) that is a replica of the smaller.

There are two basic categories of transistors:

- (i) Bipolar Junction Transistor (BJT)
- (ii) Field Effect Transistor (FET)

These two types of devices differ greatly in construction and theory of operation but their broad applications are similar.

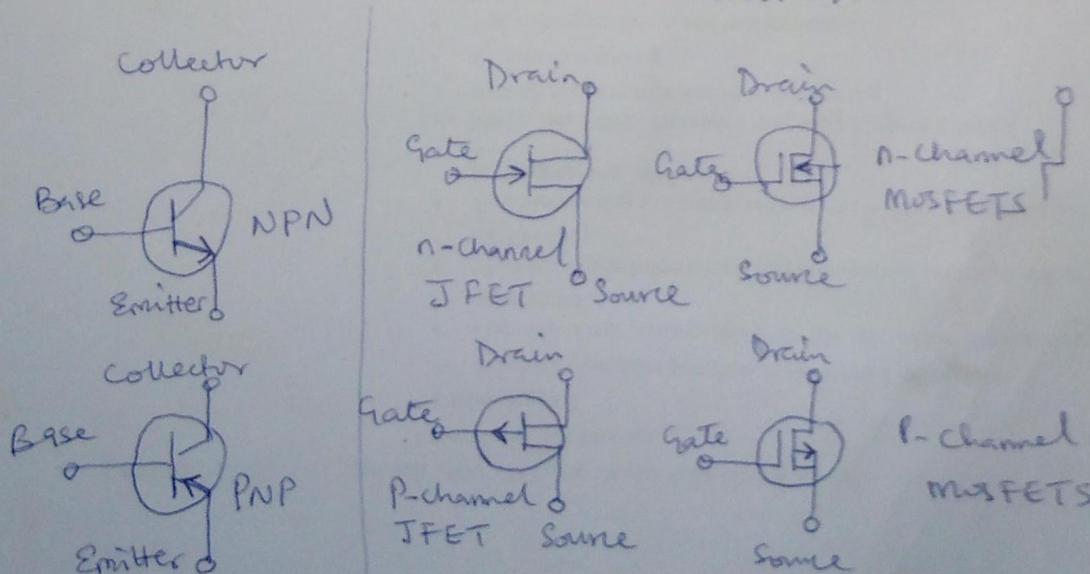


fig 1

(i) Bipolar Junction Transistor

(ii) Field Effect Transistors

(B)

Figure 1 Shows the schematic symbols for the two types of the bipolar transistor (pnp and npn) and the field effect transistor

A transistor consists of three (3) regions; for the BJT they are base, emitter, and collector while gate, source, and drain are for the FET. In order for a transistor to operate properly as an amplifier, the junctions must be correctly biased with external voltages. An examination shows that the emitter current is the sum of the collector and base currents thus:

$$I_e = I_c + I_b$$

(C)

Common Base Configuration

When a transistor is connected with the base as the common or ground terminal, it is called a common base connection. In common base amplifier, an important parameter is the Short circuit gain which is defined as the ratio of change in collector current to the change in emitter current and given by

$$\alpha = I_c / I_e$$

In common base amplifier, the input signal voltage and the output signal voltage are in phase

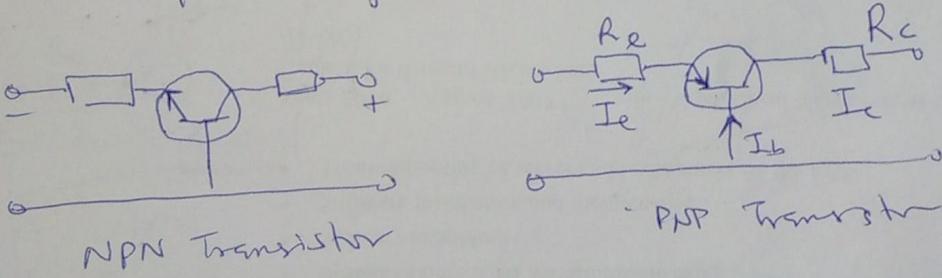


Fig 2 Common Base Configuration.

Common Emitter Configuration

This configuration is when a transistor is connected such that the emitter is the common or ground terminal. Here the DC current gain (β) is the ratio of I_c to I_b and given by $\beta = I_c / I_b$

(D)

β is the static forward current transfer ratio
usually denoted by h_{fe} on data sheets.

Establishing relationship between β and α ,

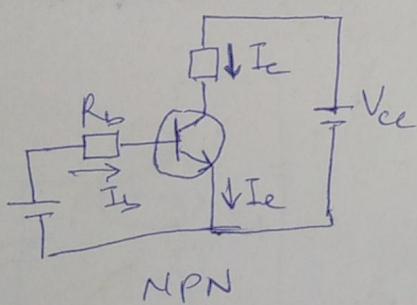
$$\beta = I_c/I_b \text{ , or } I_b = I_c/\beta$$

$$\alpha = I_c/I_e \text{ or } I_e = I_c/\alpha$$

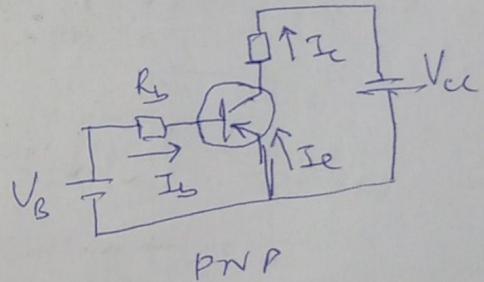
$$I_e = I_c + I_b$$

$$I_c/\alpha = I_c + I_c/\beta$$

$$1/\alpha = 1 + 1/\beta \text{ or } \beta = \alpha\beta + \alpha(\beta+1)$$



NPN



PNP

Fig 3 Common Emitter Configuration.

$$\alpha = \frac{\beta}{\beta+1} \text{ and } \beta = \frac{\alpha}{1-\alpha}$$

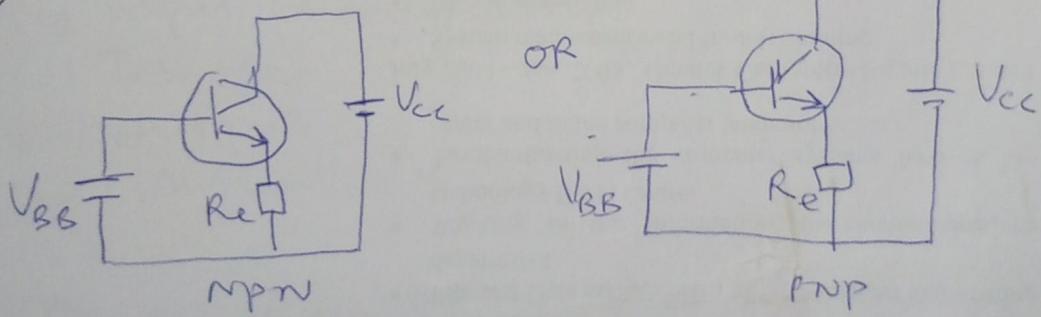
(E)

Common Collector Configuration

When a transistor is connected such that the collector is the common or ground terminal, it is called Common Collector Configuration or emitter follower. The main use of the emitter follower is as an impedance transformer where it is connected between a high impedance source and a low impedance load.

This is because the common collector amplifier has high ^{Input} impedance and low output impedance. Its gain is about unity.

*



Fy4 Common Collector Configuration

F

Transistor Static Characteristics

A number of current/voltage plots are used in the study of the operation of a transistor circuit. These curves are known as static characteristics. Curves give information about the value of current flowing into or out of one terminal for either a given current flowing or a given voltage applied.

* Four sets of characteristics are commonly used for each configuration.

- (i) Input characteristics
- (ii) Transfer ✓
- (iii) Output ✓
- (iv) Mutual ✓

Common Base Static Characteristics

Has the input characteristics shown how the emitter current varies with change in the emitter-base voltage when the collector-base voltage is held constant. The slope of the characteristics is called Input Conductance of the transistor ($\frac{\Delta I_e}{\Delta V_{eb}}$). This is specified in

(Q)

Fig 5 Showing typical Common base Input Characteristics.

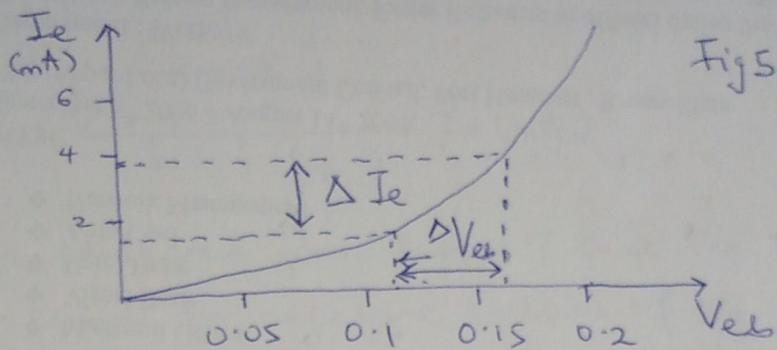


Fig 5 Common base Input Characteristics.

Figure 6 Shows the Common base transfer characteristics which shows how the collector current varies with changes in emitter current when the collector-base voltage is held constant. The slope of the transfer characteristic gives the short circuit current gain represented by $(\Delta I_c / \Delta I_e)$

The output characteristics indicates the way the collector current varies with change in collector-base voltage with the emitter current held constant. The reciprocal of the slope of the output characteristic $(\Delta V_{cb} / \Delta I_c)$ gives the output resistance of the transistor.

(H)

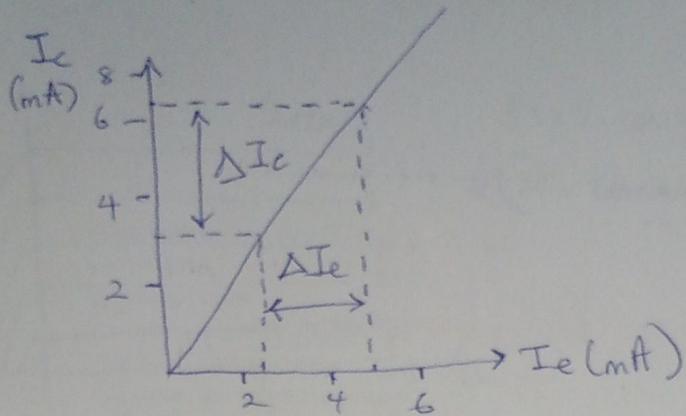
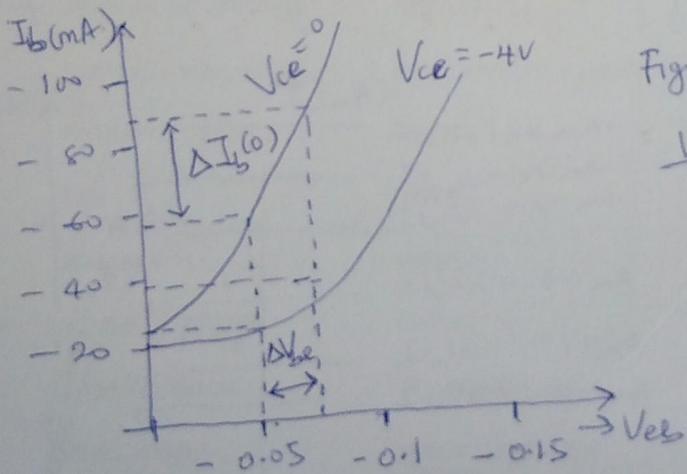


Fig 6 Transfer Characteristics

It can be observed from figure 7 that the collector current flows for negative values of the collector-base voltage when the emitter current is zero. This current is the minority charge carrier current that passes across the collector/base junction and is known as the Collector leakage current I_{Cbo} .

Common Emitter Static Characteristic



Base current is held constant.

Figure 8: The Common emitter Input Characteristics: This shows the way in which the base current varies with change in the base-emitter voltage when the collector-emitter voltage is held constant.

(5)

The characteristics enables us to obtain the output resistance given by $R_o = \Delta V_{ce} / \Delta I_c$. It can be seen from figure 9 that collector current flows even when the input or base current is zero. This current is the Common-emitter Leakage Current (I_{CEO}).

Biasing Techniques

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. The dc level of operation of a transistor is controlled by a number of factors including the range of possible operating points on the device characteristics.

- * The term Biasing means the application of dc voltage to establish a fixed level of current and voltage which in turn will establish the operating point. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).

(K)

Fixed Bias Technique

This provides a straight forward and simple method of establishing the Q-point. Considering the base-emitter junction, we obtain

$$V_{be} = I_B R_B + V_{be} \text{ so that } I_B = \frac{(V_{cc} - V_{be})}{R_B}$$

Similarly, for collector emitter loop, we obtain

$$V_{ce} = I_C R_C + V_{ce} \text{ or } V_{ce} = V_{cc} - I_C R_C.$$

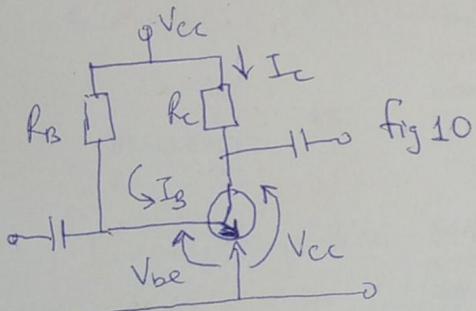


fig 10 Fixed bias circuit

given that the transistor is silicon.

Solution

$$I_{BQ} = \frac{(V_{cc} - V_{be})}{R_B} = (12 - 0.7) / (240 \times 10^3) = 47.68 \mu A$$

$$I_{CQ} = \beta I_{BQ} = 50 (47.68 \times 10^{-6}) = 2.35 \text{ mA}$$

$$V_{ceQ} = (V_{cc} - I_{CQ} R_C) = 12 - (2.35 \times 10^3 \times 2.2 \times 10^3) = 6.83 \text{ V}$$

$$V_{BB} = V_{be} = 0.7 \quad (\text{since the transistor is silicon and } V_{ee} = 0)$$

$$V_{BC} = V_{BB} - V_{ce} = (0.7 - 6.83) = -6.13 \text{ V}$$

The Negative sign indicate that the junction is reverse biased.

Example: For the fixed bias configuration shown in figure 10

$$R_B = 240 \text{ k}\Omega, R_C = 2.2 \text{ k}\Omega$$

$$V_{cc} = 12 \text{ V and } \beta = 50. \text{ Determine}$$

$$I_{BQ}, I_{CQ}, V_{ceQ}, V_{BB}, \text{ and } V_{BC}$$

(L)

Emitter Stabilized Bias Circuit

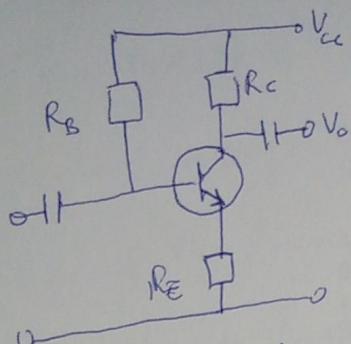


Fig 11 Emitter Stabilized Bias

Figure 11 shows the circuit of an Emitter stabilized bias, the circuit contains an emitter resistor to improve the stability level over that of the fixed bias configuration.

$$\text{Here } V_{cc} = I_B R_B + V_{be} + I_e R_e$$

$$\text{but } I_e = (\beta + 1) I_B \therefore V_{cc} = I_B R_B + V_{be} + (\beta + 1) I_B R_e$$

$$I_B = \frac{V_{cc} - V_{be}}{R_B + (\beta + 1) R_e}$$

Considering the collector emitter loop, we obtain

$$V_{ce} = I_e R_c + V_{ce} + I_e R_e = I_c R_c + V_{ce} + I_c R_e \text{ since } I_c \approx I_e$$

$$V_{ce} = V_{ce} + I_c (R_c + R_e) \text{ or } V_{cc} = V_{ce} - I_c (R_c + R_e)$$

(M)

Voltage Divider Bias Circuit

In the previous bias configurations, the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor. However since β is temperature sensitive, it is necessary to develop a bias circuit that is independent of β , as in Figure 12 below.

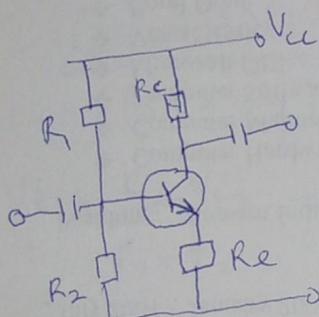


Fig 12

Voltage Divider Bias

Here let $R_t = \frac{R_1 R_2}{R_1 + R_2}$

If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can almost be independent of β .

$$V_t = \frac{R_2 V_{CC}}{R_1 + R_2} = V_{R2}$$

$$I_B = \frac{V_t - V_{BE}}{R_1 + (\beta + 1) R_E} \quad \text{and} \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$