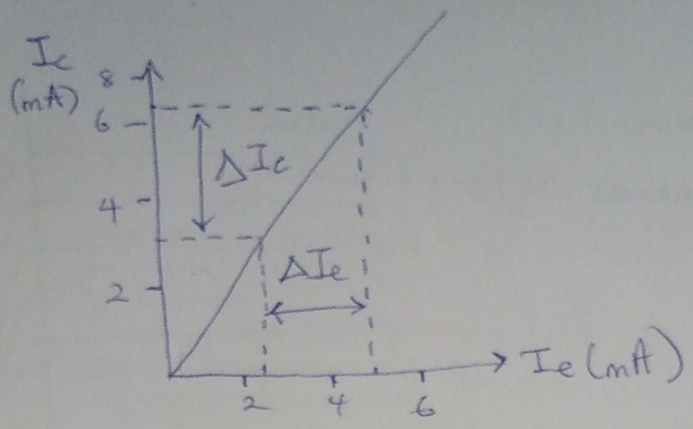


Fig 6 Transfer Characteristics

It can be observed from figure 7 that the collector current flows for negative values of the collector-base voltage when the emitter current is zero. This current is the minority charge carrier current that passes across the collector/base junction and is known as the Collector leakage current Icbo

Common Emitter Static Characteristic

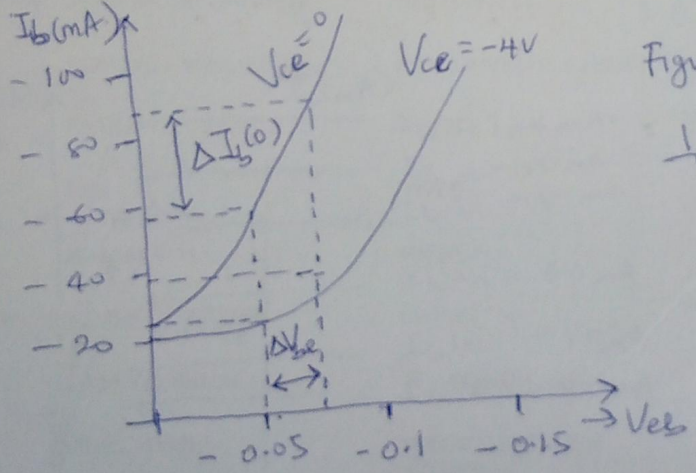


Figure 8: The Common emitter Input Characteristics: This shows the way in which the base current varies with change in the base-emitter voltage when the collector-emitter voltage is held constant.

(I)

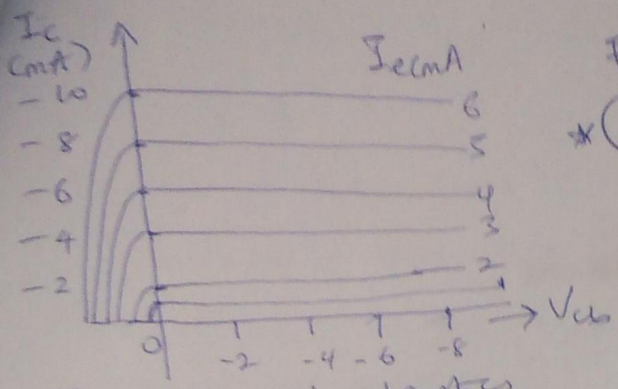


Fig 7 output Characteristics

*(for Common base Static Characteristics)

Fig 7 output Characteristics

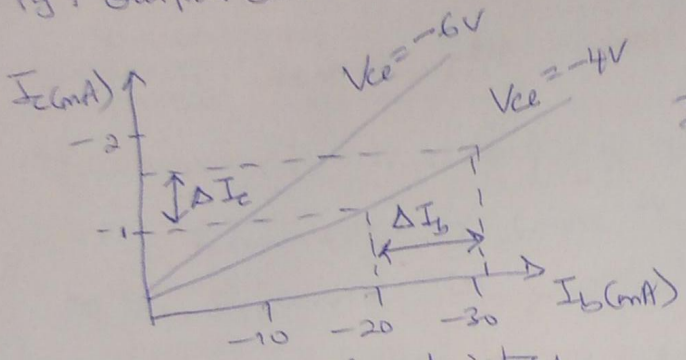


Fig 8 Transfer Characteristics.

Figure 8 is the Common emitter Transfer characteristics which shows how the Collector Current changes with changes in the base current.

The Slope of this characteristics gives the current gain of the transistor in this Configuration.

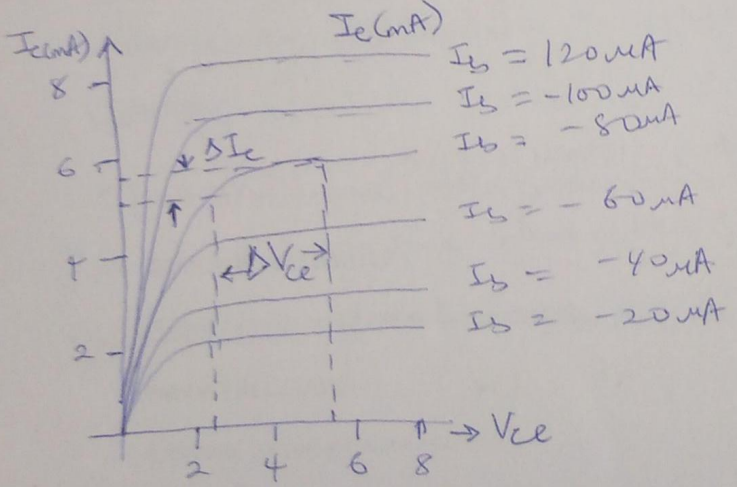


fig 9 Output Characteristics

*(For Common Emitter Static Characteristics)

Figure 9 Shows the Common-emitter output characteristics which Illustrates the changes that occur in Collector current with changes in Collector-emitter Voltage for Constant Value of base Current.

The characteristics enables us to obtain the output resistance given by $R_o = \Delta V_{ce} / \Delta I_c$.

It can be seen from figure 9 that collector current flows even when the input or base current is zero. This current is the Common-emitter Leakage Current (I_{CEO})

BIASING TECHNIQUES

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. The dc level of operation of a transistor is controlled by a number of factors including the range of possible operating points on the device characteristics.

The term Biasing means the application of dc voltage to establish a fixed level of current and voltage which in turn will establish the operating point. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).

(K)

Fixed Bias Technique

This provides a straight forward and simple method of establishing the Q-point. Considering the base-emitter junction, we obtain

$$V_{cc} = I_B R_B + V_{be} \text{ so that } I_B = \frac{(V_{cc} - V_{be})}{R_B}$$

Similarly, for collector emitter loop, we obtain

$$V_{cc} = I_c R_c + V_{ce} \text{ or } V_{ce} = V_{cc} - I_c R_c.$$

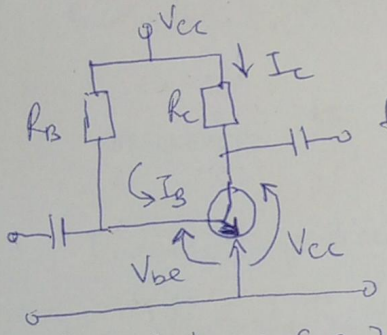


fig 10 Fixed bias circuit

fig 10

Example: For the fixed bias configuration shown in figure 10 $R_B = 240K\Omega$, $R_c = 2.2K\Omega$ $V_{cc} = 12V$ and $\beta = 50$. Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_{BB} and V_{BC} given that the transistor is Silicon.

Solution

$$I_{BQ} = \frac{(V_{cc} - V_{be})}{R_B} = (12 - 0.7)/(240 \times 10^3) = 47.08\mu A$$

$$I_{CQ} = \beta I_{BQ} = 50(47.08 \times 10^{-6}) = 2.35mA$$

$$V_{CEQ} = (V_{cc} - I_{CQ} R_c) = 12 - (2.35 \times 10^{-3} \times 2.2 \times 10^3) = 6.83V$$

$V_{BB} = V_{be} = 0.7$ (Since the transistor is Silicon and $V_{EE} = 0$)

$$V_{BC} = V_{BB} - V_{CE} = (0.7 - 6.83) = -6.13V$$

The Negative Sign Indicate that the Junction is reverse biased.

(L)

Emitter Stabilized Bias Circuit

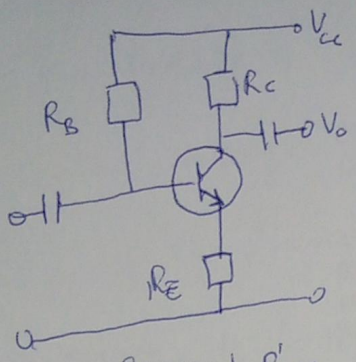


fig 11 Emitter Stabilized Bias

Figure 11 shows the circuit of an Emitter stabilized bias, the circuit contains an emitter resistor to improve the stability level over that of the fixed bias configuration.

Here $V_{cc} = I_B R_B + V_{be} + I_e R_e$

But $I_e = (\beta+1) I_B$ $\therefore V_{cc} = I_B R_B + V_{be} + (\beta+1) I_B R_e$

$$I_B = \frac{V_{cc} - V_{be}}{R_B + (\beta+1) R_e}$$

Considering the collector emitter loop, we obtain

$V_{cc} = I_c R_c + V_{ce} + I_e R_e = I_c R_c + V_{ce} + I_c R_e$ since $I_c \simeq I_e$

$V_{cc} = V_{ce} + I_c (R_c + R_e)$ or $V_{cc} = V_{ce} - I_c (R_c + R_e)$

(M)

Voltage Divider Bias Circuit

In the previous bias configurations, the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor. However since β is temperature sensitive, it is necessary to develop a bias circuit that is independent of β: as in Figure 12 below.

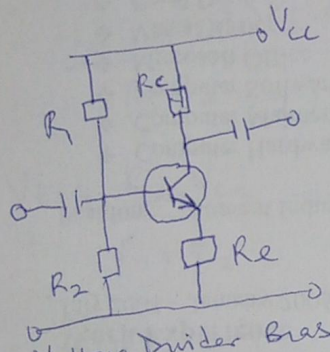


Fig 12 Voltage Divider Bias

If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can almost be independent of β

Here let $R_t = \dfrac{R_1 R_2}{R_1 + R_2}$

$$V_t = \frac{R_2 V_{cc}}{R_1 + R_2} = V_{R2}$$

$$I_B = \frac{V_t - V_{be}}{R_1 + (\beta + 1) R_e} \qquad \text{and } V_{ce} = V_{cc} - I_c (R_c + R_e)$$

Example

For the emitter bias circuit shown in figure 11, determine I_B, I_C, V_{CE}, V_C, V_E, V_B and V_{BC}, given that $\beta = 50$

Solution

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 - 0.7}{430 \times 10^3 + (51)(10^3)} = 40.1\,\mu A$$

$$I_C = I_B \beta = 50(40.1 \times 10^{-6}) = 2.01\,mA$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 20 - (2.01 \times 10^{-3})(2 \times 10^3 + 10^3)$$

$$= 20 - 6.03 = 13.97\,V$$

$$V_C = V_{CC} - I_C R_C = 20 - (2.01 \times 10^{-3})(2 \times 10^3) = 20 - 4.02 = 15.98\,V$$

$$V_E = V_C - V_{CE} = (15.98 - 13.97)\,V = 2.01\,V$$

$$V_B = V_{BE} + V_E = (0.7 + 2.01)\,V = 2.71\,V$$

$$V_{BC} = V_B - V_C = (2.71 - 15.98)\,V = -13.27\,V$$

Example

Determine the dc bias voltage V_{CE} and the current I_C for the circuit of figure 12 given that $R_1 = 39K\Omega$, $R_2 = 3.9K\Omega$, $R_C = 10K\Omega$, $R_E = 1.5K\Omega$, $V_{CC} = 22V$ and $\beta = 140$

Solution

$$R_t = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{(39 \times 10^3)(3.9 \times 10^3)}{(39 + 3.9)10^3} = 3.55K\Omega$$

$$V_t = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9 \times 10^3 \times 22)}{(39 + 3.9)10^3} = 2V$$

$$I_B = \frac{(V_t - V_{be})}{R_t + (\beta + 1)R_E} = \frac{2 - 0.7}{(3.55K\Omega) + (141)(1.5K\Omega)} = 6.05\mu A$$

$$I_C = \beta I_B = 140(6.05 \times 10^{-6}) = 0.85mA$$

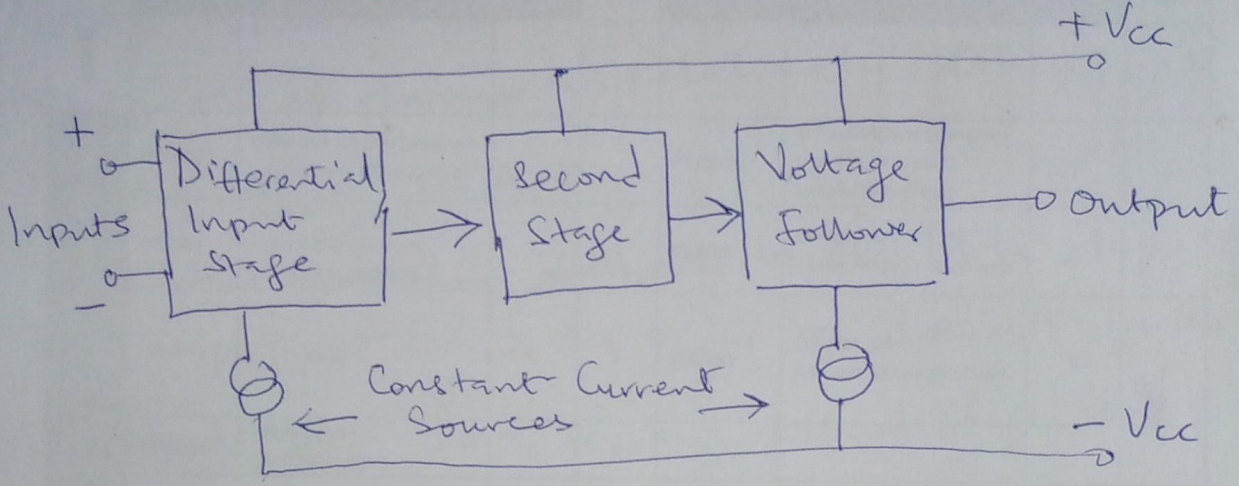
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 - (0.85 \times 10^{-3})(10 \times 10^3 + 1.5 \times 10^3)$$

$$= 12.22V$$

Design of Operational Amplifiers

Structure of Op Amp:



This diagram is a DC amplifier, with DC coupling between the stages. It uses a positive supply rail of Voltage Vcc and a negative rail of Voltage −Vcc so that the output signal can swing both positive and negative with respect to 0V

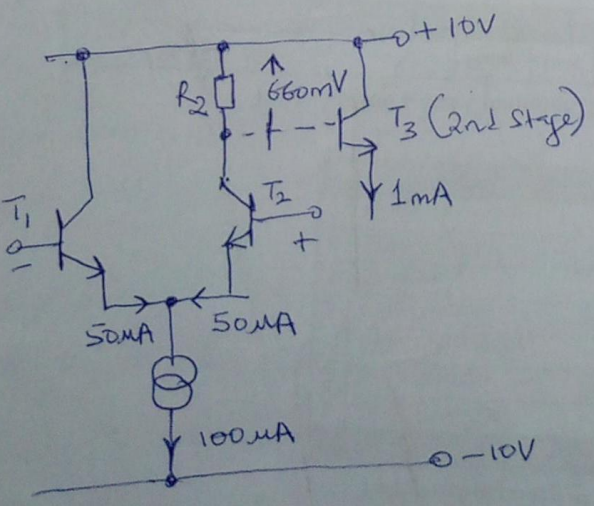
Typical supply voltage range from ±2V to ±18V

The Input Stage is a difference amplifier. IC op amps has a high input resistance of 1M ohm in some types, and many mega ohms in others. This stage is designed to operate at low current so as to optimize its noise performance. Its voltage gain is typically 5–10.

The second stage has the highest voltage gain this stage has the lowest cut-off frequency. The final stage is the output stage, it is a form of voltage follower with a voltage gain of one. Its output resistance is relatively low; typically 100Ω or so.

The operating currents of the three stages of the amplifier are in the order of 100uA for the input stage, 1mA for the second stage, and 10mA for the output stage. The constant current sources supply operating current to the input stage and the output stage.

Differential Pair Input Stage



This figure shows a simple differential pair, using BJTs. The two transistors of the differential pair are T_1 and T_2. The operating point is set by both inputs at 0V

Because of the circuit symmetry, the two emitter currents are then equal (assuming identical transistor characteristics) These make up the current $I_E = 100\mu A$ which is provided by the current source, so each emitter current is $50\mu A$.

For the best noise figure, bipolar transistors should be chosen with a high current gain at low collector current; and operated at 50 – 100 μA. Hence the choice for the input stage.

Using the operating current and supplies of ±10V, we assume use of bipolar transistors with current gain values of $h_{fe} = \beta = 200$, with $V_{BE} = 660mV$ at 1mA. Op amp is usually used with negative feedback to determine its gain and frequency response, and to stabilize its output operating point close to 0V

What value of V_{BE} should be assumed for T_1 and T_2?

A value of 580 mV should be assumed for the base emitter voltages of T_1 and T_2 so, with both inputs set to 0V, the emitters have a voltage of −580 mV.

The resistor R_2 has the voltage V_{BE} of T_3, say 660mV, across it, since T_3 operates at 1mA. R_2 carries the collector current of T_2 which is 50 μA, less the base current of T_3 which is 1mA/200 = 5μA. So

$$R_2 = 600mV/45\mu A$$
$$\approx 14.7K\Omega.$$

To find the low frequency Voltage gain

Consider the case of a differential input signal of amplitude V_{in}. The non Inverting Input (of the whole op amp) is at the base of T_2, and the Inverting Input at base of T_1.

When the differential signal is applied, the signal at T_2 base is $V_{in}/2$, and that at T_1 base is $-V_{in}/2$.

So a positive value of V_{in} causes the emitter current of T_2 to increase, and that of T_1 to decrease.

The changes in emitter currents are equal and opposite.

Assume small signals, so that the Circuit Operates linearly and so the Corresponding Changes in the base-emitter Voltages are equal and opposite, and the emitter Voltage remains fixed at about $-580mV$.

Thus, each transistor acts as if it were a grounded emitter amplifier, since its emitter Voltage is at 0V as far as signals are concerned. For a Conventional grounded emitter amplifier, the Output Voltage for an input V_1 is

$$V_2 = -g_m R_L V_1$$

The effective load resistance is R_{eff}, which is R_2 in parallel with r_i of T_3, and the effective input voltage is $V_{in}/2$.

So the signal at T_2 collector is

$$V_2 = -g_m R_{eff} V_{in}/2$$

the low frequency voltage gain A_1 is

$$A_1 = \frac{V_2}{V_{in}}$$

$$= -\tfrac{1}{2} g_m R_{eff}/2$$

In this case, $g_m = 40V^{-1} \times 50\mu A = 2mS$.

Since T_3 operates at 1mA, its r_e is $25mV/1mA = 25\Omega$

and $r_i = h_{fe} r_e = 200 \times 25 = 5K\Omega$

So $R_{eff} = 14.4K\Omega \| 5K\Omega \approx 3.7K\Omega$

The gain has the value

$$A_1 = -\tfrac{1}{2} \times 2mS \times 3.7K\Omega$$

$$= -3.7$$