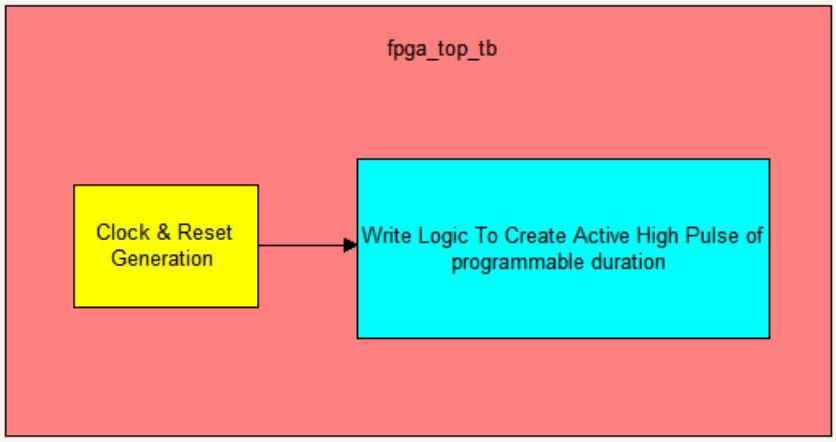
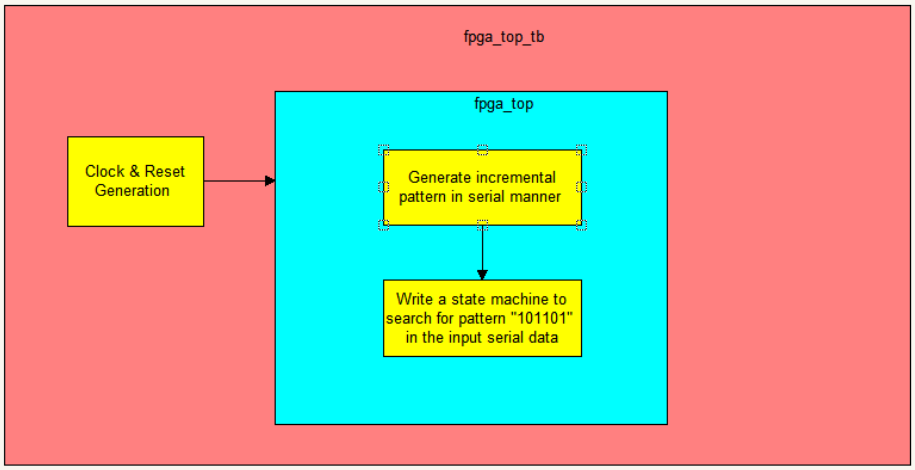
Problem no. 1



Design Pass Criteria : Pulse Duration should be same as expected. Try with different values of width and duration. RTL coding guidelines must be followed.
Pulse Generation should automatically start when reset goes down
Duration and Period would be compile time programmable
The Unit of width will be 1 clock cycle. i.e. if Width is 5 and Pulse Period is 12, the pulse should be High for 5 clock cycles and low for 7 clock cycles

Problem no. 2

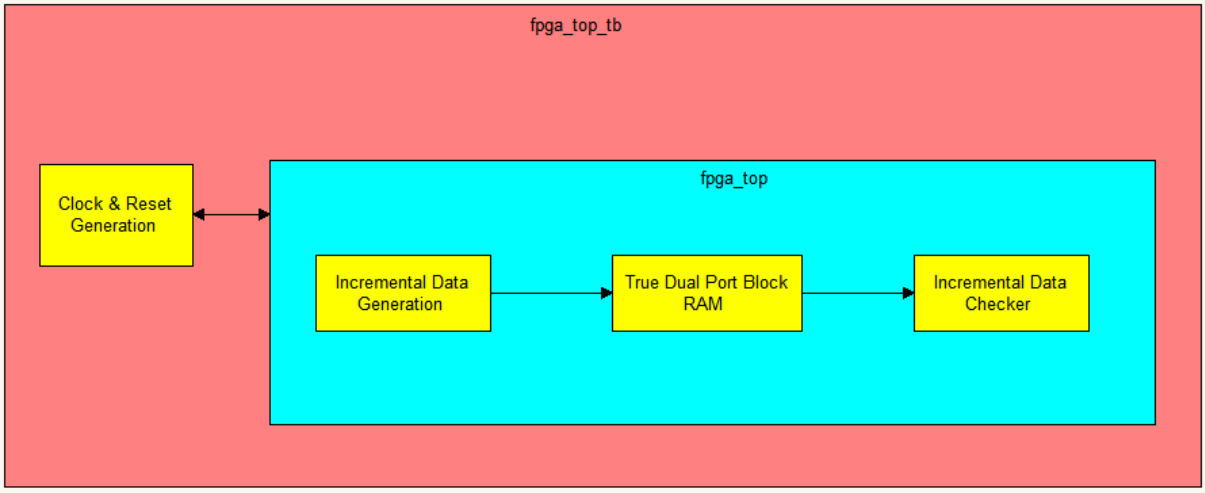


Requirements:

1. State machine should be able to search multiple occurances of the pattern. i.e. we need to generate a pulse when the pattern appears.
2. The incremental pattern is 8 bit wide (should be generated once in 8 clock cycles)
3. This pattern needs to be sent 1 bit at a time (serial)
4. Detector Block receives this 1 bit data stream and detects the pattern

Design Pass Criteria : Pattern seaching should be correct. RTL coding guidelines must be followed.

Problem no. 3



Requirements:

1. RAM should be compiled in library "building_blocks" and rest of the design in library "work"

2. RAM Initialized to 0.

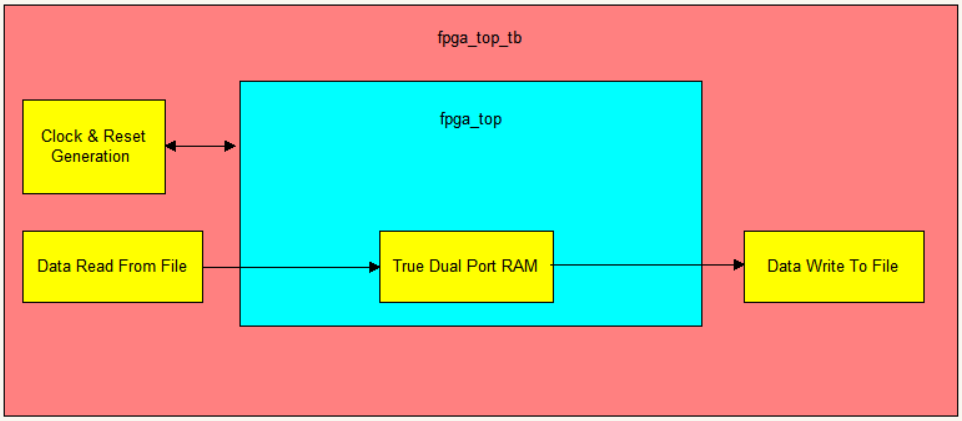
3. Both ports of RAM use same clock

4. Data Generator starts operation soon after reset goes low

5. Data checker starts operation after 2 clock cycles

Design Pass Criteria : Data Checker should Pass. RTL coding guidelines must be followed.

Problem no. 4



Requirements:

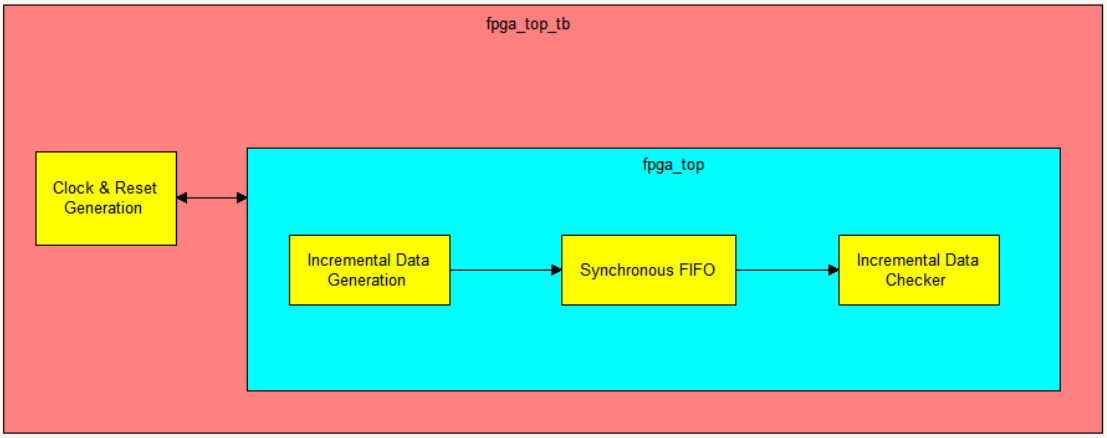
1. create records for read/write containing Address, Data and Wr_en/Rd_en. (Port list will contain clk, reset and records for read and write operation)

2. data read from file is written to RAM using this record. Same is true for read operation.

3. Data in the file should be Hex

Design Pass Criteria : Output File Should Match the Input File. RTL coding guidelines must be followed.

Problem no. 5



Requirements:

1. FIFO to be compiled in library "building_blocks" and rest of the design in library "work"

2. max value of circular incremental pattern is 8 bit compile time programmable

3. Data width of FIFO = 64 bit, Size of incremental Data = 8 bit (i.e. each clock cycle, 8 bytes of incremental data is to be written)
e.g If max value is x"0C"
during first clock cycle data to be written to FIFO = x"0706050403020100"
during second clock cyle data to be written will be = x"0201000C0B0A0908"
* use variables, array, loop to generate this data pattern

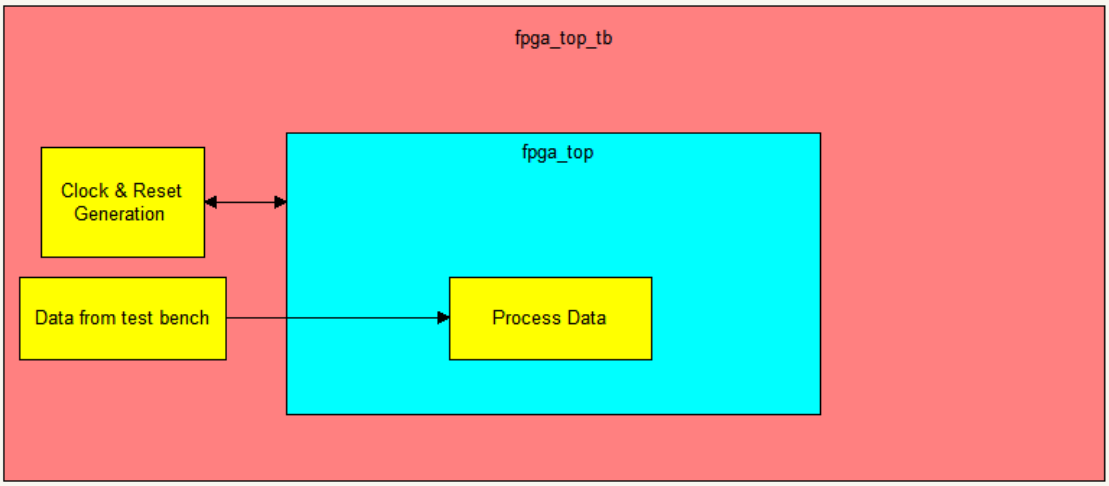
4. Checker will generate same pattern based on Valid (Empty) from FIFO to verify the data.

5. No signal can directly be passed from Generator to Checker.

6. Operation of Generator Block is controlled by an Enable signal from test bench.
i.e. Generator will generate data when Enable Signal is high and will HOLD its position when Enable signal is low (this signal is not given to checker block)

Design Pass Criteria : Data Checker should Pass. RTL coding guidelines must be followed.

Problem no. 6



Requirements:

1. Inputs are four 8-bit vectors A, B, C and D

2. need to find a condition when (A OR B) is not equal to ((B AND C) XOR D)

3. operation ((B AND C) XOR D) should be performed in two clock cycles

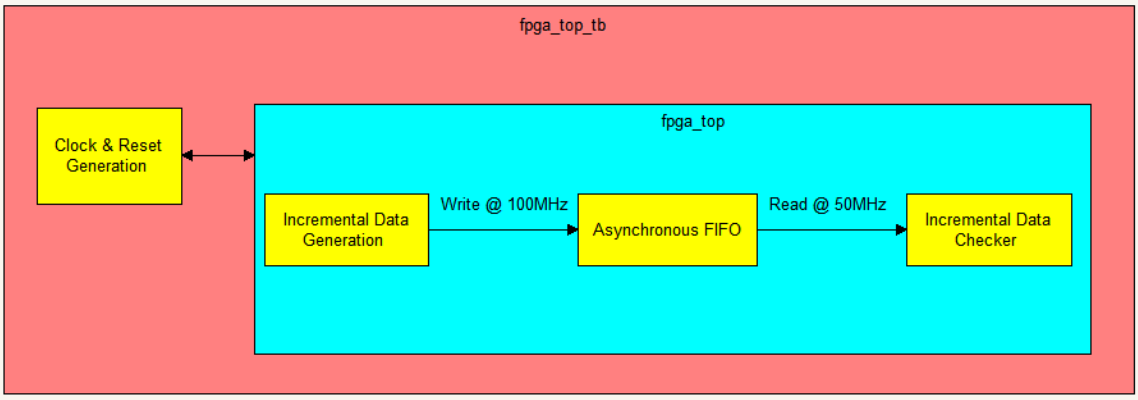
4. Inputs will be changed every clock cyle (i.e. pipelining should be done)

5. Output will be 1 bit signal which will be high when condition is met.

6. Inputs are generated from TB using a 32 bit counter
bit 7 DT 0 => A
bit 15 DT 8 => B
bit 23 DT 16 => C
bit 31 DT 24 => D

Design Pass Criteria : Design should perform given operation and follow design guidelines

Problem no. 7

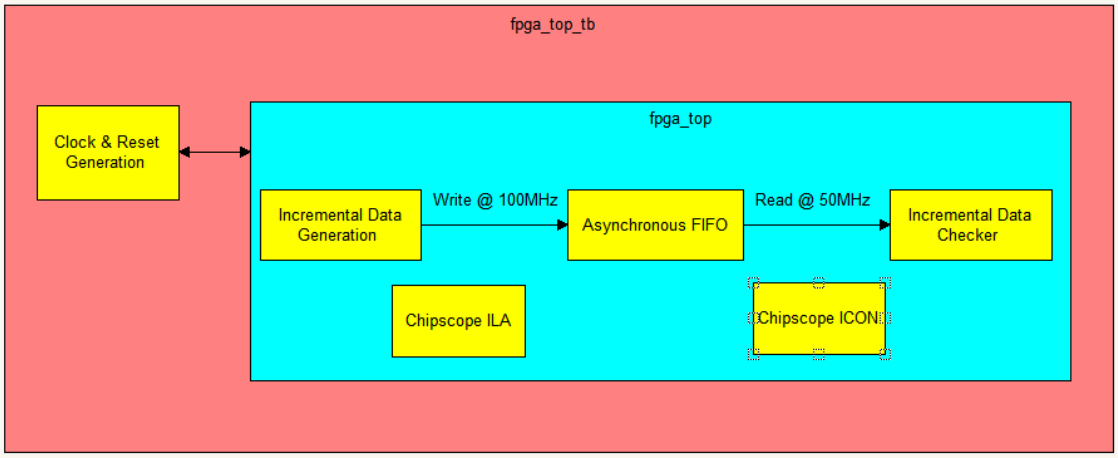


Requirements:

1. Clock 50 MHz is provided and clock 100 MHZ to be generated using PLL
2. Writing should stop when FIFO Almost full occurs and should resume when it goes down
3. similarly reading should not start untill empty goes down
4. Generator will start operation when it gets start pulse from test bench

Design Pass Criteria : Data Checker should Pass. RTL coding guidelines must be followed.

Problem no. 8



Requirements:

1. In the design of training 7, add chipscope

Design Pass Criteria : Data Checker should Pass. RTL coding guidelines must be followed.