Design and Implementation of a Fully Differential 6th-Order Sallen-Key Active Low-Pass Filter

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Content

1. Introduction

In the context of modern wireless communication systems, the demand for high-speed, low-power, and highly linear analog filtering solutions has been steadily increasing. Analog baseband filters play a critical role in shaping signal bandwidth, reducing out-of-band noise, and ensuring proper signal integrity before digitization.

The Sallen-Key topology has emerged as a compelling candidate for active low-pass filter design due to its simplicity, good frequency response characteristics, and ease of cascading into higher-order configurations. In particular, the fully-differential implementation of the Sallen-Key filter offers enhanced common-mode noise rejection, improved linearity, and compatibility with differential signal processing, which is standard in RF front-end and baseband applications.

This document outlines the design and simulation of a 6th-order fully-differential low-pass filter targeting a bandwidth of 20 MHz. The filter is based on the architecture and methodology described in the reference paper by Quan Hu et al. This ongoing document serves both as a design log and a technical reference for future development phases, including the upcoming Common-Mode Feedback (CMFB) integration.

2. Design Objectives

The primary objective of this project is to develop a high-performance, fully differential 6th-order Sallen-Key low-pass filter suitable for wideband wireless communication systems. The design aims to achieve a balance between simplicity, performance, and integration feasibility within a 180nm CMOS process.

Key design goals include:

- **High Linearity and Low Distortion**: Ensuring minimal signal distortion to maintain signal integrity in high-frequency applications.
- **Wide Bandwidth**: Achieving a bandwidth that accommodates the target frequency range for wideband communication.
- **Low Power Consumption**: Designing for energy efficiency to suit portable and battery-powered devices.
- **Compact Integration**: Utilizing a topology that allows for efficient integration within the constraints of modern CMOS processes.
- **Robust Common-Mode Rejection**: Implementing a fully differential design to enhance common-mode noise rejection and improve overall signal quality.

These objectives guide the design choices, including the selection of the Sallen-Key topology and the fully differential architecture, to meet the demands of modern wireless communication systems.

3. Design Methodology

3.1 Overview of the Sallen-Key Topology

The chosen architecture for this filter is a fully differential implementation of the Sallen-Key low-pass topology. The Sallen-Key configuration was selected due to its well-known simplicity, robustness, and effectiveness in active filter design. It offers an excellent balance between performance and ease of integration for low-order and cascaded high-order filter structures.

In the context of this design, three identical second-order stages are cascaded to realize a 6th-order low-pass filter. The fully differential nature of the topology provides superior common-mode noise rejection, enhanced linearity, and better immunity to power supply variations—characteristics that are critical for analog signal processing in wideband wireless communication systems.

Compared to alternatives like gm-C, LC, and MFB filters:

- gm-C filters, although suitable for tunable high-frequency applications, are more susceptible to process, voltage, and temperature (PVT) variations. They also typically demand complex biasing schemes and consume more power due to the reliance on transconductance stages.
- LC filters, while offering sharp roll-off and high-Q performance, are impractical for full integration in a CMOS process, especially at these frequencies, due to the large silicon area required for on-chip inductors.
- Multiple Feedback (MFB) filters can provide high selectivity, but the closed-loop feedback structure increases design complexity and reduces modularity when cascading stages, making it harder to control interaction between stages.

In contrast, the Sallen-Key topology simplifies the design by allowing independent design and verification of each second-order section. Its unity-gain configuration fits the target specifications of 1 V/V closed-loop gain and stable operation with minimal gain ripple. Additionally, it offers more predictable behavior under transient and AC simulations, which is beneficial during iterative optimization and layout-aware verification.

Thus, the fully differential Sallen-Key topology serves as an ideal foundation for the 6th-order filter design, meeting the performance, simplicity, and integration constraints defined in this project.

3.2 Target Specifications

Technology	TSMC_65nm
Supply voltage	1.2v
Closed loop gain	1v/v
Closed loop Bandwidth	20MHz
dbc @ 200MHz	-55dbc
Max group delay	30nsec
Dynamic range	50db
Load capacitance	40fF
Gain ripples	<1db
CMRR	>60db
CM settling time	$\frac{1}{2}$ diff settling time
One reference current source.	10uA
Group_delay	<30nsec
Stable when driving by 200mv differential step	

3.3 Filter Order and Frequency Band

To meet the stringent performance requirements of wideband wireless communication systems, a 6th-order low-pass filter was selected. A 6th-order implementation provides sufficient roll-off to suppress high-frequency interferers while preserving in-band signal integrity.

The Butterworth response was chosen for this filter due to its maximally flat magnitude response in the passband. This ensures minimal signal distortion and gain ripple, both of which are critical when dealing with analog baseband signals. Unlike Chebyshev or elliptic filters, which offer sharper roll-off at the expense of passband ripples or phase nonlinearity, the Butterworth topology provides a smooth frequency response and excellent phase linearity within the passband.

This flatness helps maintain the signal quality without introducing amplitude distortion or compromising the group delay excessively. Group delay flatness is particularly important in wideband systems where data symbols can span a large portion of the spectrum. The design targets a closed-loop bandwidth of 20 MHz with an attenuation of at least –55 dBc at 200 MHz. A Butterworth filter of order 6 achieves this while maintaining a monotonic roll-off and minimal overshoot in the time domain.

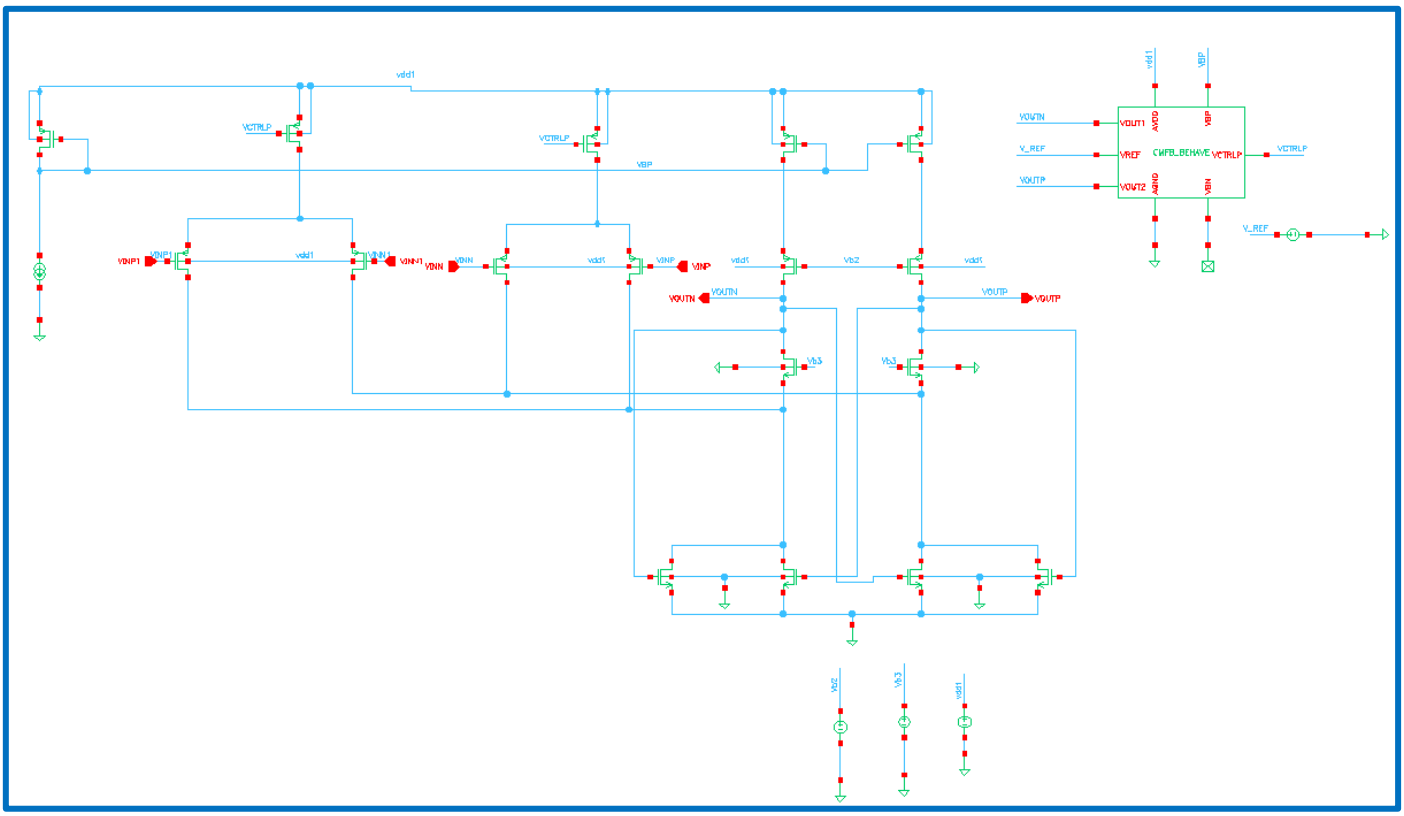
The pole locations for a normalized 6th-order Butterworth filter are placed evenly on a semicircle in the left half of the complex s-plane. These poles were scaled and mapped accordingly to match the target bandwidth and implemented using three cascaded second-order fully differential Sallen-Key stages. Each stage contributes a pair of complex conjugate poles, and the cutoff frequency for each stage is chosen to preserve the overall Butterworth response.

In summary, the choice of a 6th-order Butterworth filter strikes a practical balance between spectral selectivity, transient response, and implementation simplicity, making it well-suited for this application.

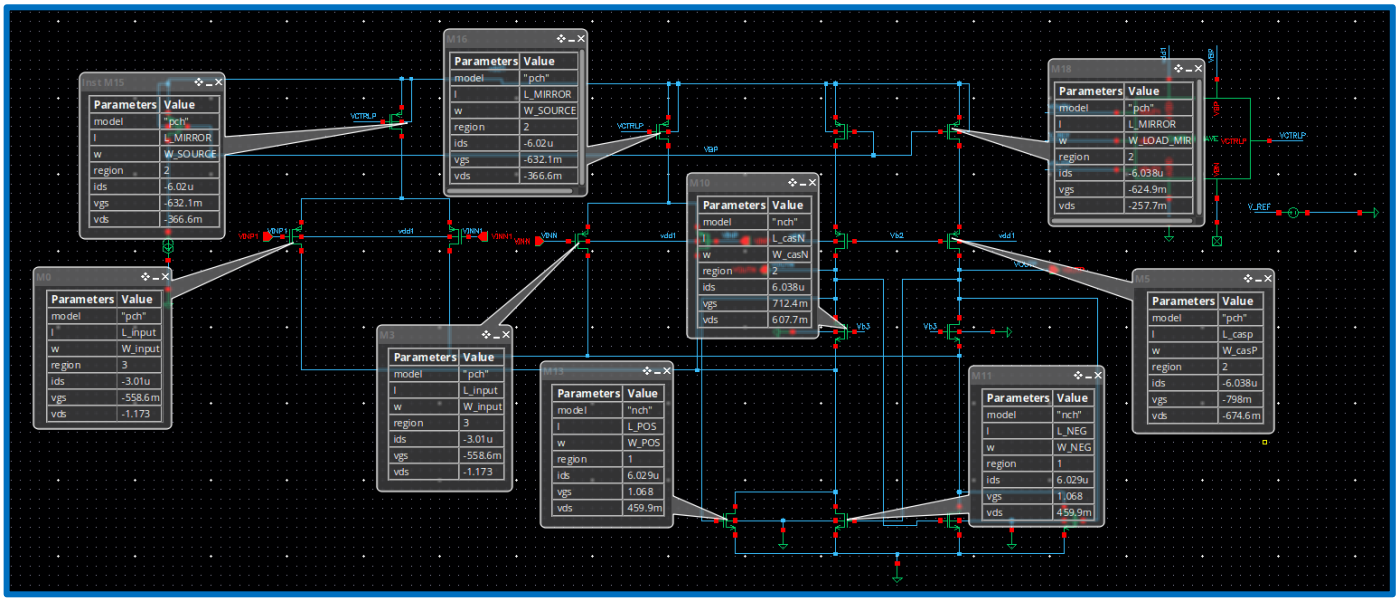
4.Design

4.1 Phase I: Folded OTA Design

Schematic :



Dc analysis :

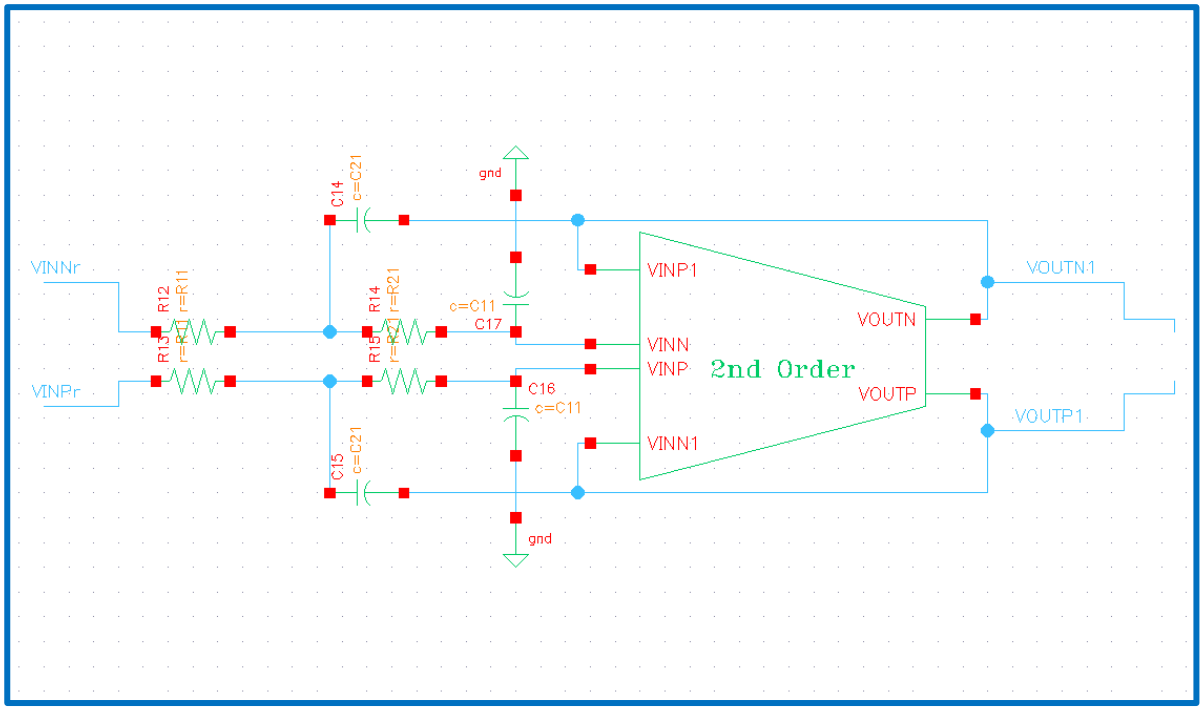


Gain and bandwidth :

Test	Output	Nominal
openloop:1	VF("/VOD")	
openloop:1	bandwidth(VF("/VOD") 3 "low")	8.106M
openloop:1	gainBwProd(VF("/VOD"))	3.216G
openloop:1	ymax(mag(VF("/VOD")))	395.7

4.2 Phase II: 2nd-Order Stage Design

Schematic :



Component design :

we will use Equal R methodology

So,

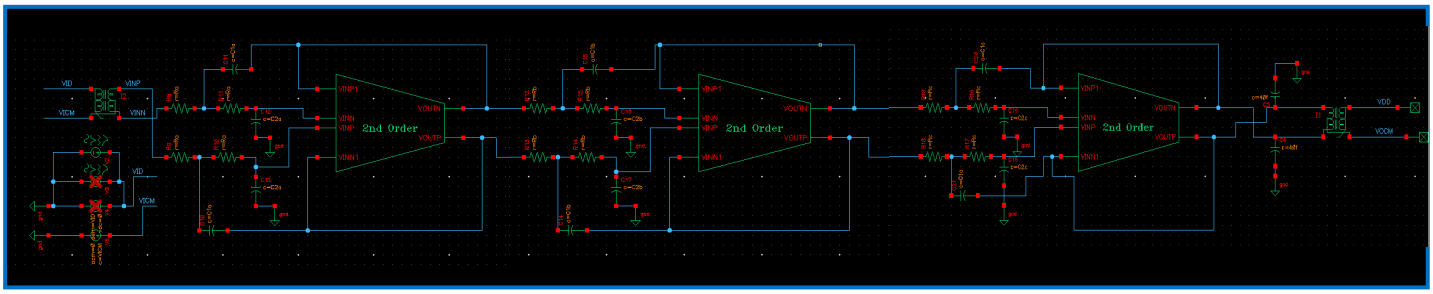
$$\omega_o = \frac{1}{R\sqrt{C_1 C_2}} \; ; \; Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}} \quad \& \quad DC\ gain = K = 1$$

Taking Every suitable Q from this table we were able to calculate every stage componont

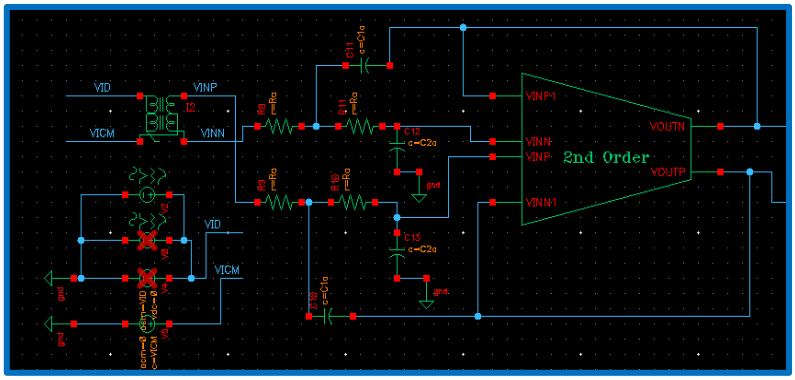
Filter Order	Stage 1		Stage 2		Stage 3		Stage 4		Stage 5	
	FSF	*Q*	*FSF*	*Q*	*FSF*	*Q*	*FSF*	*Q*	*FSF*	*Q*
2	1.000	0.7071								
3	1.000	1.0000	1.000							
4	1.000	0.5412	1.000	1.3065						
5	1.000	0.6180	1.000	1.6181	1.000					
6	1.000	0.5177	1.000	0.7071	1.000	1.9320				
7	1.000	0.5549	1.000	0.8019	1.000	2.2472	1.000			
8	1.000	0.5098	1.000	0.6013	1.000	0.8999	1.000	2.5628		
9	1.000	0.5321	1.000	0.6527	1.000	1.0000	1.000	2.8802	1.000	
10	1.000	0.5062	1.000	0.5612	1.000	0.7071	1.000	1.1013	1.000	3.1969

4.3 Cascading to 6th-Order Filter

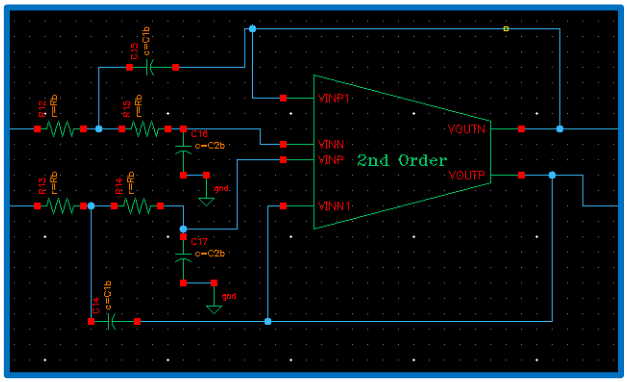
Schematic as one block :



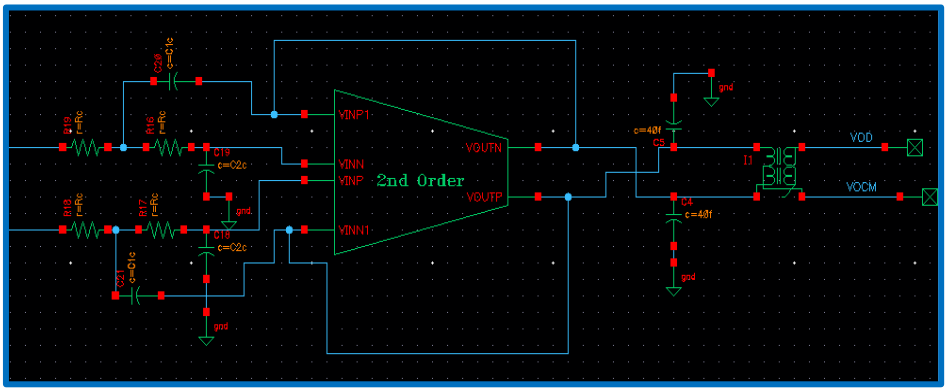
Stage one :



Stage Two :



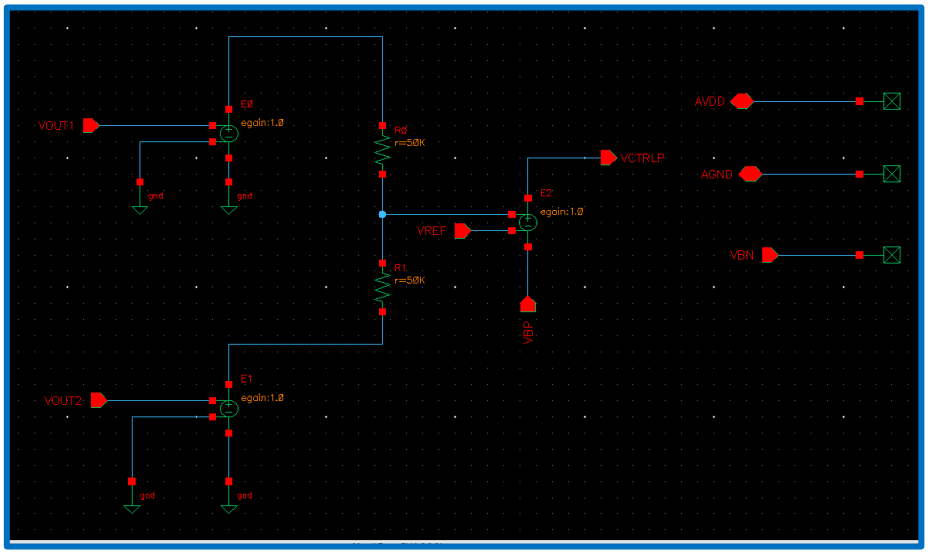
Stage Three :

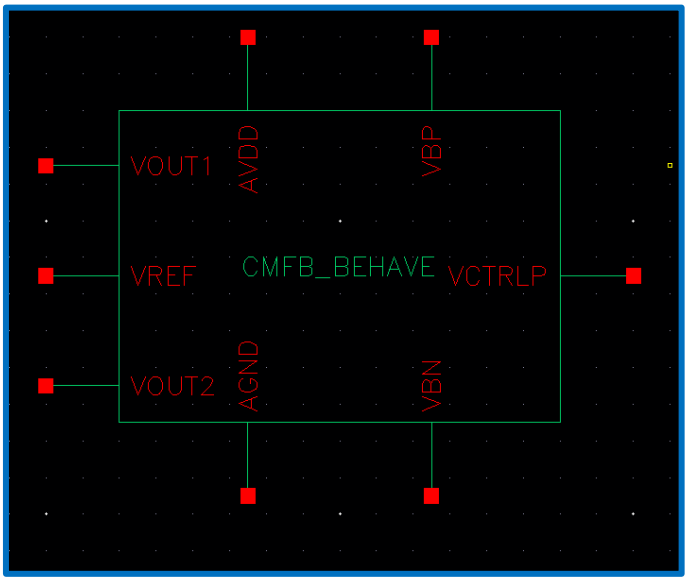


4.4 Common-Mode Feedback :

For now, we will use an ideal CMFB

Schematic :

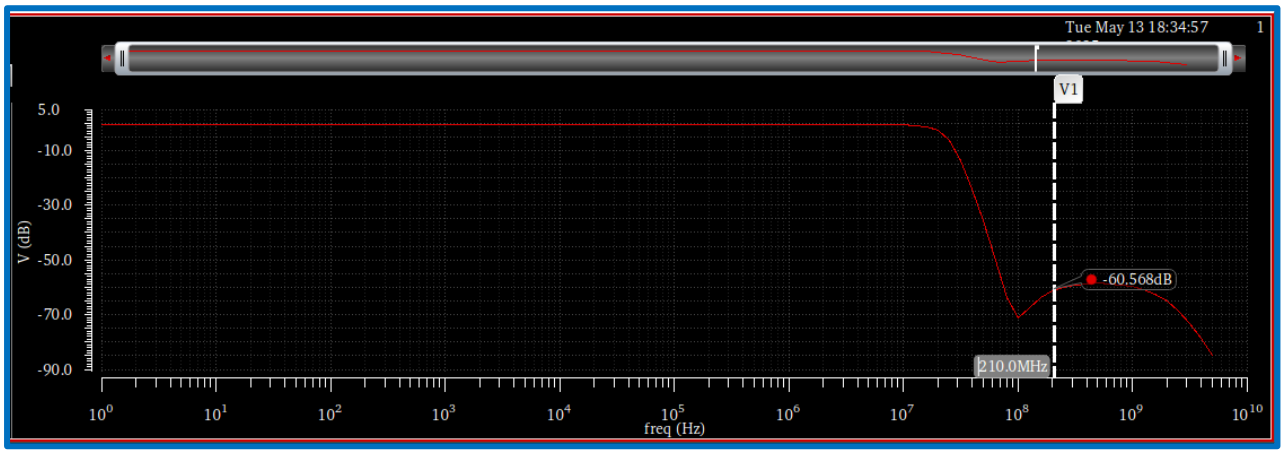




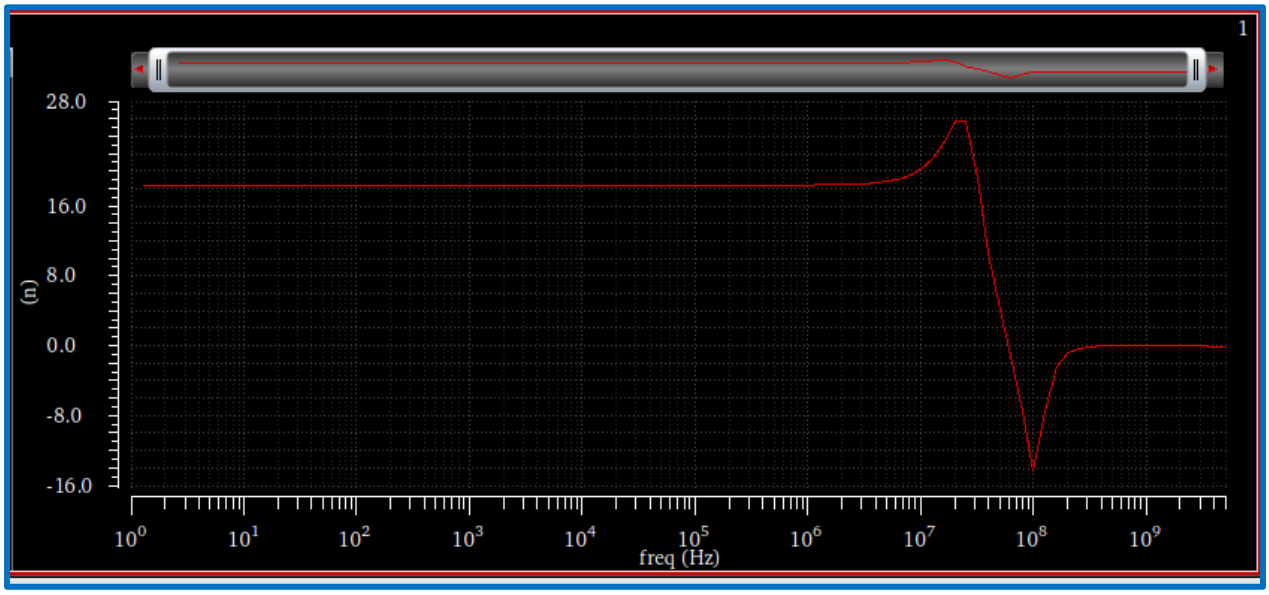
5. Simulation Results

5.1 AC Analysis :

Av (dB) , band of attenuation at 10*BW :



Group Delay :



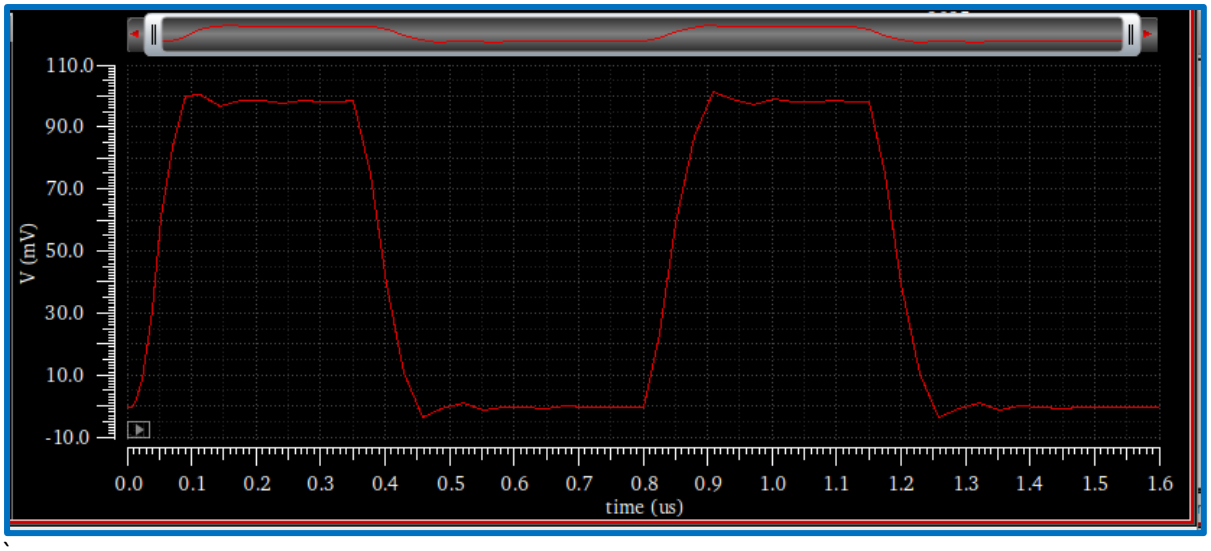
Output Results :

Output	Nominal	Spec	Weight
Av_dB			
BW	21.22M		
GBW	21.06M		
Ymax	991.9m		
GroupDelay			
max_GroupDelay	25.89n		

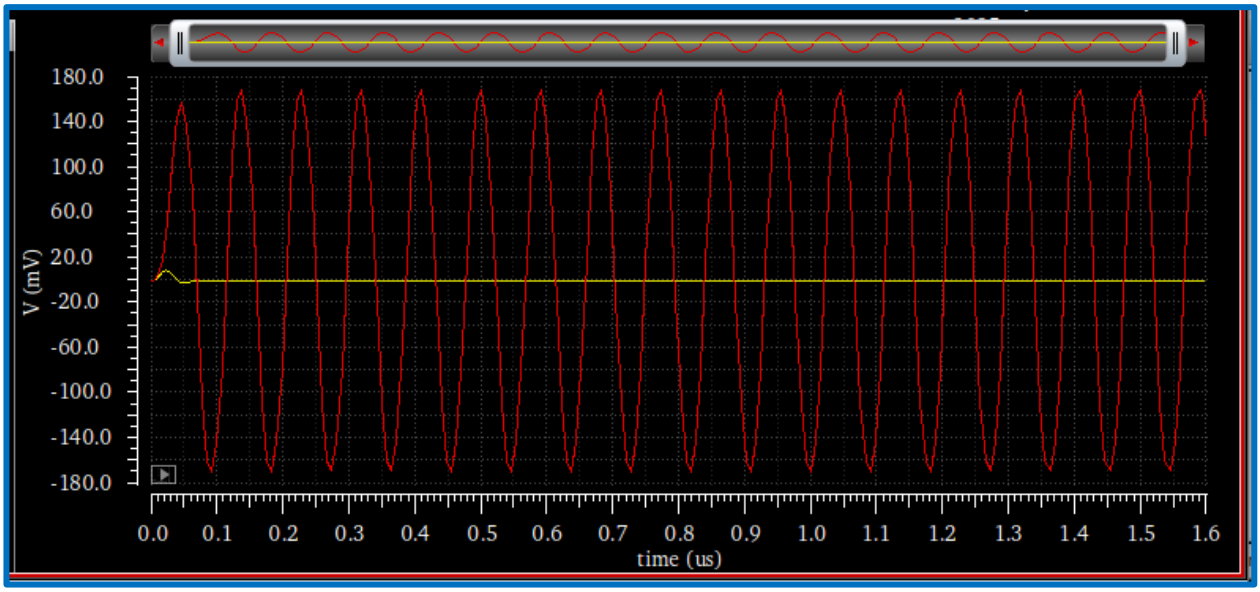
5.2 Transient Analysis :

Output transient response of 200mv input pulse:

Output transient response of 100mv input pulse:



Two Sine Wave signals with 11MHz,210MHz respectively :



6. Next Steps

The design has progressed through the folded implementation, single second-order stage, cascading to form the 6th-order filter, and initial verification via AC and transient simulations. The upcoming tasks focus on completing and validating the design for robust operation and integration:

- **Common-Mode Feedback (CMFB) Design and Integration :**
  Design and integrate the CMFB circuit to ensure stable common-mode voltage levels in the fully differential filter stages. This is essential for reducing distortion, improving common-mode rejection, and maintaining overall stability.
- **Additional Analysis and Verification :**
  Perform further simulations including noise analysis, Monte Carlo process variation, temperature corners, and stability verification. These will help confirm the filter's robustness across all operating conditions.
- **Final Optimization and Documentation :**
  Based on simulation feedback result, fine-tune the design as needed, finalize the documentation.

7. References

1. Hu, Q., Yang, L., & Huang, F. (Year). *A 100-170MHz Fully-Differential Sallen-Key 6th-Order Low-Pass Filter for Wideband Wireless Communication*. Institute of RF- & OE-ICs, Southeast University, Nanjing, China. Email: huquan_ic@163.com

2. Karki, J. (Date). *Active Low-Pass Filter Design*. Texas Instruments, AAP Precision Analog.

3. Sedra, A. S., & Smith, K. C. (2015). *Microelectronic Circuits* (7th Edition). Oxford University Press.

4. Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*. McGraw-Hill.

5. Franco, S. (2014). *Design with Operational Amplifiers and Analog Integrated Circuits* (4th Edition). McGraw-Hill.