Exercise 1 – I/O Port Interfacing

B – The chip doesn't have enough address lines

This is a 16-port I/O chip, so it should have 4 address lines (because $2^4 = 16$). The fourth address line would be labeled "A3" and it would be connected to the "A3" line on the bus.

Exercise 2 – Bus Performance

C – 1000M Bytes/sec

The bus has 32 data lines, so it can move 32 bits (4 bytes) per transfer. The clock speed of the bus allows 250M transfers per second, so the throughput (bandwidth) of the bus is:

250M transfers/sec x 4 bytes /transfer = 1000M bytes/sec

Exercise 3 – Block Transfer Performance

A – 1270 ns (1.27 µsec)

The bus has 32 data lines, so it can move 32 bits (4 bytes) per clock cycle. So transferring 500 bytes will take 500 bytes / 4 bytes per cycle = 125 cycles. We need an additional 2 cycles at the start to set up the block transfer, so it takes a total of 127 clock cycles.

The clock speed of the bus is 100MHz, so each clock cycle takes:

1 / 100 000 000 = 0.000 000 010 sec
= 0.000 010 msec
= 0.010 µsec
= 10 nsec

127 clock cycles at 10nsec per clock cycle means the entire transfer will take 127 x 10 = 1270ns.