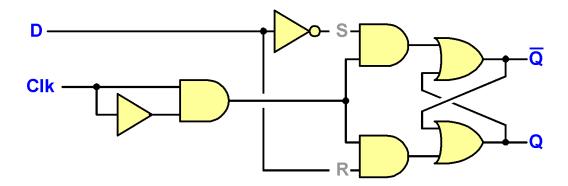
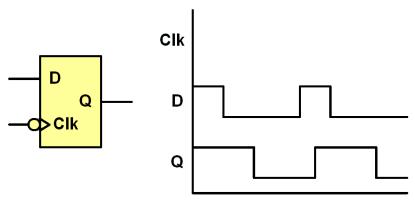
1. Identify the errors in the following edge-triggered D flip-flop:



2. How many transistors does it take to build an edge-triggered D flip-flop?

Assume that the number of transistors needed to build a gate is the same as the number of inputs it has.

3. The timing diagram below shows the relationship between the signals for the flip/flop shown at the left. **Fill in the "Clk" signal** on the timing diagram.



## **COMP 2825 – Computer Architecture**

4. **Draw diagrams** showing the **pins** needed for memory chips with the following organizations:

4M x 1	1M x 4	(using RAS/CAS pins)

5. What are the two major types of RAM (Random Access Memory)?

6. **Why** is dynamic memory slow?

7. What is the difference between PROM and EPROM?