

1. **Which** of the following techniques were used to speed up the MIC-1 microarchitecture?

translating the microinstructions  
adding an instruction fetch unit  
adding a microinstruction fetch unit  
increasing the number of words in the control store  
using a two-bus architecture  
using a three-bus architecture  
eliminating the Main1 microinstruction  
adding registers to the data path

2. **Which** of the following are part of the **Instruction Fetch Unit**?

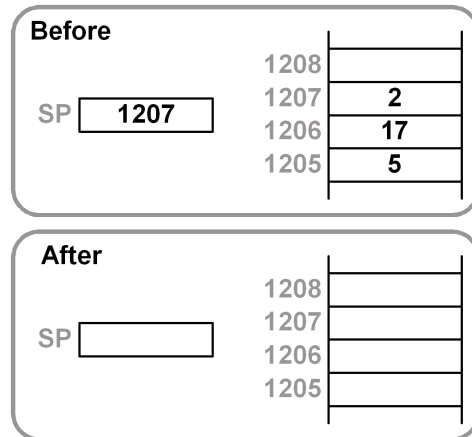
Shift Register  
PC2 Register  
A, B and C Registers

3. **How** was the data path **changed** to turn it into a pipelined microarchitecture?

4. **List** the **four** pipeline stages used in the MIC-3 microarchitecture:

5. (a) The MIC-2 microcode below implements an IJVM instruction. If the stack was in the “before” state shown at right, **fill in the “after” state** of the stack to show what the microcode does.

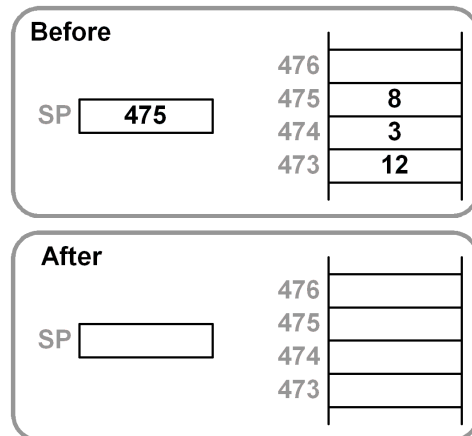
xxx1    **MAR = SP – 1; rd**  
 xxx2    **MAR = SP**  
 xxx3    **H = MDR; wr**  
 xxx4    **MDR = TOS**  
 xxx5    **MAR = SP – 1; wr**  
 xxx6    **TOS = H; goto (MBR1)**



- (b) What is the name of the IJVM instruction that this microcode implements?

6. (a) The MIC-3 microcode below implements an IJVM instruction. If the stack was in the “before” state shown at right, **fill in the “after” state** of the stack to show what the microcode does.

- (b) What is the name of the IJVM instruction that this microcode implements?



Load ALU Inputs	Execute ALU Function	Store ALU Results
A = SP		
A = TOS	C = A + 1	
	C = A	SP = MAR = C
		MDR = C; wr; goto (MBR1)