

1. What **two** types of **locality** make cache systems effective?
  
  
  
  
  
  
  
  
  
  
2. What **three things** are stored in every line of a cache system?
  - a)
  - b)
  - c)
  
  
  
  
  
  
  
  
  
  
3. When a memory address is sent to a cache system it's broken up into three pieces which are used to search the for data. What are the **names** of these three fields?
  - a)
  - b)
  - c)
  
  
  
  
  
  
  
  
  
  
4. A system with a capacity of 4GBytes uses a two-way set associative cache that has 4096 lines and 32 bytes per line.
  - a) How large is the cache (in bytes)?
  
  
  
  
  
  
  
  
  
  
  - b) Draw a diagram of how the memory address is used by the cache.
  
  
  
  
  
  
  
  
  
  
5. **Why** doesn't a direct-mapped require a **cache replacement policy**?

6. A computer system stores 3 bits per jump instruction for a Finite State Machine which does dynamic branch prediction.

a) **How many circles** will the Finite State Machine's diagram have on it?

b) **How many arrows** will the Finite State Machine's diagram have on it?

7. In each of the pairs of the instructions below, **identify** what kind of **dependency** would keep the second instruction from executing at the same time as the first instruction:

$R4 = R3 + R2$ $R2 = R5 * R3$

$R3 = R0 + R7$ $R5 = R3 - R4$

$R5 = R0 + R3$ $R5 = R0 - R3$

8. Which of the dependencies in question 7 could be eliminated through the use of **Register Renaming**?

9. A system using Superscalar Execution has a scoreboard in the following state:

Read Counts								Write Counts							
R0	R1	R2	R3	R4	R5	R6	R7	R0	R1	R2	R3	R4	R5	R6	R7
0	1	0	3	0	0	2	0	1	0	0	0	0	1	0	0

Assuming that there are no hidden registers, **circle the instructions below** which **could** be issued with the scoreboard in this state.

$R2 = R3 + R7$	$R6 = R4 + R7$	$R7 = R2 + R4$
$R4 = R1 - R5$	$R5 = R2 * R4$	$R4 = R5 + R7$

10. **Which architectural level** of a computer system is the boundary between the CPU **hardware** and the **software** that runs on it?

11. Circle the words below which are characteristics of the Instruction Set Architecture level of a computer system:

Memory Model	Performance	Data Types
Pipeline Stages	Registers	Instructions

12. A computer system requires all memory accesses be **aligned** on **4-byte boundaries**. **Circle** the hexadecimal addresses below that would cause an **error**:

2F0D	7598	0000
333C	2086	FFFF

13. **What** is the **Harvard Architecture**?

14. What is the **difference** between **User Mode** and **Kernel Mode**?

15. In the UltraSPARC architecture, what value does the R0 register hold?

16. How many bits are there in the registers for the:
- a) Pentium-4
  - b) UltraSPARC III
17. What are the names of the registers which hold the following information in a typical computer system?
- a) The address of the next instruction to be executed.
  - b) The address of the top word on the stack
  - c) The address of the area holding the local variables for the current procedure.
  - d) The state of the last ALU operation.