Exercise 1 – NAND Latch

1. **A** – **TRUE**

   We don't know the bottom input for the top NAND gate, but from the truth table we can see that if either input is FALSE then the output must be TRUE. Since NOT-S is FALSE, this means the output must be TRUE.

2. **B** – **FALSE**

   Since the TRUE output from the top NAND gate is connected to the top input of the bottom NAND gate, and since the NOT-R input is TRUE, we can tell that both inputs to the bottom NAND gate are TRUE. This means the output of the bottom NAND gate is FALSE.

Exercise 2 – NAND Latch

1. **A** – **TRUE**

   We don't know the top input for the bottom NAND gate, but from the truth table we can see that if either input is FALSE then the output must be TRUE. Since NOT-R is FALSE, this means the output must be TRUE.

2. **B** – **FALSE**

   Since the TRUE output from the bottom NAND gate is connected to the bottom input of the top NAND gate, and since the NOT-S input is TRUE, we can tell that both inputs to the top NAND gate are TRUE. This means the output of the top NAND gate is FALSE.

Exercise 3 – Edge vs. Level Triggering

B For a positive level-triggered latch, the output is the same as the input as long as the clock signal is TRUE (high). When the clock signal is FALSE (low), the output remains unchanged, even if the D input changes. The B output line is the only one that follows these rules.

Exercise 4 – Edge vs. Level Triggering

D For a positive edge-triggered flip-flop, the latch is loaded only at the instant the clock changes from FALSE to TRUE (low to high transition). At that instant the output of the flip-flop will change to match the state of the D input. The changes in the D output line follow this pattern. The reason the line doesn't change at the first low-to-high clock transition is because the flip-flop had a FALSE value before that instant and the D input was also FALSE – so the new value loaded into the flip-flop was the same as the old one.

Exercise 5 – Edge vs. Level Triggering

C For a negative level-triggered latch, the output is the same as the input as long as the clock signal is FALSE (low). When the clock signal is TRUE (high), the output remains unchanged, even if the D input changes. The C output line is the only one that follows these rules.

Exercise 6 – Edge vs. Level Triggering

A For a negative edge-triggered flip-flop, the latch is loaded only at the instant the clock changes from TRUE to FALSE (high to low transition). At that instant the output of the flip-flop will change to match the state of the D input. The changes in the A output line follow this pattern.

Exercise 7 – Memory Circuit

1. **A** – **Reading**

   The CS input is TRUE so the chip is activated. This TRUE input activates the first two green AND gates it's connected to, one of which will have a TRUE output depending on the state of the RD/NOT-WR signal. The RD/NOT-WR signal is also TRUE, so it's the bottom of those two green gates which is turned on. This enables the output two tri-state buffers (bottom green triangles) to pass the output of the selected flip-flops to the D0 and D1 connections of the chip.

2. **B** – **Upper-right flip-flop**

   The D0 output is connected to the right column of flip-flops and the A0/A1 inputs control which row of those is selected. Both A0 and A1 are FALSE – this means that of the four orange AND gates only the top one outputs TRUE (because the two FALSE A0/A1 signals are inverted before reaching that gate). This TRUE output turns on both of the yellow AND gates it's connected to, allowing the output of the A and B flip-flops to pass through to the D1 and D0 outputs.

Exercise 8 – Memory Pinouts

1. **C**

   A chip with 1K (1024) addresses must have 10 address signals because $2^{10} = 1024$. And since it's 1K x 4, it must have four data connections. Note that chip "A" has 11 address connections, not 10.

2. **B** – **1M x 4**

   This chip has 10 address connections (A0-A9), but it also has NOT-RAS and NOT-CAS connections. This means that the address is sent to the chip in two 10-bit parts, which means the address is actually 20 bits long. Since 2^{20} = 1M (1024 x 1024 or 1,048,576), and since the chip has only 1 data connection, it's organization is "1M x 4"