COMP 2825 – Computer Architecture

Review Solutions – Week 10

1. What **two** types of **locality** make cache systems effective?

   <u>Spatial</u> locality and <u>Temporal</u> locality

2. What **three things** are stored in every line of a cache system?

   a) **Valid Bit**

   b) **Tag**

   c) **Data**

3. When a memory address is sent to a cache system it's broken up into three pieces which are used to search the for data. What are the **names** of these three fields?

   a) **Tag**

   b) **Line number**

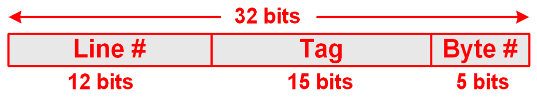
   c) **Byte number**

4. A system with a capacity of 4GBytes uses a two-way set associative cache that has 4096 lines and 32 bytes per line.

   a) How large is the cache (in bytes)?

   4096 lines x 32 bytes/entry = 131,072 bytes (128K bytes)
   2-way set associative has 2 entries per line, so
   2 x 128K bytes = <u>256K bytes</u>

   b) Draw a diagram of how the memory address is used by the cache.



5. **Why** doesn't a direct-mapped require a **cache replacement policy**?

   A direct-mapped cache has only one entry per cache line.

   (Only a set-associative cache has more than one entry per cache line. When new data is loaded, the cache needs to choose which entry to use – the "cache replacement policy" dictates how that choice is made.

   Since a direct-mapped cache has only one entry, no choice is needed.)

6. A computer system stores 3 bits per jump instruction for a Finite State Machine which does dynamic branch prediction.

   a) **How many circles** will the Finite State Machine's diagram have on it?

   8 circles (because 2^3 = 8 states, and 1 state per circle)

   b) **How many arrows** will the Finite State Machine's diagram have on it?

   16 arrows (because each state has a "Jump" and "No Jump" transition leading from it to another state

7. In each of the pairs of the instructions below, **identify** what kind of **dependency** would keep the second instruction from executing at the same time as the first instruction:

R4 = R3 + $\boxed{\text{R2}}$ $\boxed{\text{R2}}$ = R5 * R3	$\boxed{\text{R3}}$ = R0 + R7 R5 = $\boxed{\text{R3}}$ – R4	$\boxed{\text{R5}}$ = R0 + R3 $\boxed{\text{R5}}$ = R0 – R3
WAR – Write After Read	**RAW – Read After Write**	**WAW – Write After Write**

8. Which of the dependencies in question 7 could be eliminated through the use of **Register Renaming**?

   WAR and WAW – both "Write After" dependencies can be eliminated by storing the result in a different (hidden) register.

9. A system using Superscalar Execution has a scoreboard in the following state:

Read Counts								Write Counts							
R0	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R0**	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**
0	1	0	3	0	0	2	0	1	0	0	0	0	1	0	0

Assuming that there are no hidden registers, **circle the instructions below** which **could** be issued with the scoreboard in this state.

[✓ R2 = R3 + R7]	R6 = R4 + R7	[✓ R7 = R2 + R4]
R4 = R1 – R5	R5 = R2 * R4	R4 = R5 + R7

10. **Which architectural level** of a computer system is the boundary between the CPU **hardware** and the **software** that runs on it?

    The <u>Instruction Set Architecture</u> level.

11. Circle the words below which are characteristics of the Instruction Set Architecture level of a computer system:

[✓ Memory Model]	Performance	[✓ Data Types]
Pipeline Stages	[✓ Registers]	[✓ Instructions]

12. A computer system requires all memory accesses be **aligned** on **4-byte boundaries**. **Circle** the hexadecimal addresses below that would cause an **error**:

[✓ 2F0D]	7598	0000
333C	[✓ 2086]	[✓ FFFF]

13. **What** is the **Harvard Architecture**?

    A memory system which uses completely separate memories and address spaces for instructions and data.

14. What is the **difference** between **User Mode** and **Kernel Mode**?

    Kernel mode can access all ISA features, but User Mode isrestricted to only those instructions which cannot affect the state of the operating system or other programs.

15. In the UltraSPARC architecture, what value does the R0 register hold?

    0 (zero)

16. How many bits are there in the registers for the:

    a) Pentium-4

    32 bits

    b) UltraSPARC III

    64 bits

17. What are the names of the registers which hold the following information in a typical computer system?

    a) The address of the next instruction to be executed.

    Program Counter (PC) or Instruction Pointer (IP)

    b) The address of the top word on the stack

    Stack Pointer (SP)

    c) The address of the area holding the local variables for the current procedure.

    Frame Pointer, Base Pointer, Local Variable Pointer (FP / BP / SP)

    d) The state of the last ALU operation.

    Flags or Status register