NAME: _____

(50 marks total)

This is an individual assignment. You may collaborate with others from your class, but your answers must demonstrate significant individual effort differentiating them from others' work.

1. A graphics program is drawing an image on the screen. The program is running on a multilevel computer system with the following characteristics:
   - The transistors in the computer have a switching delay of 20ps (ie, it takes 20ps for a transistor to switch from ON to OFF or vice versa).
   - The maximum clock speed of the computer system is limited by the need to wait for switching to occur through 15 transistors (ie, transistor 1 switches, then transistor 2, then transistor 3, etc.) In other words, shortest clock cycle is the amount of time it takes a transistor to switch on or off 15 times.
   - At the microarchitecture level, one microinstruction can be executed on each clock cycle.
   - It takes an average of 3 microinstructions to execute each ISA level instruction.
   - Each instruction at the Assembly Language level is equivalent to exactly one ISA level instruction (except for those that call the Operating System as described below).
   - An average of 5% of the Assembly Language instructions are call instructions which request the Operating System routines to display pixels. Each of these call instructions requires an additional 180 ISA level instructions to be executed by the Operating System.
   - The high-level language that the graphics program is written in requires an average of 3 Assembly Language instructions for each high-level language statement.
   - It takes 20 high-level language statements to display a single pixel in the image.
   - The image being displayed is 1000 pixels across by 500 pixels vertically.

   a) How long does it take to display the image? Show your calculations. (4 marks)

   b) This CISC architecture is replaced by a RISC architecture which is the same in all respects, except that it does not use microinstructions and can execute each ISA instruction in a single clock cycle. But because only very simple ISA instructions are supported, it takes an average of 6 Assembly Language instructions for each high level language statement. How long will it take this system to recalculate the spreadsheet? (2 marks)

   c) What is the maximum clock speed of this systems (in MHz)? (1 mark)

2. The following diagram shows the **hexadecimal** contents of several memory cells:

Memory Contents	2F	1C	04	9D	37	5E	42	86	01	57	
Memory Address	4C1F	4C20	4C21	4C22	4C23	4C24	4C25	4C26	4C27	4C28	

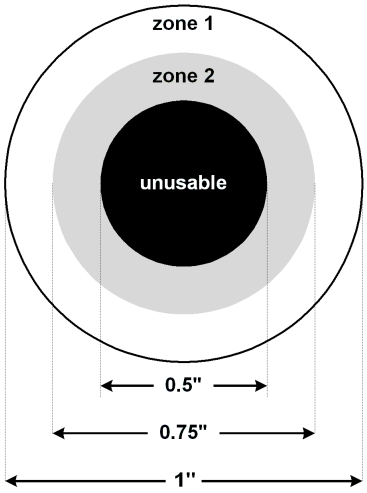
Write the **decimal values** of the following numbers (2 marks each):

a) The **2-byte number** stored in **Little-Endian** format at memory address **4C26:**

b) The **4-byte number** stored in **Big-Endian** format at memory address **4C20**:

3. The largest flash memory devices that are widely available hold around 16GBytes of information. Assuming that Moore's Law continues to hold, plot the expected capacity of the largest flash memory devices over the next 15 years [Hint: calculate the 2023 value first so you know what the maximum vertical scale should be] (2 marks):

4. You're designing a disk drive and are limited by the following factors:



- The magnetic head and oxide coating technology permits a maximum linear bit density of 2,000,000 bits/inch along a track.
- The head positioning technology restricts the tracks to being no closer than 25 microinches apart. This means the centerline of one track will be 25 microinches from the centerline of the next.
- The drive uses disks that are 3" in diameter.
- The hub of the disk is 1" in diameter (in other words, the innermost tracks on the disk will be 1" in diameter)
- To increase capacity, the drive will contain two zones as shown in the diagram. All tracks in a given zone have the same number of sectors per track which is different than the number of sectors per track in the other zones.
- The intersector gaps will be the equivalent of 500 bits long.
- Each sector requires an additional 800 bits for header information and ECC (error correcting codes).

a) If the drive has one platter and if each sector holds 512 bytes, **how much data will your disk be able to hold**? Show your calculations (5 marks)

b) What will the be the **maximum transfer rate** for the drive if it spins at 5,400 rpm? (2 marks)

c) **If your disk only had one zone** with the same number sectors per track for the whole disk, what would be the new **disk capacity** and **maximum transfer rate**? (2 marks)

d) **For the three-zone disk**, if you **increase the sector size to 1024 bytes**, what will the new **capacity** and **transfer rate** of the disk be (assume the same number of bits for the gap size and ECC) (2 marks)

5. A web server handles queries from a database. The most recent queries are stored in main memory to so that they can be satisfied quickly. If not found in memory, the queries are read from disk. The disk is a Hybrid Hard Drive (HHD) which uses 4GB of flash memory as a cache for information stored on the actual disk platters. The access times and hit rates of the subsystem are as follows:

Storage	**Access Time**	**Hit Rate**
Main Memory	50ns	50%
HHD Flash Memory	10µs	80%
Hard Disk Platters	10ms	100%

Answer the following questions:

a) What is the **average access time** for the system? Show your calculations. (3 marks)

b) **How much does the HHD Flash Memory speed the system up?** (For example, if a system without the Flash Memory has an average access time of 100ns and a system with it has an average access time of 50ns, the L2 cache speeds the system up by 100ns / 50ns = 2X) (2 marks)

c) What would the **Flash Memory hit rate** have to be in order to achieve an average access time of **10.05µs**? (3 marks)

6. "Blu-ray" drives use blue lasers and data packed much more densely to store up to **50GB** on a 2-layer disc. They hold high definition movies recorded using **true colour** with a resolution of **1920 x 1080**. The movies are compressed to fit in the available space.

   a) If the 50GB disc can exactly hold a compressed 3-hour movie, **how quickly** (in bytes/sec) must the compressed data be read from the drive in order to play the movie at normal speed? (1 mark)

   b) If the movie contains 30 frames per second, **how much raw data** (in bytes) must be sent to the display each second after the information read from the drive is decompressed? (1 mark)

   c) Based on your answers above, what must the **compression ratio** be for this movie? (1 mark)

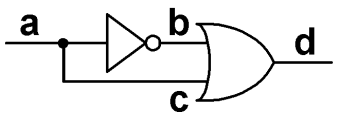
   d) If the movie was **not** compressed, **how much storage** would it require? (1 mark)

7. Examine the **8-bit shifter** circuit shown in the Week 3 presentation material.

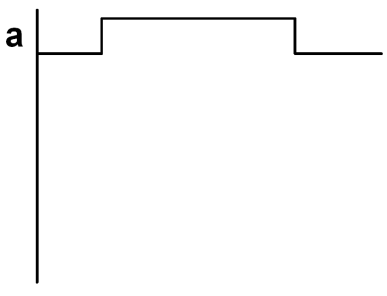
   a) **How long would it take** for the shifter to produce a result assuming the following: (1 mark)
   - All 8 bits of the input number and the "left or right" control signal are all applied at the same time
   - It takes 0.1ns for a signal to pass through any logic gate
   - It takes no time for a signal to travel along the wires from one logic gate to the next one.

   b) Would this be faster or slower than an 8-bit adder circuit? Why? (1 mark)

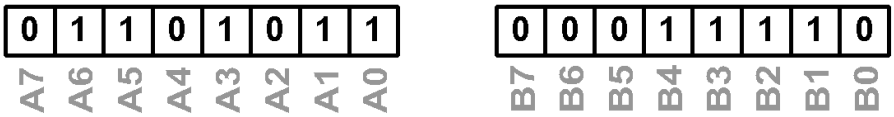
8. At right is a pulse generator circuit which is similar to the one shown on page 162 of the textbook, except that it uses an "OR" gate instead of an "AND" gate:



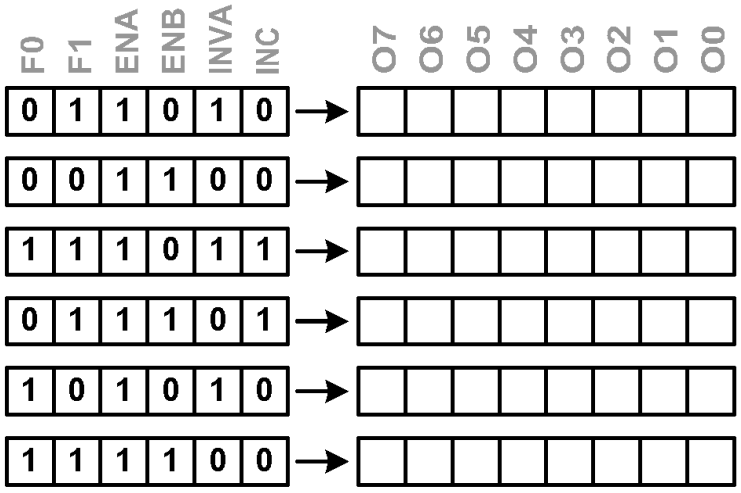
   Draw a timing diagram similar to the one in textbook figure 3-25 (b) to show how the circuit operates (3 marks)



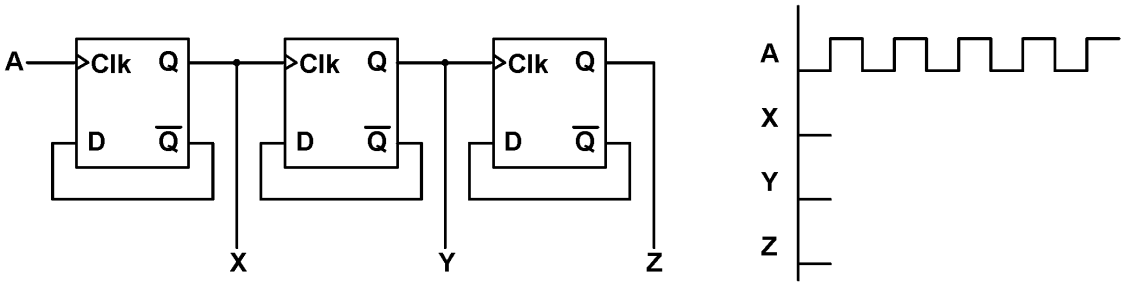
9. An 8-bit ALU is built from bit slices as shown on page 156 of the textbook. The following two numbers are present at the data inputs of the ALU:



Show the output produced by the ALU for these input values and the following combinations of control inputs: (3 marks)



10. Three **D flip-flops** are connected as shown below. Each flip-flop has it's **data input** connected to it's own **NOT-Q output**. **Fill in the timing diagram** at the right to show how the output of the flip-flops change. Assume that all thee flip-flops start with their Q outputs in the FALSE state. (3 marks):



11. **Design a circuit** to do a **2's-complement operation** on a 4-bit number **using as few gates as possible**. The circuit will have 4 inputs (the 4-bit number) and 4 outputs (the 4-bit result). For example, if the input number is "0100" (decimal 4), the output should be "1100" (decimal -4). (3 marks)