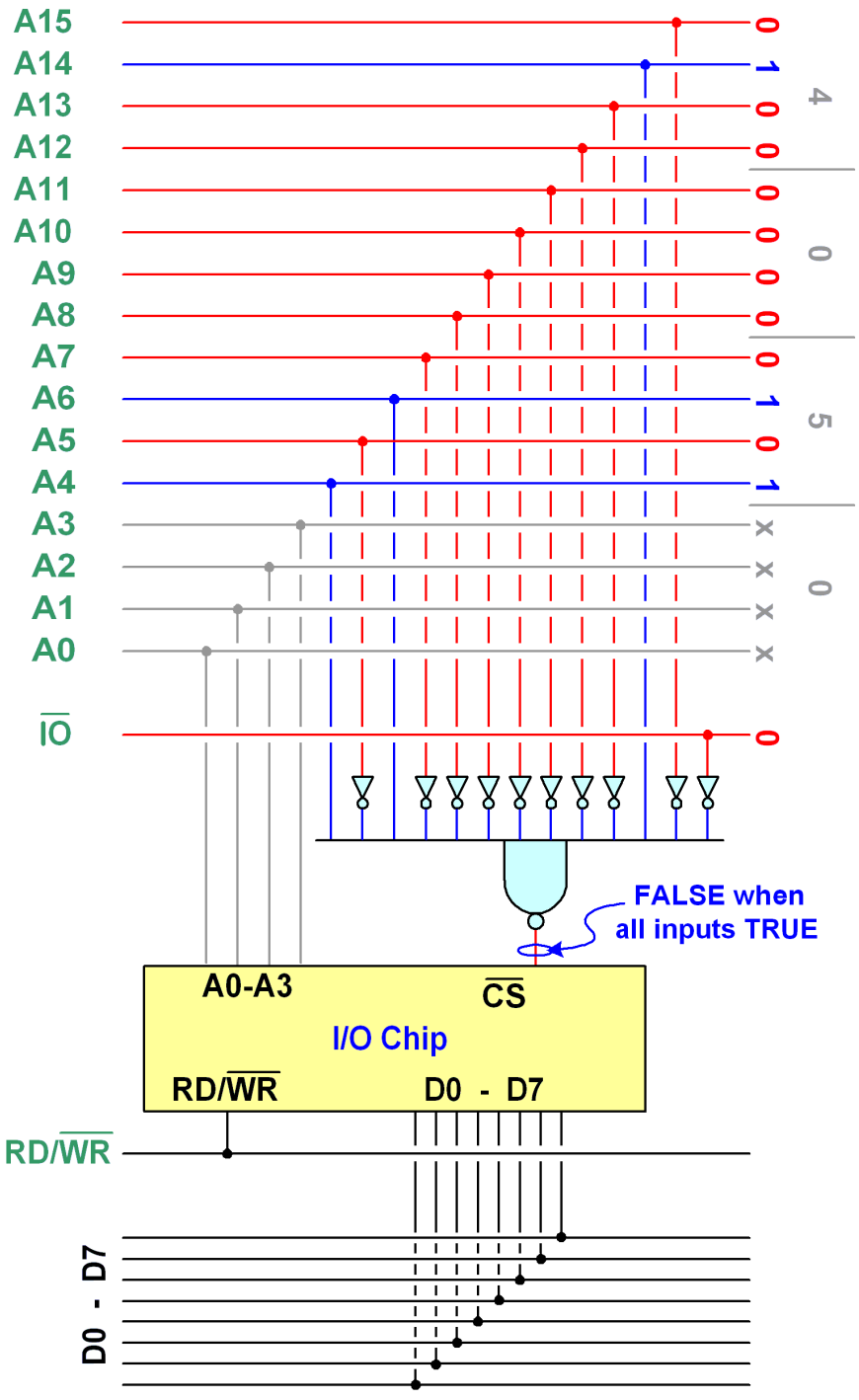
1. **Connect the following I/O chip** to the bus using **full decoding logic** which gives the I/O ports addresses starting with hex **4050**:



Circle **ALL of the correct answers** for **each** question below (1 mark each):

2. Computer systems can include the following **types of buses**:
- [a.] Embedded
- b. Silicon
- c. Software
- [d.] Memory
- [e.] I/O

3. The following **system buses** have been used in microcomputer systems:
- [a.] AGP
- b. ASCII
- [c.] ISA
- d. DDR
- [e.] PCI

4. The **performance** (it's transfer capacity in bytes/second) of a **system bus** can be improved by:
- [a.] Increasing the clock speed of the bus
- [b.] Increasing the number of data wires in the bus
- c. Increasing the number of address wires in the bus
- d. Increasing the number of control wires in the bus
- e. Increasing the number of devices connected to the bus

5. An **asynchronous system bus**:
- a. Uses a clock signal to coordinate the signals flowing across the bus
- [b.] Uses special synchronization signals such as "Master Synch" and "Slave Synch" for coordination
- [c.] Can perform each bus transaction as quickly as the bus slave is able to handle the data
- d. Has a WAIT signal which can be asserted if the bus slave can't respond quickly enough
- e. Is easier to design and more commonly used than a synchronous bus

6. A Bus **Master**:
- [a.] Can send data to a bus slave
- [b.] Can receive data from a bus slave
- c. Decides which device will take control of the bus
- [d.] Can move data to or from memory without the intervention of the CPU
- e. Is always associated with a particular bus slave

7. The following bus signals are associated with **Bus Arbitration**:
- a. Memory Request
- b. I/O Request
- [c.] Bus Grant
- [d.] Bus Request
- e. Reset

8. Which of the following are true with regard to the handling of **Interrupts**:
- a. The CPU can send an interrupt signal to an I/O device to interrupt what it is doing
- [b.] An I/O device can send an interrupt signal to the CPU to interrupt what it is doing
- c. An I/O device can send an interrupt signal to memory to interrupt what it is doing
- [d.] The CPU uses an Interrupt Vector Table when an interrupt occurs
- [e.] When an interrupt occurs, an Interrupt Service Routine is invoked to handle it

9. The Pentium-4 uses a **pipelined bus**. Pipelining of signals on the bus is possible because:
a. The Pentium-4 uses negative logic signals
b. The Pentium-4 uses multiplexed address and data signals
c. The Pentium-4 has different pins for signals used in the different stages of the pipeline
d. The Pentium-4 uses the same pins for signals used in the different stages of the pipeline
e. Bus transactions don't last very long.

10. The following types of devices are connected to a **PCI bus** in a typical desktop computer system:
a. CPU
b. Memory
c. Keyboard **(none of these are normally connected directly to the PCI bus)**
d. Mouse
e. Modem

11. Newer versions of the **PCI bus** include:
a. PCI-Wireless
b. PCI Serial
c. PCI Express
d. PCI Parallel
e. PCI-X

12. A **block transfer** on a computer bus:
a. Occurs when the bus is already in use by another device
b. Performs multiple data transfers
c. Performs multiple address transfers
d. Can be performed in a single bus cycle
e. Is faster than using individual read or write cycles to transfer data

13. The following types of devices are connected to a **USB bus** in a typical desktop computer system:
a. CPU
b. Memory
c. Keyboard
d. Mouse
e. Modem

14. **USB V2** operates at the following **speed**:
a. 1.5MByte/sec
b. 12MByte/sec
c. 60MByte/sec
d. 133MByte/sec
e. 480MByte/sec

15. **New versions** of the **USB** standard include the following:
a. USB-Link
b. USB-Parallel
c. USB On the Go
d. WiFi USB
e. Wireless USB