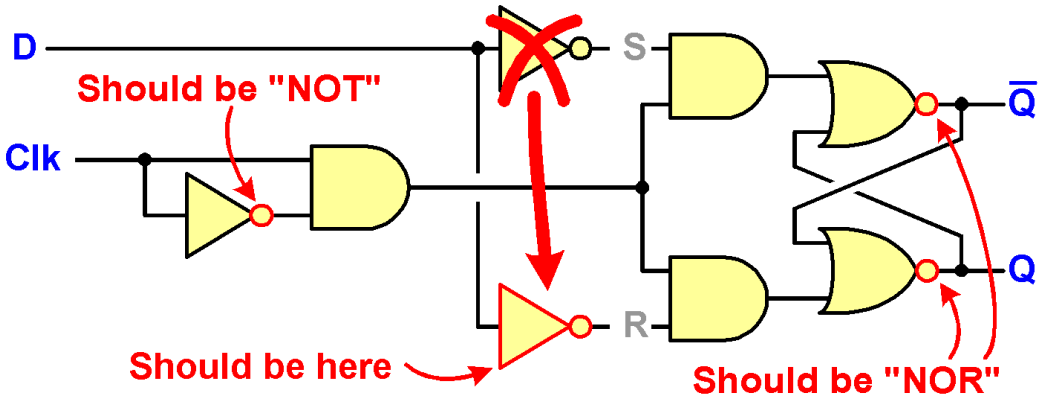
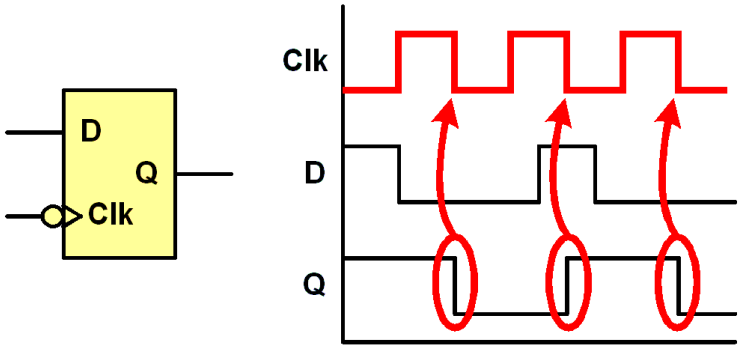
1. Identify the errors in the following edge-triggered D flip-flop:



2. How many transistors does it take to build an edge-triggered D flip-flop? Assume that the number of transistors needed to build a gate is the same as the number of inputs it has.

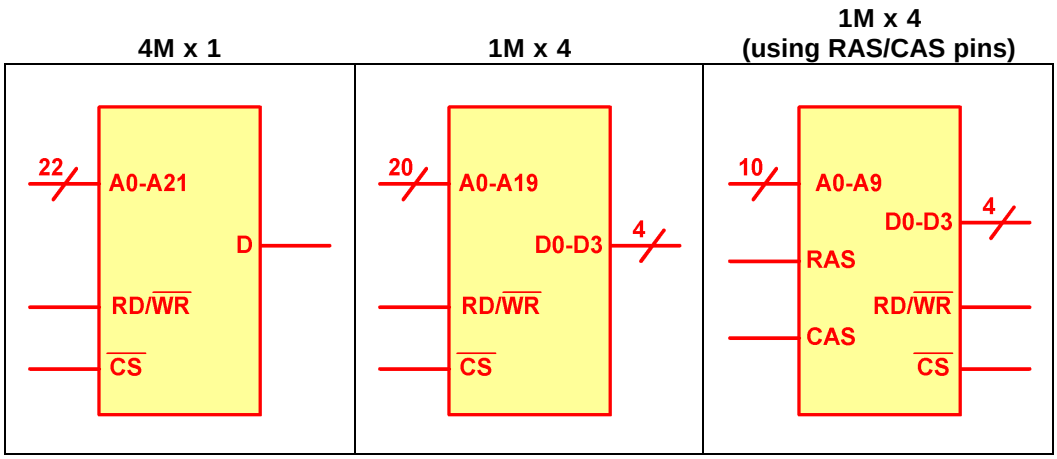
2 NOR gates X 2 transistors/gate = 4 transistors
3 AND gates X 2 transistors/gate = 6 transistors
2 NOT gates X 1 transistor/gate = 2 transistors
Total = 4 + 6 + 2 = 12 transistors

3. The timing diagram below shows the relationship between the signals for the flip/flop shown at the left. **Fill in the "Clk" signal** on the timing diagram.



Negative edge triggered, so Q can only change on trailing edge of clock...

4. **Draw diagrams** showing the **pins** needed for memory chips with the following organizations:



5. **What are** the two major types of RAM (Random Access Memory)?

Static RAM (SRAM), and
Dynamic RAM (DRAM)

6. **Why** is dynamic memory slow?

because the memory contents need to be constantly refreshed, and it can't be access while refreshing.

7. **What is the difference** between **PROM** and **EPROM**?

PROM can be programmed only once,
EPROM can be erased and reprogrammed many times