A method to remove odd harmonic interferences in square wave reference digital lock-in amplifier

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Digital lock-in amplifier using square wave reference is much easier to be implemented compared to digital lock-in amplifier using sinusoidal wave reference. However, because of the odd harmonics containing in the square wave reference, the interferences at the odd harmonics of the reference cannot be removed with conventional algorithm. A new square wave digital lock-in algorithm is presented in this paper. It cannot only be capable of removing the interferences of the odd harmonics in the signal, but also can detect the amplitudes and the phases of the interferences. The real and imaginary parts of the frequency component of interest and those of the odd harmonic interferences are calculated simultaneously. The results of simulation experiments show the feasibility of the proposed algorithm. The algorithm is computationally efficient and thus suitable for weak signal detection implemented in the general microprocessor. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4792596]

I. INTRODUCTION

The lock-in amplifier is well known for its performance in measuring weak alternating current (AC) signals, even when these signals are obscured by high level of noise.[1] It has been widely applied to a variety of fields[2–9] such as impedance measurement, bio-signal measurement, optical spectroscopy, and so on. The phase sensitive detector (PSD), which can select a specific component of the signal at a given frequency, is of great importance for a lock-in amplifier. Lock-in amplifiers can be categorized into two types, analog lock-in amplifiers (ALIA) and digital lock-in amplifiers (DLIA), based on the different implementations of PSD.[10] Both analog and digital PSDs need reference signals at the frequency of interest which are continuously multiplied with the detected signal. In analog PSDs, the multiplications are implemented in analog multipliers and then the results are filtered by low-pass filters. While in DLIAs, signals are sampled by analog-to-digital converters (ADC) and the digitalized values are multiplied with the reference wave sequences mathematically in microprocessors, where the phase-sensitive detections can thus be realized. The digital lock-in amplifier outperforms its analog counterpart because of the absence of output offset, the absence of gain error and so on.

There are two kinds of reference signals in use: the sinusoidal wave and the square wave. In DLIAs with sine wave reference, the reference sequences need to be computed or stored ahead in the read only memory (ROM) by the microprocessor. It is time-consuming to perform the multiplications between the reference wave and the signal for general microprocessors. A variety of approaches improving the performance of the DLIA have been reported.[11–16] Among these, methods making the computation process in DLIAs more efficient are particularly important. Masciotti *et al.*[11] improved the speed of digital lock-in detection for multiple modulated sources using matrix multiplication on a personal computer. In our previous work,[15] we designed an algorithm that combines oversampling and digital lock-in amplifier. The sampling frequency is configured as a multiple of four of the signal's frequency and the continuous sampled values are averaged to produce four points in every period of the signal. Thus, calculations are mainly additions and subtractions, which result in an easier implementation of the algorithm. The algorithm can also be used to detect signals with even harmonic interferences. But when it comes to detecting the signal with odd harmonics, the odd harmonics will distort the result. Leis *et al.*[16] also proposed a fast algorithm which reduced the number of arithmetic operations to four points' addition or subtraction in every period. But the sampling rate is very low as the DLIA only samples 4 points in every period. It is suggested that higher sampling rate will result in higher accuracy.[17] Actually the procedure of averaging and calculating four points is similar to that of digital lock-in amplifier using square wave reference. Computations in square wave reference PSD are mainly additions and subtractions.[18] During the positive cycle of the reference signal, the sampled values are added together, while during the negative cycle of the reference signal, the sampled data are added together and then subtracted from the previous result. The simplicity of the algorithm makes it possible to realize the demodulation process in a low-cost microprocessor. However, since the square wave contains a large amount of odd harmonics of the fundamental frequency,[19] interferences at the harmonics of the reference signal cannot be removed with conventional square wave DLIA.

This paper presents a simple approach detecting the amplitude and phase of a signal with odd harmonics using the square wave DLIA, which removes the odd harmonic

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interferences and takes advantage of the simplicity of the square wave DLIA. We assumed a two-frequency signal in which the higher frequency component is regarded as the odd harmonic interference. The algorithm was represented through the demodulation process of the two-frequency signal. The algorithm removes the odd harmonic interference and simultaneously detects the phase and amplitude of the interference. Computations in the algorithm are mainly additions and subtractions, which makes the algorithm fast and easy to be implemented, especially in general purpose microprocessors. We validated the feasibility of the algorithm by applying it to both simulated and experimental data.

II. BASIC THEORY OF DIGITAL LOCK-IN DETECTION

Supposing the detected signal is a sinusoidal waveform with a direct current (DC) offset shown as Eq. (1),

$$x(t) = \mathrm{DC} + V\sin(2\pi f t + \theta). \tag{1}$$

Where A, f, and θ are amplitude, frequency, and initial phase angle, respectively, and the term DC is the direct current voltage offset. In a digital lock-in detection system, an ADC samples the signal at a certain sampling frequency and feeds the sampling values into a microprocessor. Assuming that the ADC samples M periods and $4N$ points in every period, the number of total sampling points is $4MN$ and the sampling values are described in Eq. (2),

$$x(n) = \mathrm{DC} + V\sin(2\pi n/(4N) + \theta),$$
$$n = 0, 1, 2.....4MN - 1. \tag{2}$$

The reference signal sequence could be either a sine wave or a square wave, which is generated by the microprocessor synchronously and has the same frequency of the detected signal. Here, we discuss the situation where a square wave with unit amplitude is used as the reference signal. The Fourier expansion of the in-phase and quadrature-phase reference signals are described in Eqs. (3) and (4),

$$S(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}\sin[2\pi \times (2k+1)n/(4N)],$$
$$n = 0, 1, 2.....4MN - 1, \tag{3}$$

$$C(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{(-1)^k}{2k+1}\cos[2\pi \times (2k+1)n/(4N)],$$
$$n = 0, 1, 2\ldots 4MN - 1. \tag{4}$$

In order to get the phase and the amplitude of the detected signal, calculations in Eq. (5) are implemented in a microprocessor

$$I = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times S(n),$$
$$Q = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times C(n). \tag{5}$$

The multiplications in Eq. (5) produce a large amount of harmonics, and the averaging operations can filter the higher frequency components. Then the results of in-phase and quadrature-phase output are described in Eq. (6),

$$I \approx \frac{2V}{\pi}\cos(\theta) \quad Q \approx \frac{2V}{\pi}\sin(\theta). \tag{6}$$

And the amplitude V and phase θ can be found in Eq. (7),

$$V = \frac{\pi}{2}\sqrt{I^2 + Q^2}, \quad \theta = \arctan\left(\frac{Q}{I}\right). \tag{7}$$

III. ALGORITHM FOR TWO-FREQUENCY SIGNALS

A. The design for single frequency signal

Before introducing the algorithm for two-frequency signals, the procedure of detecting a single frequency signal using square wave DLIA is described. In order to make the quadrature multiplication possible, the sampling frequency (f_s) must be chosen to be a multiple of four times the detected signal,[19] i.e., the ADC samples $4N$ ($N = 1, 2, 3\ldots$) points in a single period of the signal. The in-phase and quadrature-phase reference signal of the same frequency as the signal in a single period are shown in Eqs. (8) and (9),

$$S(n) = \begin{cases} 1 & 0 \le n \le 2N-1 \\ -1 & 2N \le n \le 4N-1 \end{cases}, \tag{8}$$

$$C(n) = \begin{cases} 1 & 0 \le n \le N-1, 3N \le n \le 4N-1 \\ -1 & N \le n \le 3N-1 \end{cases}. \tag{9}$$

Supposing that we sample only one period of the signal $x(n)$, the computations of the in-phase and quadrature-phase signal are shown in Eqs. (11) and (12),

$$I = \frac{1}{4N}\sum_{n=0}^{4N-1} x(n) \times S(n)$$
$$= \frac{1}{4N}\left[\sum_{0}^{N-1} x(n) + \sum_{N}^{2N-1} x(n) - \sum_{2N}^{3N-1} x(n) - \sum_{3N}^{4N-1} x(n)\right], \tag{10}$$

$$Q = \frac{1}{4N}\sum_{n=0}^{4N-1} x(n) \times C(n)$$
$$= \frac{1}{4N}\left[\sum_{0}^{N-1} x(n) - \sum_{N}^{2N-1} x(n) - \sum_{2N}^{3N-1} x(n) + \sum_{3N}^{4N-1} x(n)\right]. \tag{11}$$

There are four accumulation terms in each equation, and the accumulations of the two equations are equal at the same position except for signs ahead of the terms. Replacing each accumulated result with variables A, B, C, and D in Eqs. (10) and (11), then we will get the in-phase and quadrature-phase

output according to Eqs. (12) and (13),

$$I = \frac{1}{4N}(A + B - C - D), \tag{12}$$

$$Q = \frac{1}{4N}(A - B - C + D). \tag{13}$$

Actually, we accumulate the samples in the half period of the reference signal and then subtract the samples during the other half period. The accumulation and averaging operations can be considered as a down-sampling process reducing the sampling rate to twice of the reference frequency and the down-sampled values are multiplied with sine and cosine waves whose initial phases are both $\pi/2$. The down-sampling process is equivalent to an averaging filter. The frequency response[11] of the averaging filter is given by Eq. (14),

$$H(f) = \frac{\sin(\frac{N_s \pi f}{f_s})}{N_s \sin(\frac{\pi f}{f_s})} e^{-j\frac{\pi(N_s-1)f}{f_s}}. \tag{14}$$

Where f is the signal frequency and f_s is the sampling frequency. N_s is the number of the averaging points. Here f_s is $4N$ times of f and N_s is twice of N. From Eq. (14), we observe that the averaging filter causes a phase shifting in the down-sampling process. Because of the initial phase of the reference signal and the phase shifting caused by the averaging filter, the calculated phase in Eq. (7) should be added by $\Delta\theta$, which is given in Eq. (15),

$$\Delta\theta = \frac{\pi}{2} - \frac{\pi(N_s - 1)f}{f_s} = \frac{\pi f}{f_s}. \tag{15}$$

The initial phase is described in Eq. (16),

$$\theta = \arctan\left(\frac{Q}{I}\right) + \Delta\theta. \tag{16}$$

The procedure of demodulating a single frequency signal is shown in Fig. 1, which is implemented in a microprocessor with an internal ADC or an external ADC. The ADC's sampling rate is configured as $4N$ times of the frequency of the input signal. This yields $4N$ points in each period of the signal, which means there are N points in each quarter period. Samples of the signal in every period are dispatched to the four accumulators by a multiplexed switch. The multiplexed switch is simply realized using statement "switch...case" in a C program and accumulations are carried out in each "case" branch. The switch will shift to the next branch after it gets N points and goes back to the first accumulator at the end of every period. This means that the multiplexed switch connects the four accumulators, respectively, in the first quarter, second quarter, third quarter, and fourth quarter of each period and each accumulator receives N samples from the ADC in each period when connected to the switch. Therefore, each accumulator collects $M*N$ samples during M periods of the signal. Then based on the four accumulated values and the two equations Eqs. (12) and (13), we can calculate the in-phase output (I) and quadrature-phase output (Q).Then the amplitude and phase of the input signal can be calculated according to Eq. (7).

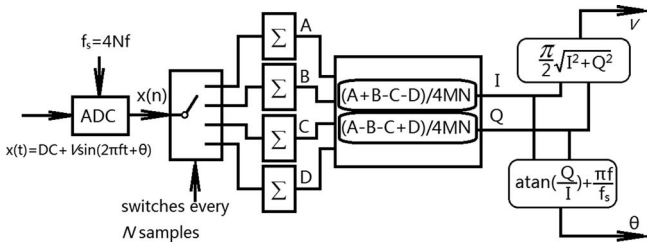

FIG. 1. Schematic diagram of digital lock-in for single frequency signal.

B. The design for two-frequency signal

In some cases, the detected signal contains odd harmonic interferences. Here, we discuss the demodulation of a two-frequency signal, in which the higher frequency component is regarded as the odd harmonic interference. The signal is described in Eq. (17),

$$x(t) = V_1 \sin(2\pi f_1 t + \theta_1) + V_p \sin(2\pi f_p t + \theta_p) \quad (f_p > f_1). \tag{17}$$

The $V_1\sin(2\pi f_1 t + \theta_1)$ term will be referred as the lower frequency component (LF) and the $V_p\sin(2\pi f_p t + \theta_p)$ term as the higher frequency component (HF) in the following part of this paper. The frequency of HF is assumed to be p times of the LF ($f_p = p*f_1$), and the signal $x(t)$ is sampled at the sampling frequency of $f_s = N_p*f_p$ ($N_p = 4N, N = 1, 2, 3\ldots$), then the sampled values would be as follows:

$$x(n) = V_1 \sin(2\pi n/(pN_p) + \theta_1) + V_p \sin(2\pi n/N_p + \theta_p). \tag{18}$$

In order to get the amplitude and initial phase of the HF, the sampled data are multiplied by the square wave reference signals with the same frequency of the HF. The Fourier series of those reference signals are given in Eqs. (19) and (20),

$$S_p(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}\sin[2\pi \times (2k+1)n/N_p], \tag{19}$$

$$C_P(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{(-1)^k}{2k+1}\cos[2\pi \times (2k+1)n/N_p]. \tag{20}$$

If the ADC samples $4M*N$ points, the results of in-phase and the quadrature-phase signal are shown in Eqs. (21) and (22),

$$I_p = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times S_p(n) \approx \frac{2}{\pi}V_p\cos(\theta_p), \tag{21}$$

$$Q_p = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times C_p(n) \approx \frac{2}{\pi}V_p\sin(\theta_p). \tag{22}$$

The amplitude and the phase of the HF are calculated from I_p and Q_p,

$$V_p = \frac{\pi}{2}\sqrt{I_p^2 + Q_p^2}, \quad \theta_p = \arctan\left(\frac{Q_p}{I_p}\right). \tag{23}$$

However, for conventional digital lock-in algorithm using the reference square wave with the same frequency of LF, we find that the outputs of the multiplication with square wave not only depend on the amplitude and the phase of the LF, but also that of HF. The Fourier expansions of the square wave reference signals with the frequency of LF are given in Eqs. (24) and (25),

$$S_1(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}\sin[2\pi \times (2k+1)n/(pN_p)], \tag{24}$$

$$C_1(n) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{(-1)^k}{2k+1}\cos[2\pi \times (2k+1)n/(pN_p)]. \tag{25}$$

(1) Assuming that $p = 4q + 3$, where $q = 0, 1, 2, 3\ldots$, the results of the multiplication and average operations are shown in the following equations:

$$I_1' = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times S_1(n)$$

$$\approx \frac{2}{\pi}V_1\cos(\theta_1) + \frac{2}{p\pi}V_p\cos(\theta_p), \tag{26}$$

$$Q_1' = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times C_1(n)$$

$$\approx \frac{2}{\pi}V_1\sin(\theta_1) - \frac{2}{p\pi}V_p\sin(\theta_p). \tag{27}$$

The second terms in Eqs. (26) and (27) depend on the amplitude and initial phase of HF, which are $1/p$ times of the results of Eqs. (21) and (22), respectively. The interference of HF can be removed by subtracting the second term. Then the in-phase and quadrature-phase component of the LF can be calculated in Eqs. (28) and (29), respectively,

$$I_1 = I_1' - I_p/p \approx \frac{2}{\pi}V_1\cos(\theta_1), \tag{28}$$

$$Q_1 = Q_1' + Q_p/p \approx \frac{2}{\pi}V_1\sin(\theta_1). \tag{29}$$

And the calculation equations of the amplitude and phase of LF are shown in Eq. (30),

$$V_1 = \frac{\pi}{2}\sqrt{(I_1' - I_p/p)^2 + (Q_1' + Q_p/p)^2},$$

$$\theta = \arctan\left(\frac{Q_1' + Q_p/p}{I_1' - I_p/p}\right). \tag{30}$$

(2) Assuming that $p = 4q+1$, where $q = 1, 2, 3\ldots$, the results of the multiplication and average operation are shown in the following equations:

$$I_1' = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times S_1(n)$$

$$\approx \frac{2}{\pi}V_1\cos(\theta_1) + \frac{2}{p\pi}V_p\cos(\theta_p), \tag{31}$$

$$Q_1' = \frac{1}{4MN}\sum_{n=0}^{4MN-1} x(n) \times C_1(n)$$

$$\approx \frac{2}{\pi}V_1\sin(\theta_1) + \frac{2}{p\pi}V_p\sin(\theta_p). \tag{32}$$

In the similar way,

$$I_1 = I_1' - I_p/p \approx \frac{2}{\pi}V_1\cos(\theta_1), \tag{33}$$

$$Q_1 = Q_1' - Q_p/p \approx \frac{2}{\pi}V_1\sin(\theta_1). \tag{34}$$

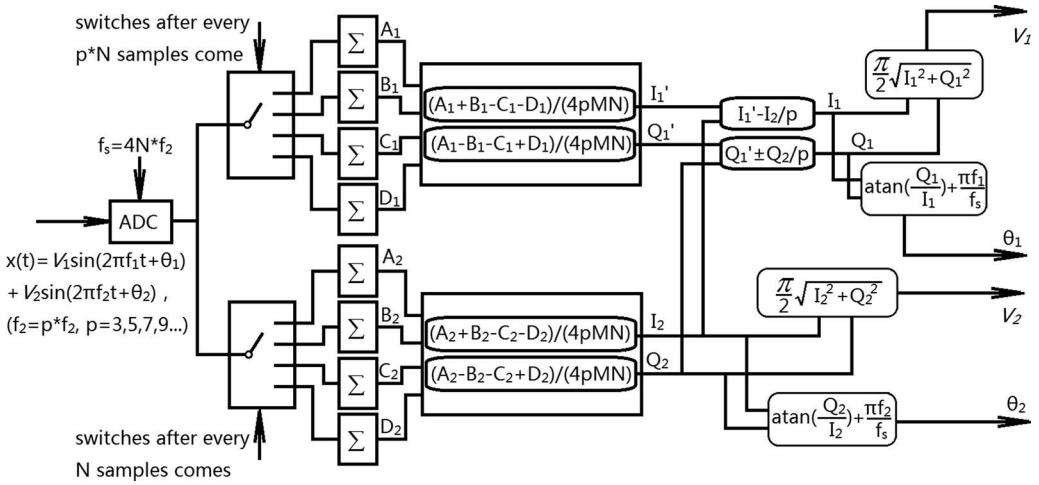

FIG. 2. Schematic diagram of digital lock-in for two-frequency signal.

The calculation equations to obtain the amplitude and phase are shown as follows:

$$V_1 = \frac{\pi}{2}\sqrt{(I_1' - I_p/p)^2 + (Q_1' - Q_p/p)^2},$$

$$\theta = \arctan\left(\frac{Q_1' - Q_p/p}{I_1' - I_p/p}\right). \quad (35)$$

According to the above calculations, we can realize the algorithm in a microprocessor with the following procedure. With only one ADC sampling the signal, the LF and HF in the signal are demodulated simultaneously. The explicit process is depicted in Fig. 2. The ADC's sampling frequency is configured as 4N times of the higher frequency. The demodulation processes of the HF and the LF are carried out in parallel, using the similar way as shown in Fig. 1. The difference is the phase-sensitive detection of LF. According to Eqs. (28), (29) or (33), (34) the I_1 and Q_1 of the LF are calculated by subtracting $1/p$ times of the I_p and Q_p of the HF, removing the interference of the HF.

The demodulation of the signal with more odd harmonics can be performed in a similar way as presented above. The higher frequency components can be detected first and then removed through the subtraction computations.

IV. EXPERIMENTS AND RESULTS

A. Simulation experiment

In order to validate the proposed algorithm obtaining the amplitude and phase of the LF and HF for a two-frequency signal, a series of simulations were carried out. The simulations were implemented in MATLAB on a PC. A signal with 1 kHz LF and 3 kHz HF was generated as shown in Eq. (36),

$$x(t) = V_1 \sin(2\pi * 1000t + \theta_1) + V_3 \sin(2\pi * 3000t + \theta_3). \quad (36)$$

The signal was sampled at a sampling rate of 120 ksps by a 12-bit ADC with a reference voltage of 4.096 V. First, we tested the proposed algorithm using the signal with a fixed initial phase of zero and variable amplitudes. The results are shown in Table I. Second, we set the amplitudes of both components to 1V and tested the signal with different initial phases. The results are shown in Table II. The results in Table I show that the calculated voltages are almost equals to the actual voltages and the results in Table II show the calculated phases by the new algorithm agree with the actual ones. The simulation experiments suggest the correctness of the algorithm.

TABLE I. The test result of different amplitudes of HF and LF by 12-bit ADC in a simulation experiment.

The actual amplitudes/V		The calculated amplitudes/V	
V_1	V_3	V_1	V_3
1.0000	1.0000	0.9995	1.0001
0.1000	1.0000	0.0995	1.0012
0.0100	1.0000	0.0102	1.0013
1.0000	0.1000	1.0006	0.0998
1.0000	0.0100	1.0001	0.0102

TABLE II. The test result of different initial phase of HF and LF by 12-bit ADC in a simulation experiment.

The actual phases/rad		The calculated phases/rad	
θ_1	θ_3	θ_1	θ_3
0.0000	0.0000	0.0003	0.0002
0.7854	0.0000	0.7853	0.0000
1.5708	0.0000	1.5714	0.0003
0.0000	0.7854	0.0000	0.7858
0.0000	1.5708	0.0004	1.5713

B. Actual experiment

In order to validate the proposed algorithm with experimental data, a data acquisition system based on a microcontroller CY8C3866AXI-040 was constructed. The microcontroller has a single cycle 8051 CPU core and several kinds of analog components.[20] As shown in Fig. 3, two 8-bit current digital-to-analog converters (DAC), an analog-to-digital converter, and a transimpedance amplifier (TIA) in the microcontroller were used. The two current DACs produced sinusoidal signals with amplitude of 2 mA and the frequencies of 1 kHz and 3 kHz respectively. The light emitting diode (LED) with wavelength of 940 nm was driven by the 1 kHz current and the LED with wavelength of 660 nm was driven by the 3 kHz current. The optical signal was measured by the photodiode and then amplified by a TIA in the microcontroller. The output of the TIA was sampled at a sampling rate of 240 ksps using the 9-bit ADC with the reference voltage of 1.024 V. The proposed algorithm was implemented by the microcontroller and then the resulting amplitudes were displayed on the Liquid Crystal Display (LCD). In order to make a comparison, the output of the TIA was also measured using a commercial DLIA 7280 DSP Lock-in Amplifier[21] made by SINGAL RECONVERY. We also implemented the conventional square

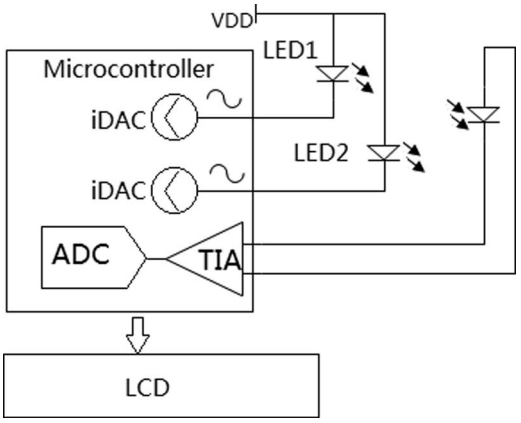

FIG. 3. Block diagram of the data acquisition system.

TABLE III. The experimental result of step (b).

7280 DSP LIA		My system (new algorithm)		Conventional algorithm
1 kHz (V)	3 kHz (V)	1 kHz (V)	3 kHz (V)	1 kHz (V)
0.4023	0.0058	0.4033	0.0054	0.4015
0.1009	0.0012	0.1007	0.0009	0.1003
0.0521	0.0000	0.0520	0.0000	0.0519
0.0108	0.0000	0.0103	0.0000	0.0103
0.0049	0.0000	0.0047	0.0000	0.0047

wave DLIA algorithm to detect the 1 kHz signal using the same data acquisition system.

The experiment was carried out following these steps:

(a) Set the integral time of the 7280 DSP LIA and the data acquisition system to be 1*s*.
(b) With the 940 nm LED turned on and the 660 nm LED turned off, we measured the output of the TIA by the 7280 DSP LIA and the data acquisition system while gradually adjusting the distance between the LEDs and the photodiode to change the output current of the photodiode.
(c) With the 940 nm LED turned off and the 660 nm LED turned on, we measured the output of the TIA using 7280 DSP LIA and the system while changing the distance between the LEDs and the photodiode.
(d) With both LEDs on, we adjusted the distance between the LEDs and the photodiode and measured the output of the TIA using 7280 DSP LIA and the data acquisition system.

The results of steps (b)–(d) are shown in Tables III–V, respectively. In Table III, the 1 kHz component can be detected by the proposed algorithm and the results are in accordance with those from the 7280 DSP LIA. It is not evident that the 3 kHz component distorts the results from the conventional algorithm because the amplitude of the 3 kHz component was very small. In Table IV, it is clear that the 3 kHz component can be detected by the proposed algorithm and the 3 kHz component distorted the results in the conventional algorithm. In Table V, it is evident that the 1 kHz and 3 kHz component can be detected by the proposed algorithm and the 3 kHz harmonic distorted the results in the conventional square wave algorithm. Above all, it is clear that the proposed algorithm can detect the signal of interest frequency and one of its odd harmonics.

TABLE IV. The experimental result of step (c).

7280 DSP LIA		My system (new algorithm)		Conventional algorithm
1 kHz (V)	3 kHz (V)	1 kHz (V)	3 kHz (V)	1 kHz (V)
0.0001	0.4080	0.0001	0.4092	0.1364
0.0001	0.0983	0.0002	0.0983	0.0328
0.0001	0.0505	0.0004	0.0504	0.0170
0.0002	0.0216	0.0002	0.0216	0.0073
0.0002	0.0097	0.0002	0.0095	0.0031

TABLE V. The experimental result of step (d).

7280 DSP LIA		My system (new algorithm)		Conventional algorithm
1 kHz (V)	3 kHz (V)	1 kHz (V)	3 kHz (V)	1 kHz(V)
0.3988	0.3604	0.4002	0.3615	0.2950
0.1039	0.0667	0.1040	0.0668	0.0843
0.0508	0.0181	0.0505	0.0180	0.0452
0.0109	0.0017	0.0103	0.0013	0.0100

V. CONCLUSION

This paper presents a new digital lock-in algorithm with square wave reference that can remove the odd harmonic interferences. We use the two-frequency signal with one odd harmonics to illustrate the designed algorithm. The algorithm is implemented to detect the two frequency components in parallel using DLIAs with as two square wave references, one for the demodulation of the HF and the other for the LF. There is a small modification in the demodulation process of LF compared with the conventional algorithm. The subtraction related to the two orthogonal PSD outputs of HF are computed in the demodulation of LF, consequently the interference of HF is removed. The simulated and experimental results suggest the correctness of the algorithm. The conventional square wave DLIAs can be only applied to detect the signal with even harmonics, thus the proposed design can be a supplementation of digital lock-in algorithm using square wave reference. Since it retains the simplicity of the conventional square wave DLIA, the algorithm can be implemented in low cost microprocessors.

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