Research article

Square wave reference digital lock-in detection using non-orthogonal demodulation

Miao Li, Yue Sun, Zhen Liang [**], Shengzhao Zhang [*]

School of Biomedical Engineering, Anhui Medical University, Hefei, 230032, China

A B S T R A C T

Digital lock-in detection technique is commonly used to measure the amplitude and phase of a selected frequency signal. The technique which uses a square wave as the reference signal has an advantage of easier implementation and higher computational efficiency compared to that uses a sine wave. However, one constraint for a square wave reference digital lock-in is that the sampling rate must be the integral multiple of 4 of all the signal frequencies. As the sampling clock may not always be able to set to the integral multiple of 4 of the signal frequencies, the constraint brings inconvenient for the implementation. Presented in this paper is a novel algorithm for square wave digital lock-in detection in which the sampling frequency doesn't have to meet the constraint. The algorithm allows frequency sweep measurements with a fixed sampling rate. For different relationships between the sampling rate and the signal frequency, different calculation equations are provided in this paper. Simulations and actual experiments show the feasibility of the proposed algorithm.

1. Introduction

Digital lock-in detection technique has been widely used in a variety of fields to measure weak signals [1-4]. It can measure a signal of interest frequency without being disturbed by noise of other frequencies. Chen et al. [4] proposed a method based on integral average digital lock-in amplifier (IADLIA) to reduce the distortion and output fluctuation of detection results of digital lock-in amplifier (DLIA). Cultrera et al. [5] proposed a setup to get calibration of lock-in amplifiers, discussed the calibration of lock-in amplifier in low frequency range. Alves et al. [6] proposed a method to obtain an enhanced frequency resolution two-phase lock-in amplifier with two channels in a microcontroller using minimum external circuitry, which can increase the frequency resolution by 1000 times. In the algorithm of digital lock-in detection, the detected signal is sampled and then multiplied respectively by a pair of mutually orthogonal reference signals, which is also called "mixing" [7]. The frequency of the reference signal should equal the interest frequency component in the detected signal. The product of the multiplication is subsequently filtered by a low pass filter. The output of the filter depends on the initial phase and the amplitude of the signal, and thus the amplitude and the phase can be extracted. One typical use of digital lock-in technique is to modulate several measured signals to different appropriate frequencies [8], and then detect the known frequency signals simultaneously, which may often be used in the optical spectrum measurement [9,10]. In a digital lock-in detection system, sinusoidal signal and square wave signal are generally used. In the system using the sinusoidal wave, multiplications between

the reference signal and the detected signal in a microprocessor will cost much computation time [11]. In a real-time application, a microprocessor with high performance may be needed. However, it will increase the cost of the whole system. Moreover in portable device using battery power supply, more computation time will cause shorter battery life. While in square wave reference digital lock-ins, as the reference signal only contains 1 and -1, the multiplication between the reference signal and the detected signal can be replaced by additions and subtractions. The additions and subtractions would cost less computation time than multiplications for a low-cost microprocessor.

Typically, in square wave digital lock-ins, the sampling rate should be 4 N (N = 1, 2, 3 …) times of the detected signal. In frequency sweep measurements [8], it is needed to measure a list signals at frequencies of $f_0, f_1, f_2, …, f_n$. The sampling rate of an analog-to-digital converter (ADC) may be set to $4N_0f_0, 4N_0f_1, 4N_2f_2, …, 4N_nf_n$ if we use square wave reference digital lock-ins. However, sampling clock of an ADC is determined by the clock source used in the system and may not be set to arbitrary frequency. The constraint that the sampling rate should be integral multiple of 4 of signal frequency narrows the application of the square wave reference digital lock-in detection technique.

In this paper, we proposed a new digital lock-in algorithm from digital lock-in algorithm using square wave reference. In the proposed algorithm, we developed new reference signal from a square wave reference. The new algorithm doesn't have to satisfy the constraint that sampling frequency should be 4 N times of the detected signal. Moreover, the new reference signal also only contains 1 and -1, the multiplications in the "mixing" is still not needed, which means the algorithm can still reduce much computation time. We validated the feasibility of the algorithm by applying it to experimental data.

2. Basic principle of conventional digital lock-in detection using square wave reference

For a signal with single frequency, let's suppose the detected signal is $x(t)$, which is shown as Eq (1). In Eq (1), the DC, A, f and φ are the direct current voltage offset, amplitude, frequency and initial phase angle, respectively. The term $noise(t)$ represents the noise.

$$x(t) = DC + A\sin(2\pi ft + \varphi) + noise(t) \tag{1}$$

In digital lock-in, the signal is being sampled and digitalized at sampling rate of f_s ($f_s > 2f$). Reference signal is needed in a digital lock-in system whose frequency is identical to that of the signal. Generally, we use two orthogonal signals in the detection, which means that one reference signal lag 1/4 period the other reference signal. In order to ensure that the generation of the orthogonal reference signals possible, the sampling rate is typically set to be 4 N (N = 1,2,3 …) times of the signal frequency.

$$f_s = 4Nf \tag{2}$$

The signal $x(t)$ is sampled and digitalized by ADC at sampling frequency of f_s, which is shown in Eq (2). The sampled signal sequences are described in Eq (3).

$$x(n) = DC + A\sin(2\pi n / 4N + \varphi) + noise(n) \tag{3}$$

The two reference signal sequences $s(n)$ and $c(n)$ of the first period are given in Eqs (4,5). The period of the reference signals is 4 N.

$$s(n) = \begin{cases} 1 & 0 \le n < 2N - 1 \\ -1 & 2N \le n < 4N - 1 \end{cases} \tag{4}$$

$$c(n) = \begin{cases} 1 & 0 \le n < N - 1, 3N \le n < 4N - 1 \\ -1 & N \le n < 3N - 1 \end{cases} \tag{5}$$

Supposing that M periods of the signal is sampled, the computation progress is given in Eqs (6,7).

$$I = \frac{1}{4MN} \sum_{n=0}^{4MN-1} x(n)s(n) \tag{6}$$

$$Q = \frac{1}{4MN} \sum_{n=0}^{4MN-1} x(n)c(n) \tag{7}$$

In fact, because the $s(n)$ and $c(n)$ only contains 1 and -1, the multiplication and accumulation progress will become additions and subtractions [12]. The results of the multiplications and the averaging operations are given in Eqs (8,9).

$$I(n) = \frac{2A}{\pi}\cos(\varphi - \pi / 4N) * h \tag{8}$$

$$Q(n) = \frac{2A}{\pi}\sin(\varphi - \pi / 4N) * h \tag{9}$$

where h is a constant with respect to the factor N shown in Eq (10). When the factor N is large enough, h is approximately to be 1.

$$h = \frac{\pi}{4N\sin(\pi/4N)} \tag{10}$$

The amplitude and the initial phase can be obtained by the Eqs (11,12).

$$A = \frac{\pi}{2} \sqrt{I^2 + Q^2} * \frac{1}{h} \tag{11}$$

$$\varphi = arctan \frac{Q}{I} + \frac{\pi}{4N} \tag{12}$$

3. New digital-lock-in algorithm

In the principle given in section II, the sampling frequency is should be set to 4 *N* times of the signal frequency in order to make orthogonal mixing possible. But how about developing new algorithm in which the constraint of "4 N times" is not needed? We take a single frequency signal to illustrate this problem.

Suppose that the sampling rate is f_s, and the signal frequency is *f*. The relationship between them is described in Eq (13).

$$\frac{f_s}{f} = 4 * \frac{N}{\alpha} \tag{13}$$

The constraints are that both *N* and α are natural numbers and $f_s > 2f$. The fraction N/α in the expression are in the simplest form. That is to say, the greatest common divisor (GCD) of *N* and α is 1. Let $f_0 = f/\alpha$, then the signal is described by Eq (14).

$$x(t) = DC + A\,sin(2\pi f t + \varphi) + noise(t) = DC + A\,sin(2\pi \alpha f_0 t + \varphi) + noise(t) \tag{14}$$

And the sampled signal value is expressed in Eq (15). at the sampling rate of f_s.

$$x(n) = DC + A\sin(2\pi \alpha n / 4N + \varphi) + noise(n) \tag{15}$$

In order to detect the signal, we generate to reference signal from the original reference signal shown in Eqs (4,5). The new reference signal $s_\alpha(n)$ and $c_\alpha(n)$ are shown in Eqs (16) and (17). The expression $((\alpha n))_{4N}$ means the remainder of αn divided by 4 N.

$$s_\alpha(n) = s(\alpha n) = \begin{cases} 1 & 0 \le ((\alpha n))_{4N} < 2N - 1 \\ -1 & 2N \le ((\alpha n))_{4N} < 4N - 1 \end{cases} \tag{16}$$

$$c_\alpha(n) = c(\alpha n) = \begin{cases} 1 & 0 \le ((\alpha n))_{4N} < N - 1, 3N \le ((\alpha n))_{4N} < 4N - 1 \\ -1 & N \le ((\alpha n))_{4N} < 3N - 1 \end{cases} \tag{17}$$

The demodulation progress is described in Eqs. (18) and (19).

$$I_\alpha = \frac{1}{4MN} \sum_{n=0}^{4MN-1} x(n)s_\alpha(n) \tag{18}$$

$$Q_\alpha = \frac{1}{4MN} \sum_{n=0}^{4MN-1} x(n)c_\alpha(n) \tag{19}$$

Though Eqs. (18) and (19) are similar to Eqs. (6,7), but the results are not the same. It is not easy to give the result of Eqs. (18) and (19) by the calculations in time domain. In order to discuss the output of the mixing and averaging progress, we analyze the signal I_α and Q_α in frequency domain. We use $r_{xs}(n)$ and $r_{xc}(n)$ to express the mixing signal in Eqs. (18) and (19), as are shown in Eqs. (20) and (21).

$$r_{xs}(n) = x(n)s_\alpha(n) \tag{20}$$

$$r_{xc}(n) = x(n)c_\alpha(n) \tag{21}$$

The averaging in Eqs (18) and (19) is actually the low pass filter [13]. The signal I_α and Q_α would be the approximately the zero-frequency component of the signal $r_{xs}(n)$ and $r_{xc}(n)$. It is easier to find the direct current component of $r_{xs}(n)$ and $r_{xc}(n)$ by computing the discreet fourier transform (DFT) of the signal x(n) and the reference signals, and then calculate the convolution of them. We apply the DFT to signal b_{xs} and r_{xc} with length of *4 N*. In Eqs. (22) and (23), $R_{xs}(k)$ and $R_{xc}(k)$ represent the DFT of r_{xs} and r_{xc}, respectively. And X(k), $S_\alpha(k)$ and $C_\alpha(k)$ are the DFT of the measured signal and reference signals.

$$R_{xs}(k) = DFT[x(n)S_\alpha(n)] = \frac{1}{4N} \sum_{l=0}^{4N-1} X(l)S_\alpha((k-l))_{4N} \tag{22}$$

$$R_{xc}(k) = DFT[x(n)C_\alpha(n)] = \frac{1}{4N} \sum_{l=0}^{4N-1} X(l)C_\alpha((k-l))_{4N} \tag{23}$$

$$X(k) \approx 2N \cdot A \left[e^{j\left(\varphi - \frac{\xi}{2}\right)} \delta(k-\alpha) + e^{-j\left(\varphi - \frac{\xi}{2}\right)} \delta(k+\alpha-4N) \right] + 4NDC\delta(k) + NOISE[k] \tag{24}$$

It is obvious that X(k) have zero values only when $k = 0$, $k = \alpha$ and $k = 4N$-α from Eq. (24), the *NOISE*(k) in Eq. (24) is DFT of the noise. Since the component of *NOISE*[k] with the same frequency as the useful signal is small and negligible, the value of $R_{xs}(0)$ and $R_{xc}(0)$ can be described in Eqs. (25) and (26).

$$R_{xs}(0) = \frac{1}{4N} \left[X(\alpha)S_\alpha(4N-\alpha) + X(4N-\alpha)S_\alpha(\alpha) + X(0)S_\alpha(0) \right] \tag{25}$$

$$R_{xc}(0) = \frac{1}{4N} \left[X(\alpha)C_\alpha(4N-\alpha) + X(4N-\alpha)C_\alpha(\alpha) + X(0)C_\alpha(0) \right] \tag{26}$$

The DFT of the new reference signal can be rewritten in the following form of Eqs. (27) and (28).

$$S_\alpha(k) = DFT[s(\alpha n)] = \frac{1}{4N} \sum_{l=0}^{4N-1} \left[S(l) \sum_{n=0}^{4N-1} W_{4N}^{(k-lq)n} \right] \tag{27}$$

$$C_\alpha(k) = DFT[c(\alpha n)] = \frac{1}{4N} \sum_{l=0}^{4N-1} \left[C(l) \sum_{n=0}^{4N-1} W_{4N}^{(k-lq)n} \right] \tag{28}$$

The result of the accumulation in the bracket in Eq. (28) can be expressed in Eq. (29).

$$\sum_{n=0}^{4N-1} W_{4N}^{(k-lq)n} = \begin{cases} 4N & l = (k+4Nm)/\alpha, m = 0, \pm1, \pm2, \pm3, \ldots \\ 0 & other \end{cases} \tag{29}$$

If the number 4 N and α are relatively prime, we have a more clear expression of $S_\alpha(0)$, $S_\alpha(\alpha)$, $S_\alpha(4N$-$\alpha)$, $C_\alpha(0)$, $C_\alpha(\alpha)$, $C_\alpha(4N$-$\alpha)$. So we discuss this question depends on whether the 4 N and α are relatively prime or not. If 4 N and α are relatively prime, the GCD of them is 1, we expressed it as GCD(4 N, α) = 1.

3.1. GCD(4 N, α) = 1

The expression of $S_\alpha(0)$, $S_\alpha(\alpha)$, $S_\alpha(4N$-$\alpha)$, $C_\alpha(0)$, $C_\alpha(\alpha)$, $C_\alpha(4N$-$\alpha)$ can rewritten in Eq. (30)~Eq. (35).

$$S_\alpha(0) = S(0) = 0 \tag{30}$$

$$S_\alpha(\alpha) = S(1) \tag{31}$$

$$S_\alpha(4N-\alpha) = S(4N-1) \tag{32}$$

$$C_\alpha(0) = C(0) = 0 \tag{33}$$

$$C_\alpha(\alpha) = C(1) \tag{34}$$

$$C_\alpha(4N-\alpha) = C(4N-1) \tag{35}$$

We joint Eq. (25)~(26) and Eq. (30)~(35) together, and then $R_{xs}(0)$ and $R_{xc}(0)$ can rewritten in the form of Eqs. (36) and (37).

$$R_{xs}(0) = \frac{2A\,cos(\varphi - \pi/4N)}{sin(\pi/4N)} \tag{36}$$

$$R_{xc}(0) = \frac{2A\,sin(\varphi - \pi/4N)}{sin(\pi/4N)} \tag{37}$$

The signal I_α and Q_α is the zero frequency of signal $r_{xs}(n)$ and $r_{xc}(n)$, respectively. The signal I_α and $Q_\alpha(n)$ are given in Eqs. (38) and (39). The term h is a constant number depends on the number 4 N which is the proportion of sampling rate and the signal frequency, as is shown in Eq. (40).

$$I_\alpha(n) = \frac{2A}{\pi} cos(\varphi - \pi/4N) * h \tag{38}$$

$$Q_\alpha(n) = \frac{2A}{\pi} sin(\varphi - \pi/4N) * h \tag{39}$$

$$h = \frac{\pi}{4N\,sin(\pi/4N)} \tag{40}$$

We obtain the amplitude and the initial phase from Eqs. (41) and (42).

$$A = \frac{\pi}{2}\sqrt{I^2 + Q^2} * \frac{1}{h} \tag{41}$$

$$\varphi = arctan\frac{Q}{I} + \frac{\pi}{4N} \tag{42}$$

3.2. GCD(4 N, α)>1

In this situation, we can't give an explicit expression of $S_\alpha(\alpha)$ and $C_\alpha(\alpha)$. If 4 N and α are not relatively prime, we simplify the fraction of 4 N/α to the simplest form to N_1/α_1. The numerator of the fraction after reduction may either be an odd number or an even number.

(1) N_1 is an even number

If N_1 is an even number, the period of $s_\alpha(n)$ and $c_\alpha(n)$ is still an even number. The signal $s_\alpha(n)$ and $c_\alpha(n)$ are zero-mean signals. So $S_\alpha(0)$ and $C_\alpha(0)$ equal zero. We rewrite the $S_\alpha(\alpha)$, $S_\alpha(4N\text{-}\alpha)$, $C_\alpha(\alpha)$ and $C_\alpha(4N\text{-}\alpha)$ in the following expressions. The parameters β, θ_0 and θ_1 depend on the frequency characteristics of the reference signal $s_\alpha(n)$ and $c_\alpha(n)$. The DFT of reference signals $s_\alpha(n)$ and $c_\alpha(n)$ of 4 N points can be calculated with the help of Computer mathematic software, and parameters β, θ_0 and θ_1 in Eq. (43)~(46) can be obtained in the software. Those works can be done before we want to realize the algorithm.

$$S_\alpha(\alpha) = \beta e^{j\theta_0} \tag{43}$$

$$S_\alpha(4N - \alpha) = \beta e^{-j\theta_0} \tag{44}$$

$$C_\alpha(\alpha) = \beta e^{j\theta_1} \tag{45}$$

$$C_\alpha(4N - \alpha) = \beta e^{j\theta_1} \tag{46}$$

Then the value of $R_{xs}(0)$ and $R_{xc}(0)$ are given in Eqs. (47) and (48).

$$R_{xs}(0) = A\beta \, sin(\varphi - \theta_0) \tag{47}$$

$$R_{xc}(0) = A\beta \, sin(\varphi - \theta_0) \tag{48}$$

And the signal I_α and Q_α can be found in Eqs. (49) and (50). The amplitude and the initial phase can be obtained by Eqs. (44) and (45).

$$I_\alpha = \frac{A}{4N}\beta \, sin(\varphi - \theta_0) \tag{49}$$

$$Q_\alpha = \frac{A}{4N}\beta \, sin(\varphi - \theta_1) \tag{50}$$

Let $\Delta\theta = \theta_1 - \theta_0$, the amplitude and the phase can be obtained by Eqs. (51) and (52).

$$A = \frac{4N}{\beta}\sqrt{\left(\frac{I_\alpha - Q_\alpha \, cos\Delta\theta}{sin\Delta\theta}\right)^2 + Q_\alpha^2} \tag{51}$$

$$\varphi = arctan\left(\frac{Q_\alpha \, sin\Delta\theta}{I_\alpha - Q_\alpha \, cos\Delta\theta}\right) + \theta_1 \tag{52}$$

(2) N_1 is an odd number

The reference signals are not zero-mean signal if N_1 is an odd number. According to Eqs. (25) and (26), in order to find $R_{xs}(0)$ and $R_{xc}(0)$, we need to know $S_\alpha(0)$ and $C_\alpha(0)$. Assuming that $S_\alpha(0)$ and $C_\alpha(0)$ equals $d*4 N$, which is described in Eq. (53).

$$S_\alpha(0) = C_\alpha(0) = 4N * d \tag{53}$$

In the same way as we do in part 1), we also calculate the parameters β, θ_0 and θ_1 in Eq. (43)~(46), and the parameters d in Eq. (51) with the help of computer software. The DFT $R_{xs}(0)$ and $R_{xc}(0)$ is described in Eqs. (54) and (55).

$$R_{xs}(0) = A\beta \, sin(\theta_0 - \varphi) + DC * d * 4N \tag{54}$$

$$R_{xc}(0) = A\beta \, sin(\theta_1 - \varphi) + DC * d * 4N \tag{55}$$

The *DC* in Eqs. (54) and (55) are direct current component of the detected signal, in the detection, it can be calculated by Eq. (56).

$$DC = \frac{1}{4MN} \sum_{n=0}^{4MN-1} x(n) \tag{56}$$

Thus the signal I_α and Q_α are shown in Eqs. (57) and (58):

$$I_\alpha = A\left[\frac{\beta}{4N} sin(\varphi - \theta_0) + DC * d\right] \tag{57}$$

$$Q_\alpha = A\left[\frac{\beta}{4N} sin(\varphi - \theta_1) + DC * d\right] \tag{58}$$

The amplitude and the initial phase of the signal can be obtained by Eqs. (59) and (60).

$$A = \frac{4N}{\beta} \sqrt{\left(\frac{(I_\alpha - (d \cdot DC) - (Q_\alpha - d * D)cos\Delta\theta}{sin\Delta\theta}\right)^2 + (Q_\alpha - d * DC)^2} \tag{59}$$

$$\varphi = arctan\left(\frac{(Q_\alpha - d * DC)sin\Delta\theta}{(I_\alpha - d * DC) - (Q_\alpha - d \cdot DC)cos\Delta\theta}\right) + \theta_1 \tag{60}$$

4. Designing and implementation

According to the analysis in Part III of this paper, we give some brief description of the designing and implementation Issues. Fig. 1 shows the diagram of an implementation of the new algorithm.

Before designing the algorithm, we should decide the interested signal frequency f and the sampling frequency f_s. We rewrite the fraction f_s/f into the form which is presented in Eq. (61). Make sure that GCD(N, α) and GCD(N_1,α_1) equal 1 and not to violate the Nyquist law. The sampling frequency should be carefully set that not make the number N too large, for the integral time is proportional to N. A new pair of reference signals is generated from the old pair of reference signals given in Eqs (4,5). whose period are equaled to 4 N. Before we realize the algorithm in a microprocessor of a digital lock-in detection system, some parameter should be prepared in advance. If $N = 4N_1$, the parameter h should be calculated by using Eq. (40). If $N \neq 4N_1$, the value of $S_\alpha(\alpha)$, $C_\alpha(\alpha)$ should be calculated by using Eqs. (43) and (45), while the DFT transform of reference signal should be taken with the help of computer mathematics software. The parameter β, θ_0, θ_1 and $\Delta\theta$ can be obtained as we do DFT of the reference signal.

Parameters such as h, β, θ_0, θ_1 and $\Delta\theta$ should be stored as constants in the microprocessor of the digital lock-in detection system. While detecting the signal, the computation of two signals I_α and Q_α should take place in the microprocessor. If $N = N_1$, the DC signal is also needed to be detected. Those computations are described in Eqs. (18), (19) and (56). Depending on the difference relationship between N_1 and $4 N$, and the odd-even feature of N1, different computation progresses should be done in the microprocessor by using equations given in Fig. 1.
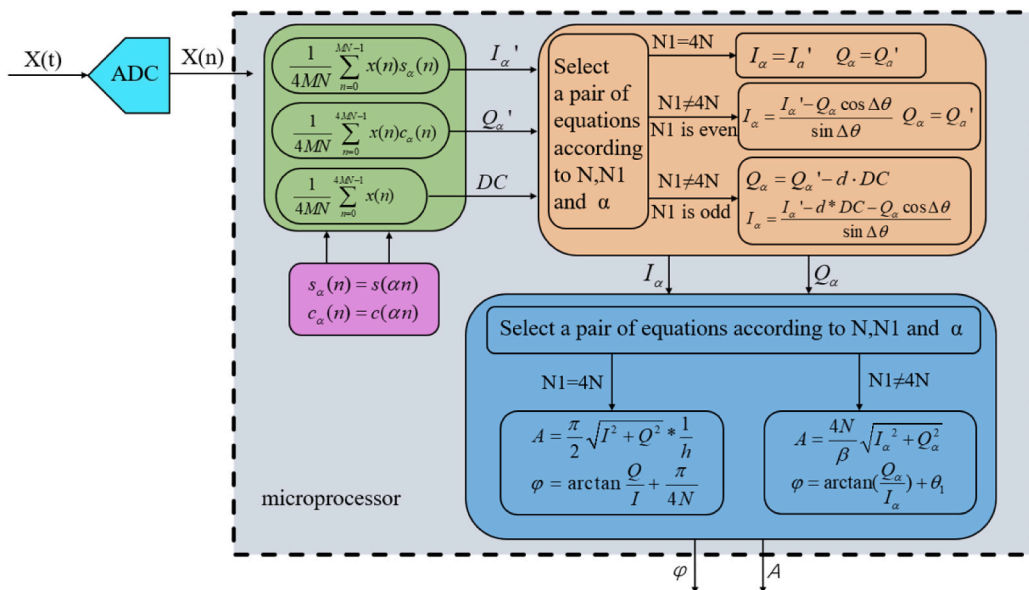

Fig. 1. Diagram of the implementation of the new algorithm.

$$\frac{f_s}{f} = 4 * \frac{N}{\alpha} = \frac{N_1}{\alpha_1} \tag{61}$$

5. Simulations and actual experiments

5.1. Simulations

The simulations were implemented in mathematics software Matlab(Version 2010. b). A signal of 1 kHz is generated as is shown in Eq. (62). The amplitude, DC offset and initial phase were set to be $1V$, $2V$ and 0.75 rad, respectively. The term *rand* is uniform distribution from 0 to 1.

$$x(t) = 1V * sin(2\pi * f * t + 0.75) + A_{noise} * rand \tag{62}$$

Integral time is set to 10 ms and the sampling rate is 200ksps. The values of f are 3 KHz,4 KHz and 8 KHz. A uniformly distributed noise with amplitude A_{noise} is added to the signal. The value of A_{noise} were set 0.01, 0.1 and 1. The results of RMSE were calculated based on 100 sets of experimental data and were shown in Tables 1–3. From the table, it can be concluded that the amplitude calculated using the proposed algorithm at different frequencies is almost equal to the real value 1V, and the phase almost equaled the real value 0.75°. The rejection ratio of the noise is about 40 dB at the integral time of 10 ms when the sampling rate is 200ksps.

5.2. Actual experiments

Impedance is a basic concept widely used in the field of electronics [14]. To test the proposed algorithm, we design a multi-frequency impedance tester based on a microcontroller CY8C5888LTI-LP097 [15]. The microcontroller has a CORTEX-M3 CPU and several types of analog components. The ADC and 8-bit current digital-to-analog converter (DAC) in the chip were utilized, as is illustrated in Fig. 2. A single current DAC cannot generate sinusoidal current waves as the wave has both positive part and negative part. Two current DACs were used, for one act as "source" to generate positive half of the signal and the other act as "sink" to generate negative half of the signal. A positive voltage bias of 1.024V is provided through the follower, for the microcontroller is unable to provide negative voltage. Integral time is set to 10 ms. The periodic voltage signal over the resistor is sampled by the in-chip ADC with a resolution of 11-bit and sampling rate of 200ksps. The microcontroller calculated the amplitude of the periodic signal using the proposed algorithm and then converts the result into the value of the resistor using the Ohm's law. We calibrated the impedance tester which used ten resistors whose values were 1kΩ, 2kΩ, …, 10 kΩ.

We connected the impedance tester to an RLC net and tested it at the frequency of 3 kHz , 4 kHz and 8 KHz, with the sampling frequency of 200KSPS, corresponding to the three cases discussed by N, α and N₁. The readings of our tester were compared with the results measured by a commercial RLC meter called GWINSTEK. The results were shown in Table 4 and Table 5. All the measured value of our tester in the table were mean value of 100 readings. As is shown in Table 2, the results of the amplitude values of the impedances measured by our tester were closed to the values measured by GWINSTEK. We further calculate the standard deviation(std) of the readings, and the maximum std did not exceed 0.1%. As is shown in Table 3, the results of the phase values of the impedances measured by our tester were closed to the values measured by GWINSTEK. We also further calculate the standard deviation(std) of the readings, and the maximum std did not exceed 1°.

To test the noise rejection ability of our system, a function generator (Rigol MSO5204) which generate random noise were couple to the system. The impedance connect to the tester is about 15 kΩ and the amplitude of the noise were set to 50 mV–500 mV. As the current source in the system was set to 32 μA , the amplitude of the sinusoidal wave is 480 mV. Integral time were set 10 ms and the frequency was set to 3 kHz. Each measurement was done for 100 times. The maximum values, the minimum values, the mean values and the standard deviations (STDs) for each level of noise were shown in Table 6. The noise level is was set from 10% of the signal amplitude to 104% of the signal amplitude. It showed that when the level of the random noise increased, the STD increased and the absolute error increased accordingly. When the noise level is about 10.04% of the signal level, the uncertainty was about 1‰ of the signal and the maximum relative error is about 4‰. When the noise level is about 104% of the signal level, the uncertainty of the measurement was about 1% and the maximum relative error is about 3.3%. The result suggested that the noise can be suppressed to 1% of its original level when the integral time was set to 10 ms using the proposed algorithm.

Table 1
Result of the simulations at frequency 3 kHz.

A_{noise}	Amplitude (Ω)		Phase (degree)	
	Mean	RMSE	Mean	RMSE
0.01	1.000E+00	9.9E-05	7.500E-01	9.7E-05
0.1	1.000E+00	9.8E-04	7.500E-01	1.1E-03
1	9.986E-01	1.0E-02	7.493E-01	9.6E-03

Table 2
Result of the simulations at frequency 4 kHz.

Anoise	Amplitude (Ω)		Phase (degree)	
	Mean	RMSE	Mean	RMSE
0.01	1.000E+00	1.0E-04	7.510E-01	9.5E-05
0.1	9.999E-01	1.0E-03	7.510E-01	1.0E-03
1	9.998E-01	1.0E-02	7.527E-01	1.1E-02

Table 3
Result of the simulations at frequency 8 kHz.

A_{noise}	Amplitude (Ω)		Phase (degree)	
	Mean	RMSE	Mean	RMSE
0.01	1.000E+00	9.9E-05	7.511E-01	1.1E-04
0.1	9.999E-01	1.0E-03	7.511E-01	1.0E-03
1	9.990E-01	1.0E-02	7.493E-01	1.1E-02
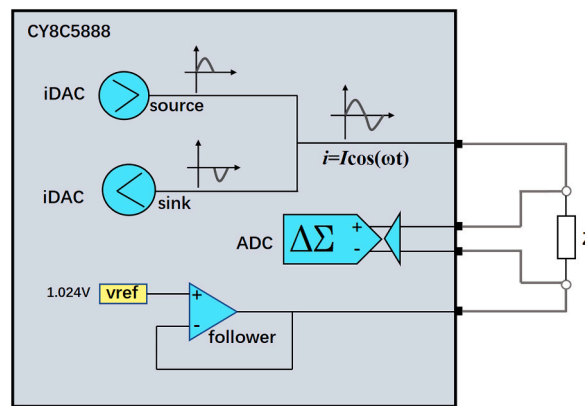
Fig. 2. Block diagram of the impedance tester.

Table 4
Impedance amplitude values of RCL net measured by our tester and GWINSTEK.

RCL net	f = 3 KHz (uint kΩ)		f = 4 KHz (uint kΩ)		f = 8 KHz (uint kΩ)	
	GWINSTEK	Our tester	GWINSTEK	Our tester	GWINSTEK	Our tester
30 mH+2kΩ	2.189	2.202	2.249	2.244	2.607	2.609
30 mH+4kΩ	4.150	4.180	4.183	4.179	4.390	4.416
30 mH+6kΩ	6.135	6.141	6.158	6.154	6.305	6.325
30 mH+8kΩ	8.127	8.130	8.145	8.136	8.256	8.286
30 mH + 10 kΩ	10.12	10.12	10.13	10.12	10.23	10.25
30 mH + 12 kΩ	12.11	12.11	12.12	12.11	12.20	12.24
30 mH + 14 kΩ	14.10	14.10	14.12	14.09	14.18	14.21
100nf+16 kΩ	16.00	15.97	16.00	15.95	16.00	15.95
100nf+18 kΩ	18.00	1.800	17.9987	17.93	17.99	17.92
100nf+20 kΩ	20.01	19.99	20.0085	19.95	20.00	19.89
100nf+22 kΩ	22.00	21.94	22.0023	21.93	22.00	21.90
100nf+24 kΩ	24.00	23.92	24.0065	23.90	24.01	23.87

6. Conclusion

Square wave reference digital lock-in detection system has a high reputation as the algorithm is much efficient and easy to implement. But the reference signal needs to be 4 integral times of the detected signal frequency. In this paper, we design a new algorithm from the traditional square wave reference digital lock-in algorithm. The new algorithm uses a pair of new reference signals which are generated from square wave signals. Depending on the relationship between the sampling frequency and the signal frequency, three different kinds of calculations are carried out by a microprocessor. Before we realize the algorithm into a microprocessor

Table 5
Impedance phase values of RCL net measured by our tester and GWINSTEK.

RCL net	f = 3 KHz (uint °)		f = 4 KHz (uint °)		f = 8 KHz (uint °)	
	GWINSTEK	Our tester	GWINSTEK	Our tester	GWINSTEK	Our tester
910Ω	0	0.7	0	0.5	0	0.6
47 nF	−89.4	−89.6	−89.4	−88.4	−89.4	−88.6
22 nF + 1000Ω	−68.7	−68.5	−62.9	−62.7	−45.1	−48.5
47 nF + 820Ω	−55.3	−54.6	−47.2	−46.5	−29	−28.38
100 nF + 680Ω	−39.2	−40.1	−31.9	−32.2	−17.9	−17.4
220 nF + 680Ω	−23.2	−22.2	−18	−16.6	−9.5	−8.7
10 mH + 470Ω	21.2	22.0	28.2	28.3	44.9	45.6
30 mH + 750Ω	32.8	33.6	40.5	41.5	59.8	60.7
30 mH + 470Ω	43.8	44.7	51.7	52.8	67.6	68.5
100 mH + 680Ω	61.9	61.1	67.8	68.8	77.7	77.4
100 mH	80.4	81.8	82.4	83.7	85.5	86.4

Table 6
The result of the measured impedance at varying noise at frequency 3 kHz.

Noise	Amplitude (Ω)			
	Mean	STD	Max	Min
50 mV	1.502E+04	1.8E+01	1.506E+04	1.495E+04
100 mV	1.495E+04	3.2E+01	1.509E+04	1.490E+04
150 mV	1.498E+04	4.8E+01	1.514E+0.4	1.485E+04
200 mV	1.500E+04	6.2E+01	1.521E+04	1.475E+04
250 mV	1.502E+04	8.0E+01	1.530E+04	1.473E+04
300 mV	1.496E+04	9.1E+01	1.530E+04	1.469E+04
350 mV	1.497E+04	1.12E+01	1.543E+04	1.466E+04
400 mV	1.495E+04	1.21E+02	1.548E+04	1.458E+04
450 mV	1.495E+04	1.43E+02	1.544E+04	1.454E+04
500 mV	1.496E+04	1.52E+02	1.550E+04	1.449E+04

based digital lock-in system, several parameters should be calculated according to the reference signals, with the help of computer software. The new algorithm doesn't need to satisfy the constraint that the sampling rate should be 4 N times of the signal frequency. We carried out simulations and actual experiments and the results show the correctness of the algorithm.

Author contribution statement

Miao Li, Yue Sun, Zhen Liang: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; wrote the paper.

Shengzhao Zhang: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data; Wrote the paper.

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Data availability statement

Data included in article/supp. material/referenced in article.

Declaration of interest's statement

The authors declare no competing interests.

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