

# D.S.P. based Field Oriented Control of Induction motor

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# Block Diagram of Field Oriented Control

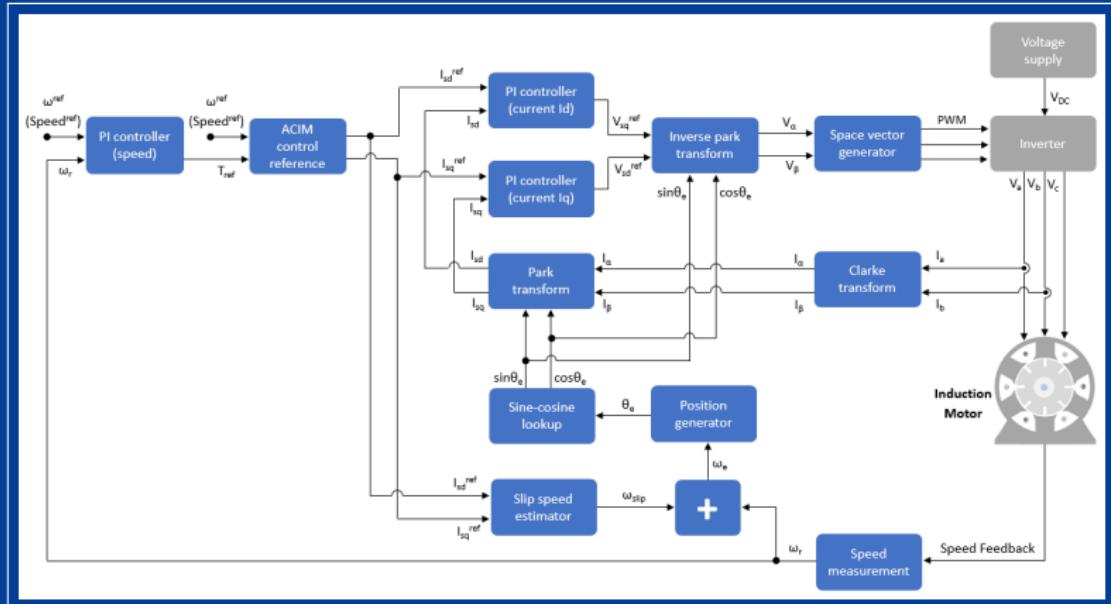


Figure: Block Diagram of Field Oriented Control

# Block Diagram of the System

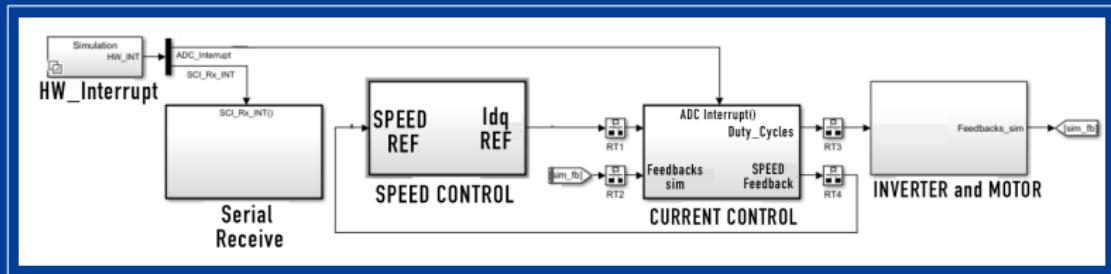


Figure: Block Diagram of the System

# Speed Control Subsystem

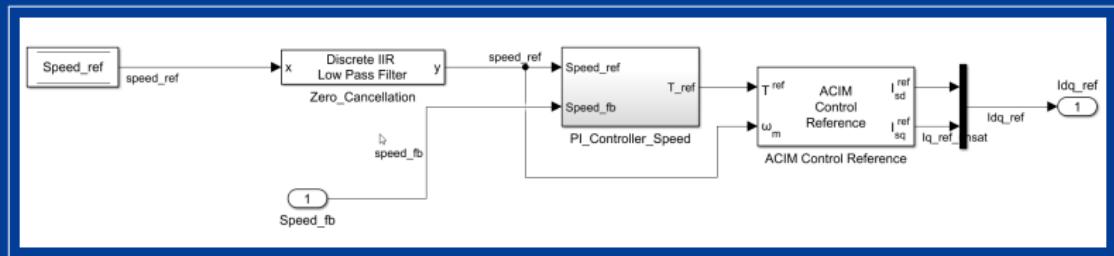


Figure: Speed Control Subsystem

# Current Measurement

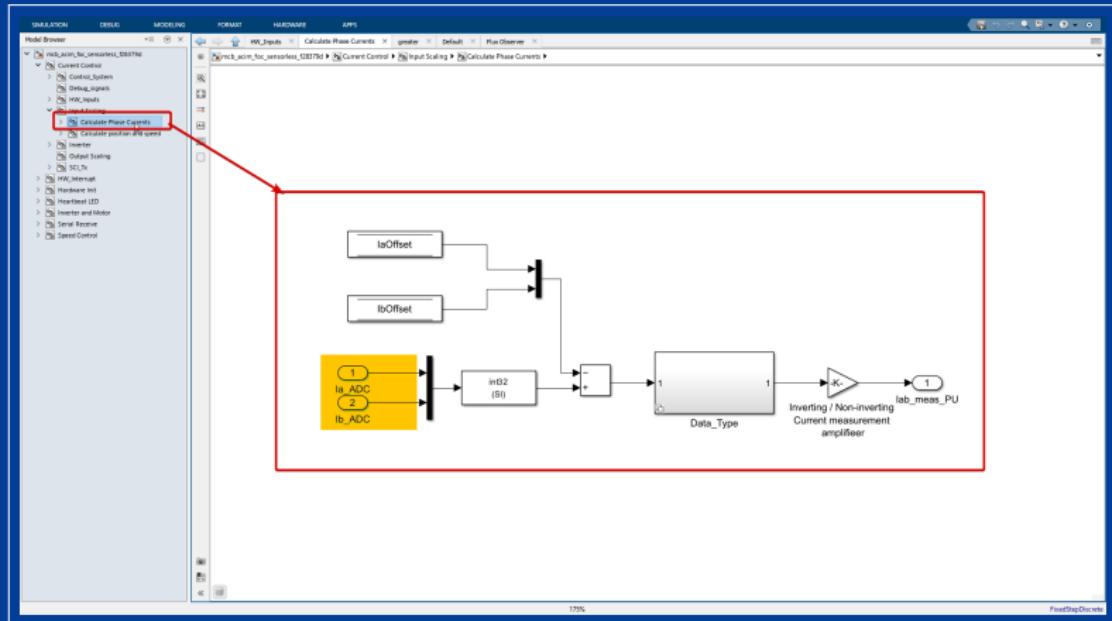


Figure: Current Measurement

# Position and Speed Estimation

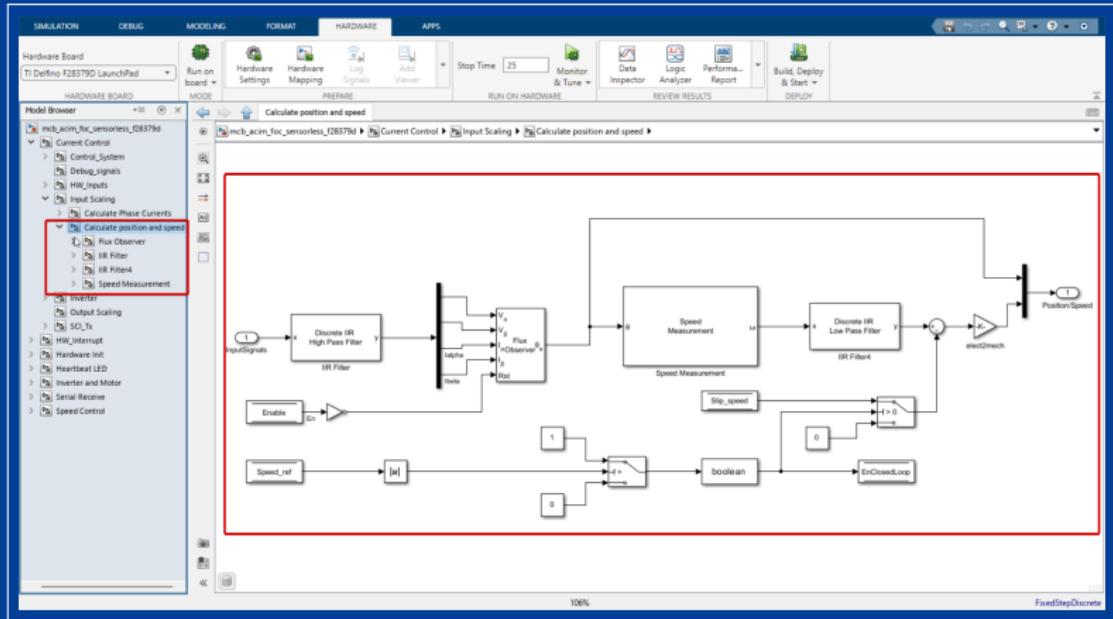


Figure: Position and Speed Estimation

# Current Control System

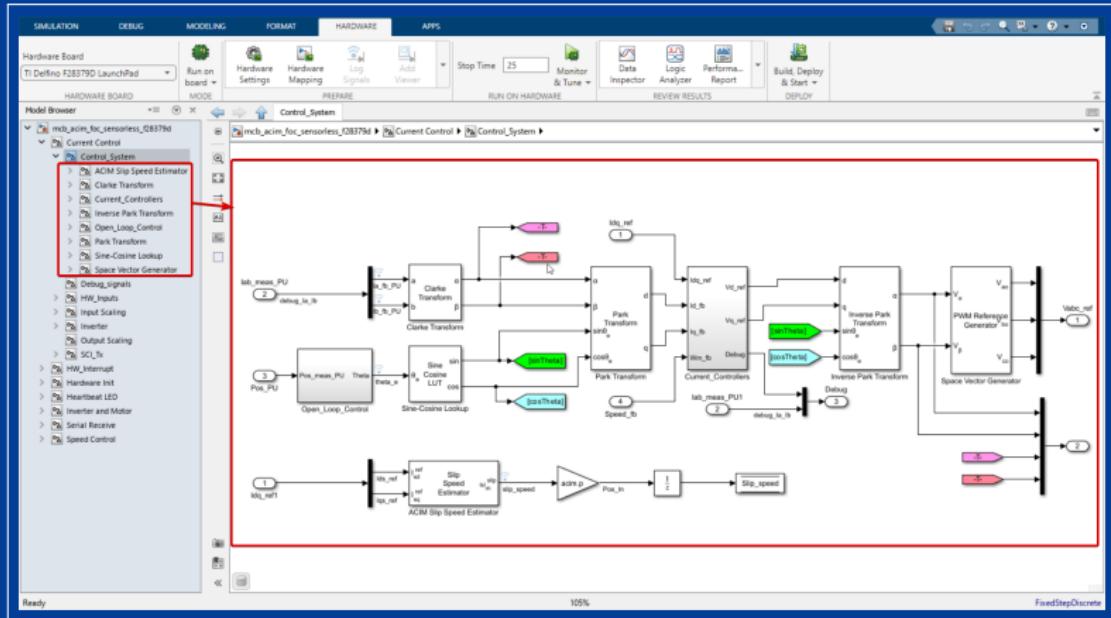


Figure: Current Control System

# Speed Response

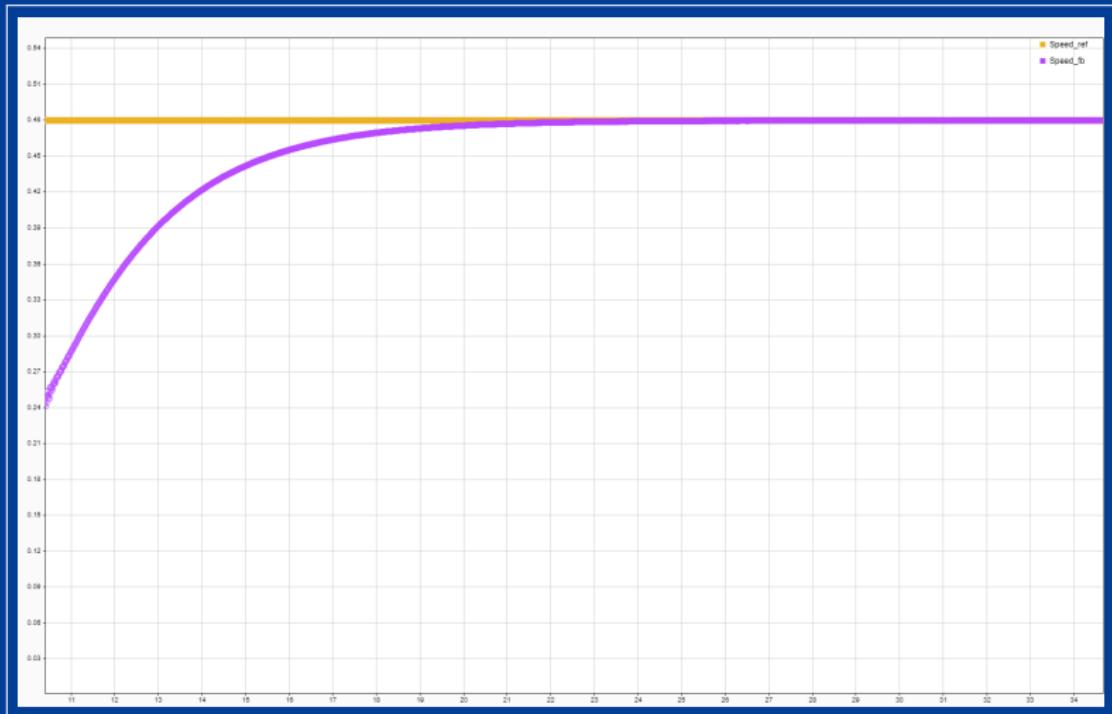


Figure: Speed Response

# Slip Speed

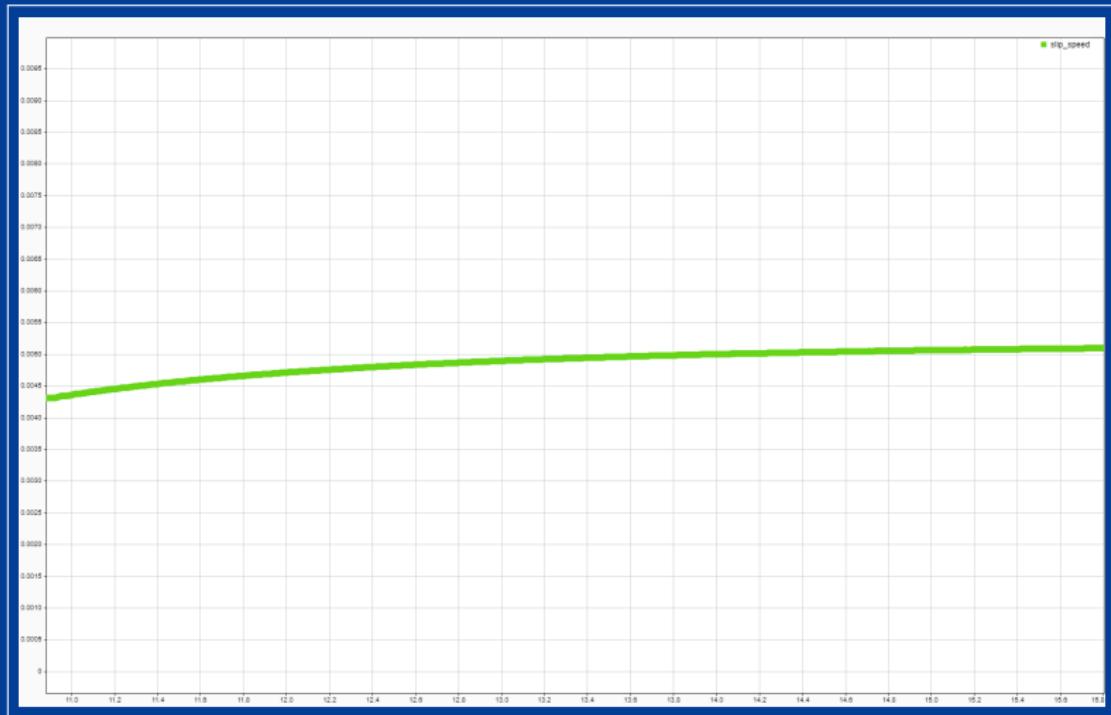


Figure: Slip Speed

## Ia and Ib Feedback/Measured Currents

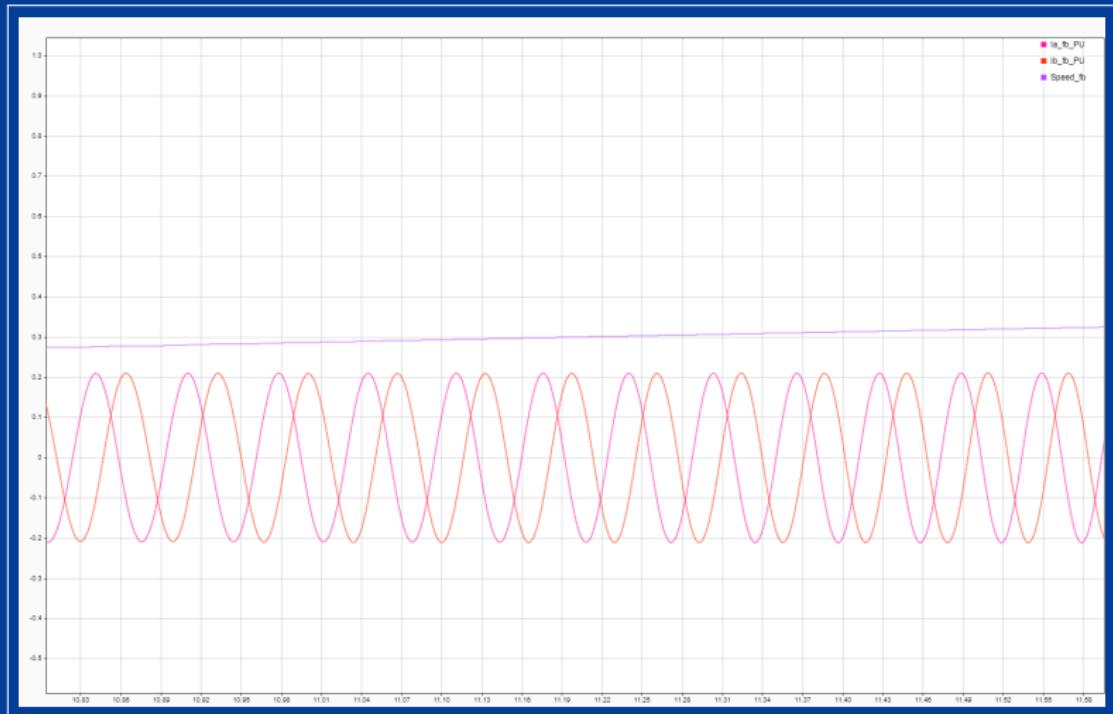


Figure: Ia and Ib Feedback/Measured Currents

## Id and Iq Reference Currents

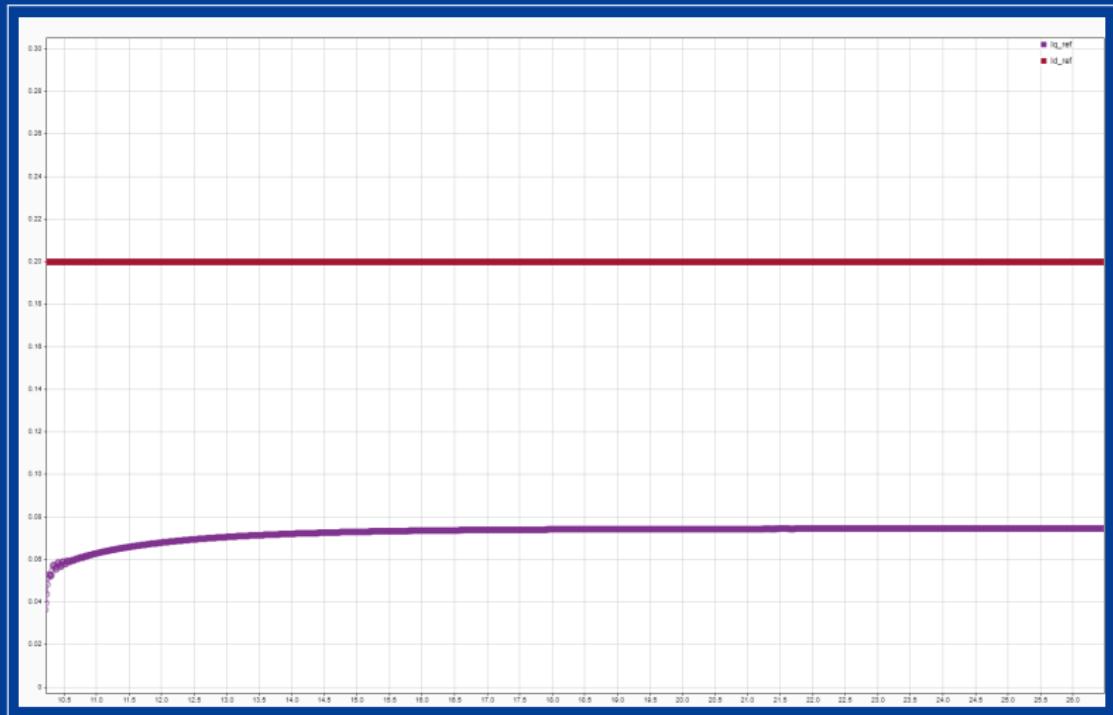
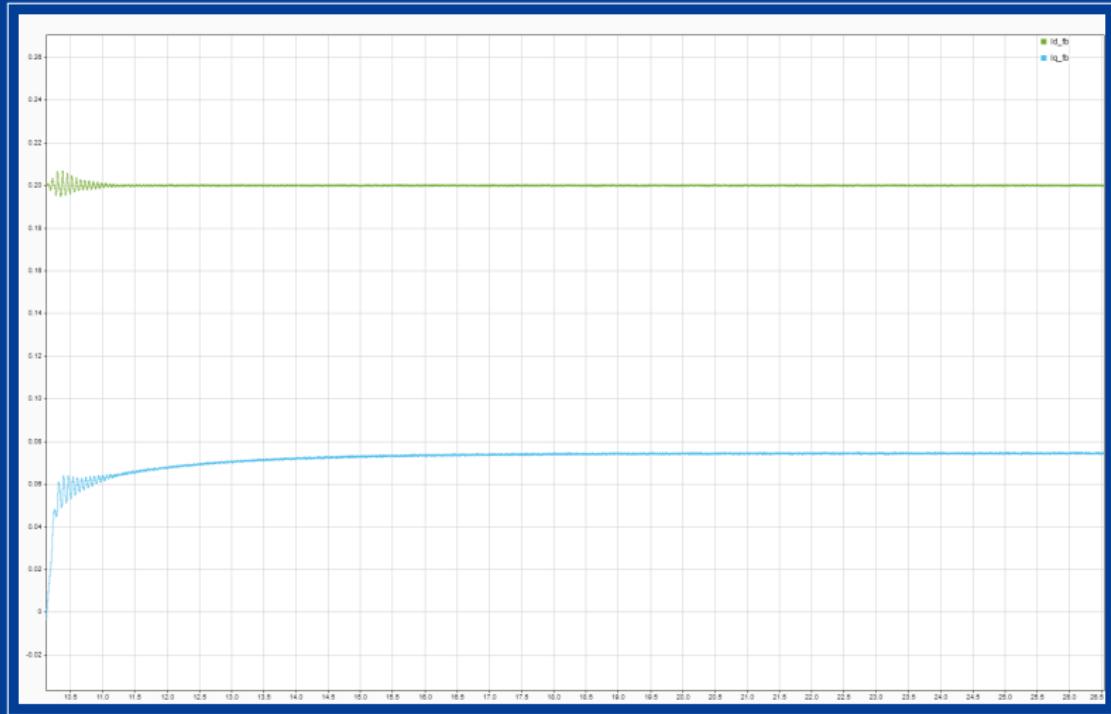
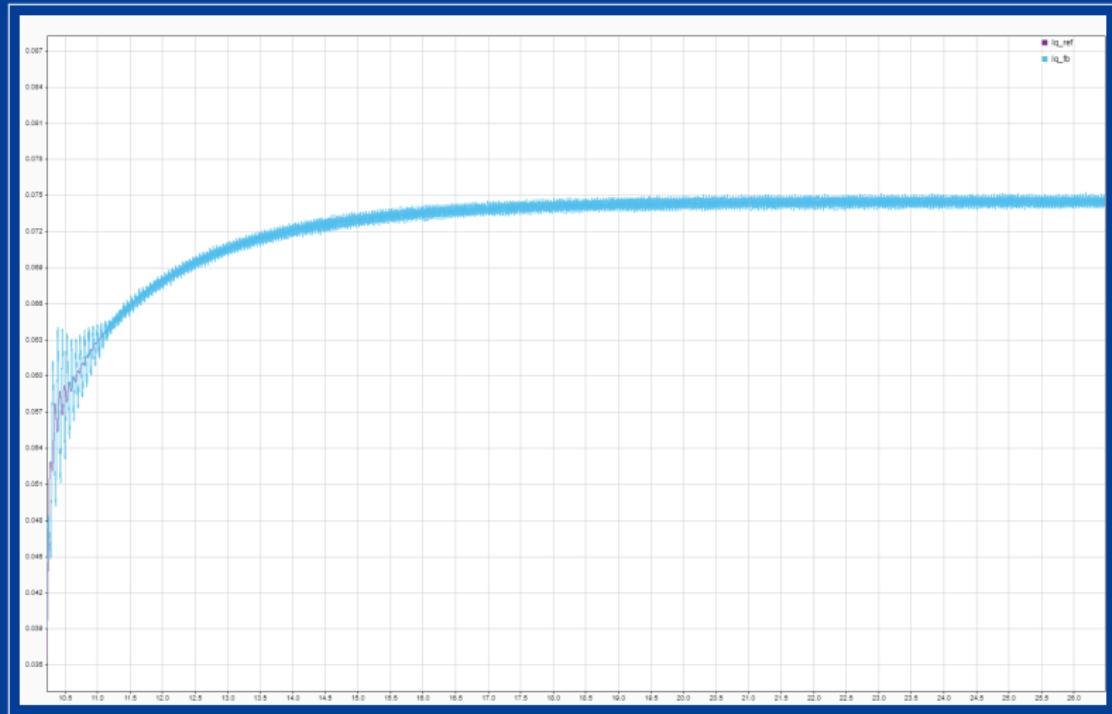


Figure: Id and Iq Reference Currents

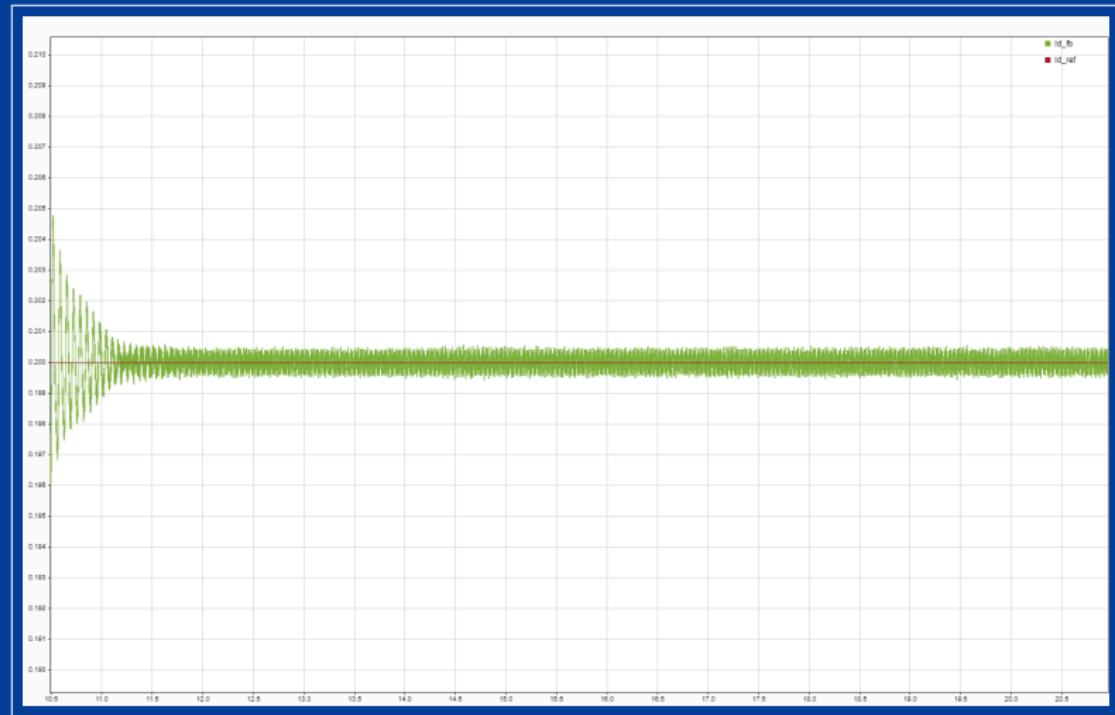
# Id and Iq Feedback Currents



# Iq Reference and Feedback Currents (Torque producing current)



# Id Reference and Feedback Currents (Magnetizing current)



# Induction Motor

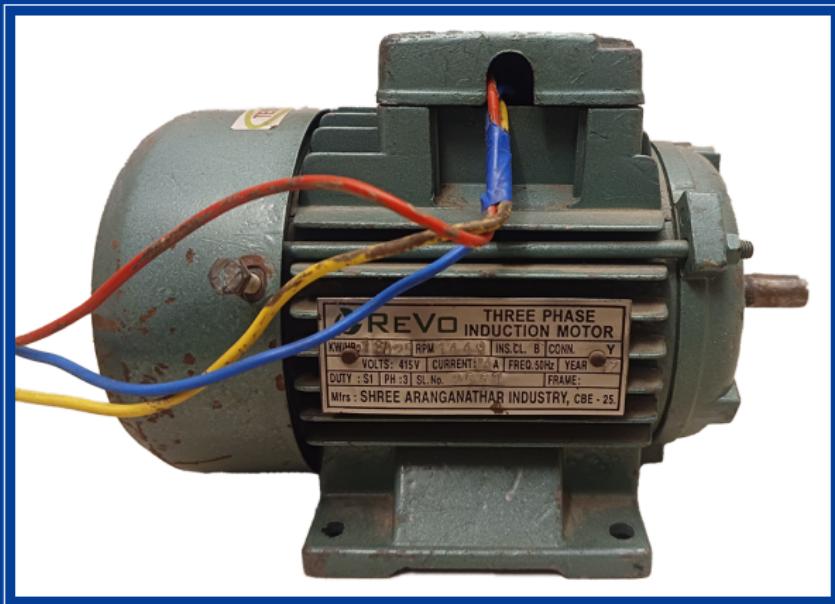


Figure: Induction Motor

# F28379d Launchpad

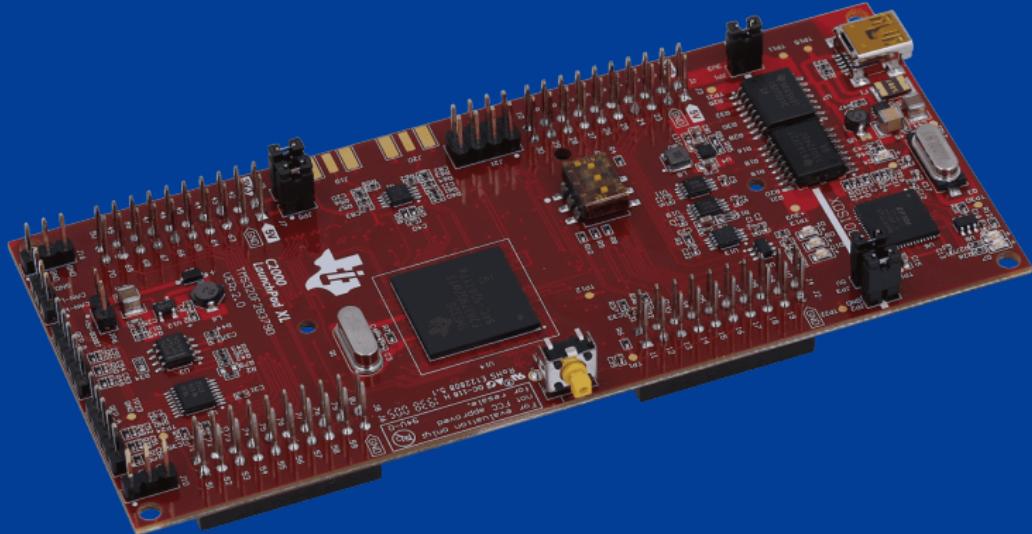


Figure: F28379D Launchpad

# Intelligent Power Module Fsam20sh60a



Figure 1. Package Overview

Figure: Intelligent Power Module FSAM20SH60A

# ACIM Parameter Estimation: No-Load Test



Figure: No-load test setup

# Fluke 434 Power Analyzer



Figure: Fluke 434 power analyzer

## No-load Test Circuit

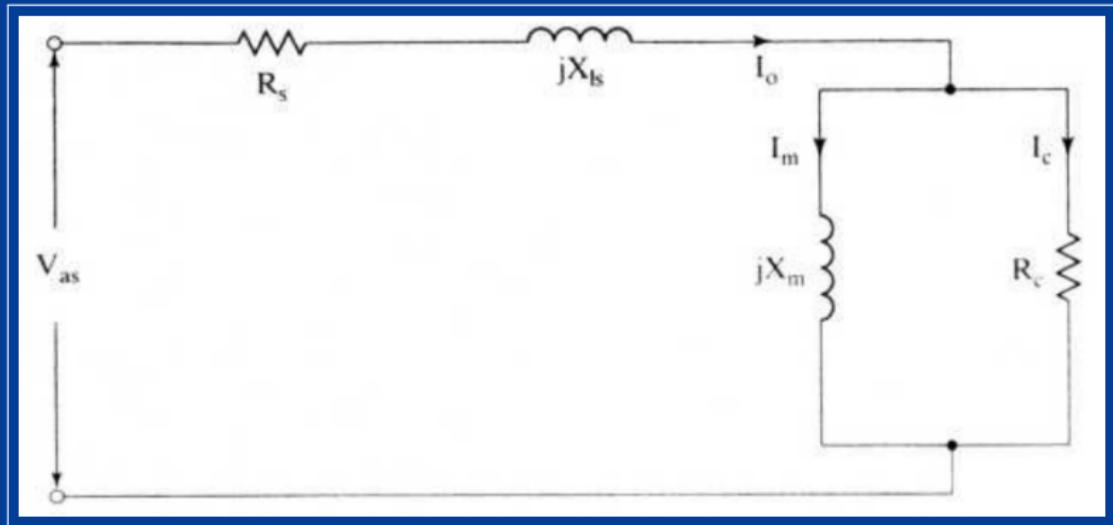


Figure: No-load test circuit

## ACIM Parameter Estimation: Blocked Rotor Test

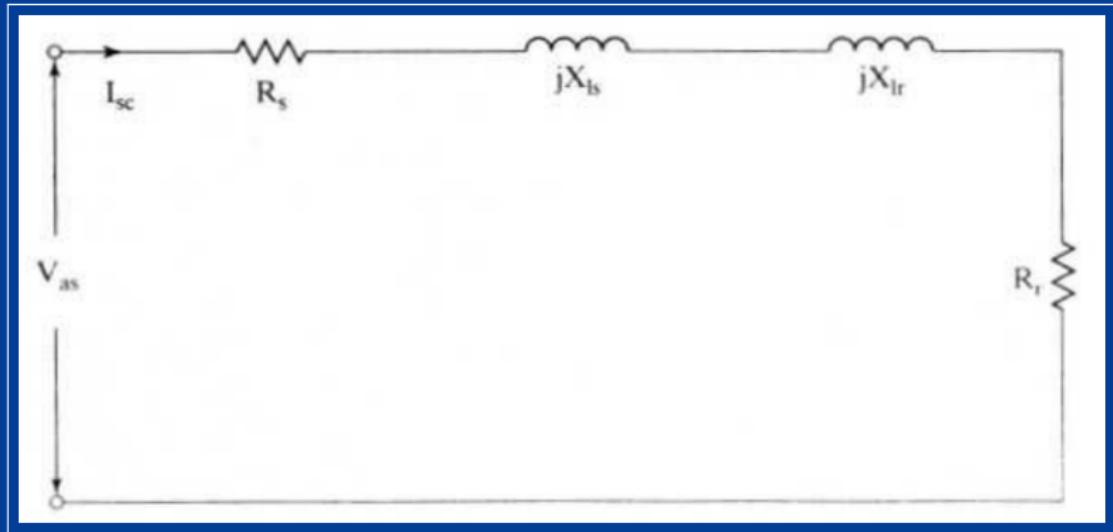


Figure: Blocked rotor test circuit

# ACIM Parameter Estimation Formulas

No-Load Test:

$$\cos \phi_0 = \frac{P_i}{V_{\text{as}} I_0}$$

$$I_m = I_0 \sin \phi_0$$

$$I_c = I_0 \cos \phi_0$$

$$L_m = \frac{V_{\text{as}}}{2\pi f_i I_m}$$

$$R_c = \frac{V_{\text{as}}}{I_c}$$

Blocked Rotor Test:

$$\cos \phi_{\text{sc}} = \frac{P_{\text{sc}}}{V_{\text{sc}} I_{\text{sc}}}$$

$$Z_{\text{sc}} = \frac{V_{\text{sc}}}{I_{\text{sc}}}$$

$$R_r = Z_{\text{sc}} \cos \phi_{\text{sc}} - R_s$$

$$X_{\text{eq}} = Z_{\text{sc}} \sin \phi_{\text{sc}}$$

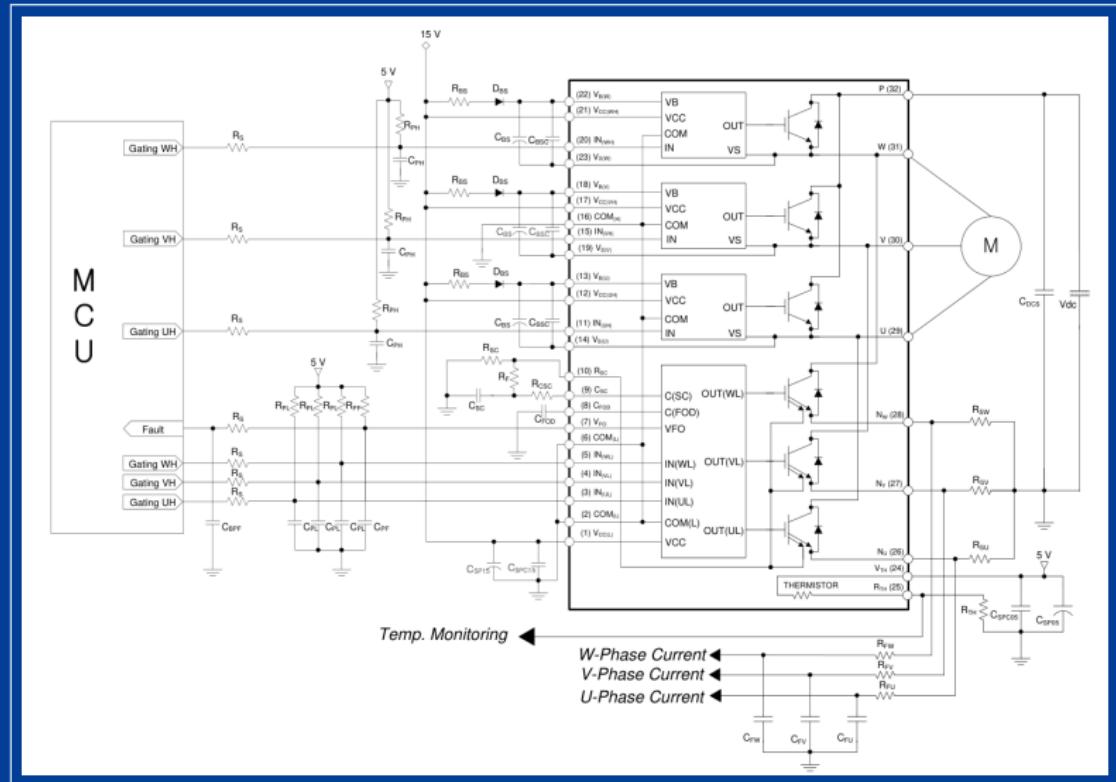
$$X_{\text{eq}} = X_{\text{ls}} + X_{\text{lr}}$$

## ACIM Parameter Estimation Results

Sensorless FOC 3PH parameter estimation				
	Efficiency	0.7		
	frequency	50	Hz	
Sno	TESTS to DO	Parameters	1	2
1	COLD TEST	DC STATOR RESISTANCE(Ohms)	65	60.8
		Temperature	Rated value	Room temperature
2	NO LOAD TEST	INPUT ACTIVE POWER , PH(Watts)	38.33	21.67
		INPUT STATOR VOLTAGE (Line to Line)*	415.00	350.00
		INPUT STATOR VOLTAGE (Phase)	239.60	202.07
		INPUT STATOR CURRENT , PH	0.77	0.63
		POWER FACTOR MEASURED	0.20	0.19
		PHI(radians)	1.37	1.38
		Im(A)	0.75	0.62
		Ic(A)	0.15	0.12
		Lm(H)	1.02	1.03
		Rc(Ohm)	1562.61	1709.26
3	LOCKED ROTOR TEST	INPUT ACTIVE POWER , PH	16.67	76.67
		INPUT STATOR VOLTAGE (Line to Line)**	100.00	219.00
		INPUT STATOR VOLTAGE (Phase)	57.74	126.44
		INPUT STATOR CURRENT , PH	0.47	1.00
		POWER FACTOR MEASURED	0.57	0.66
		PHI(radians)	0.97	0.85
		Zsc(Ohm)	123.72	126.44
		Rr(Ohm)	5.11	18.45
		Xeq(Ohm)	101.94	94.99
		Xls(Ohm)	50.97	47.49
		Xlr(Ohm)	50.97	47.49

## Figure: ACIM Parameter Estimation Results

# PCB Design



# MCU Interface Circuit

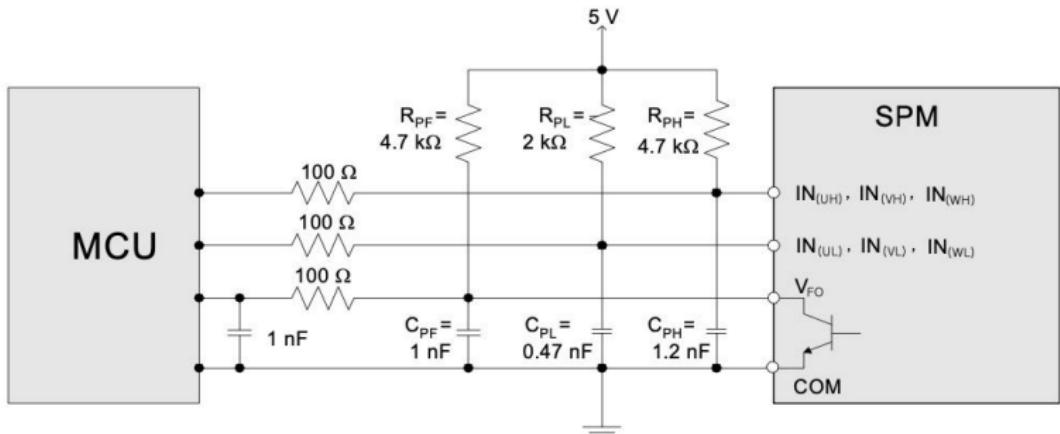


Figure 12. Recommended MCU I/O Interface Circuit

Figure: MCU Interface Circuit

# Short Circuit Protection Circuit

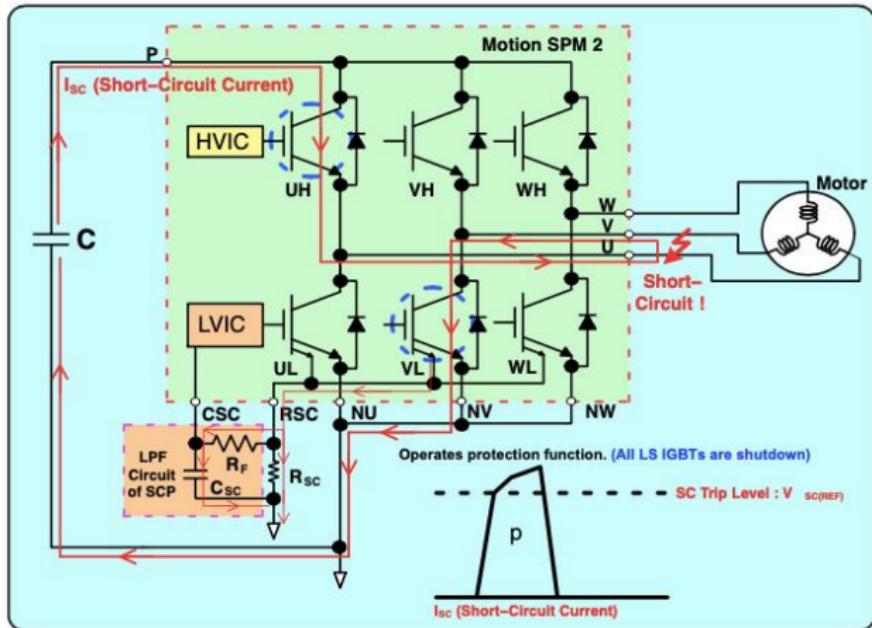


Figure 11. Operation of Short-Circuit Current Protection

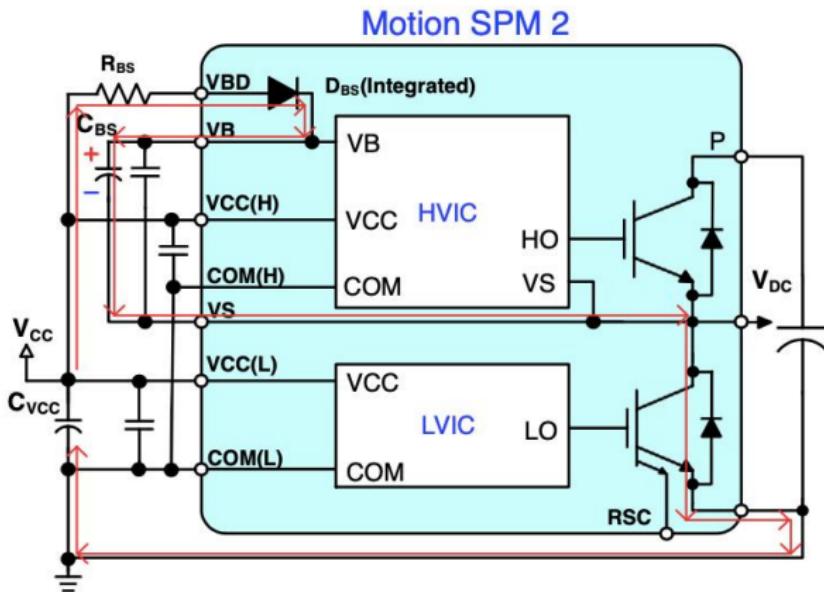
Figure: Short Circuit Protection Circuit

# Under Voltage Lockout Circuit

Control Voltage Range [V]	DIP-SPM Function Operations
0 ~ 4	<u>Control IC does not operate. Under voltage lockout and fault output do not operate.</u> <u>dV/dt noise on the main P-N supply might trigger the IGBTs.</u>
4 ~ 12.5	<u>Control IC starts to operate. As the under voltage lockout is set, control input signals are blocked and a fault signal F<sub>o</sub> is generated.</u>
12.5 ~ 13.5	Under voltage lockout is reset. IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so V <sub>CE(sat)</sub> and the switching loss will be larger than that under normal condition.
<u>13.5 ~ 16.5 for V<sub>CC</sub></u> <u>13 ~ 18.5 for V<sub>BS</sub></u>	<u>Normal operation. This is the recommended operating condition.</u>
16.5 ~ 20 for V <sub>CC</sub> 18.5 ~ 20 for V <sub>BS</sub>	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. <u>It causes increasing system noise.</u> And peak short circuit current might be too large for proper operation of the short circuit protection.
<u>Over 20</u>	<u>Control circuit in the DIP-SPM might be damaged.</u>

Figure: Under Voltage Lockout Circuit

## Bootstrap Circuit



**Figure 31. Current Path of Bootstrap Circuit for the Supply Voltage ( $V_{BS}$ ) of a HVIC when Low-Side IGBT Turns On**

Figure: Bootstrap Circuit

## Bootstrap Initial Charging

### *Selection of Bootstrap Capacitor Considering Initial Charging*

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time ( $t_{charge}$ ) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\Delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}}$$

(eq. 1)

where:

$V_F$  = Forward voltage drop across the bootstrap diode

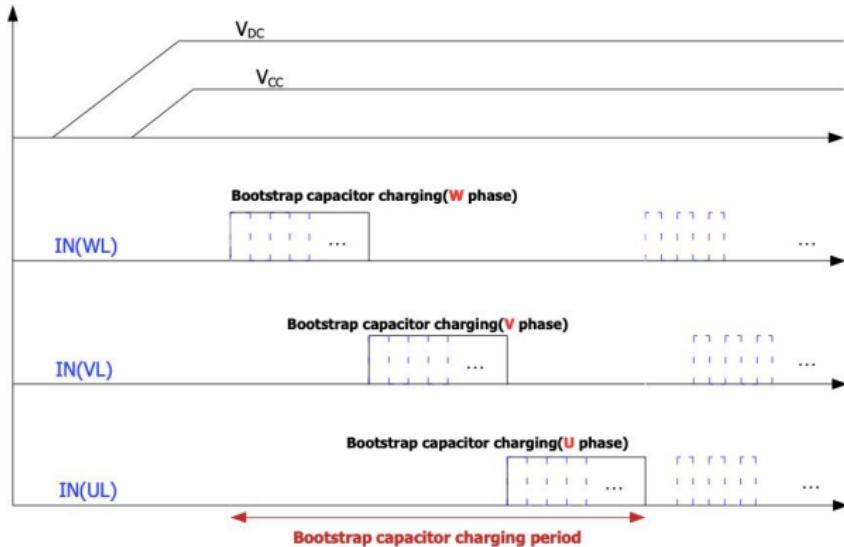
$V_{BS(min)}$  = The minimum value of the bootstrap capacitor

$V_{LS}$  = Voltage drop across the low-side IGBT or load

$\Delta$  = Duty ratio of PWM

Figure: Bootstrap Initial Charging

## Bootstrap Initial Charging



**Figure 33. Recommended Initial Bootstrap Capacitors Charging Sequence**

Figure: Bootstrap Initial Charging

# PCB Layout Design

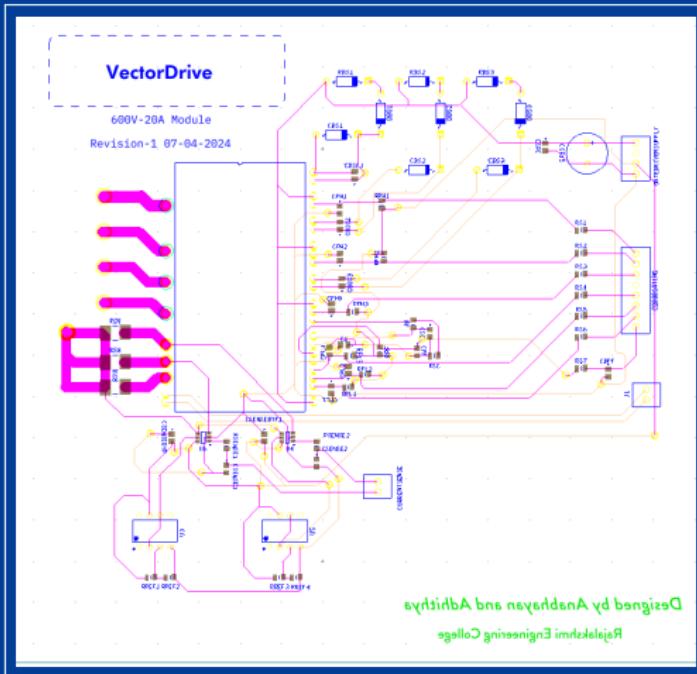


Figure: PCB Layout Design in Ultiboard

## 3D View of PCB Layout

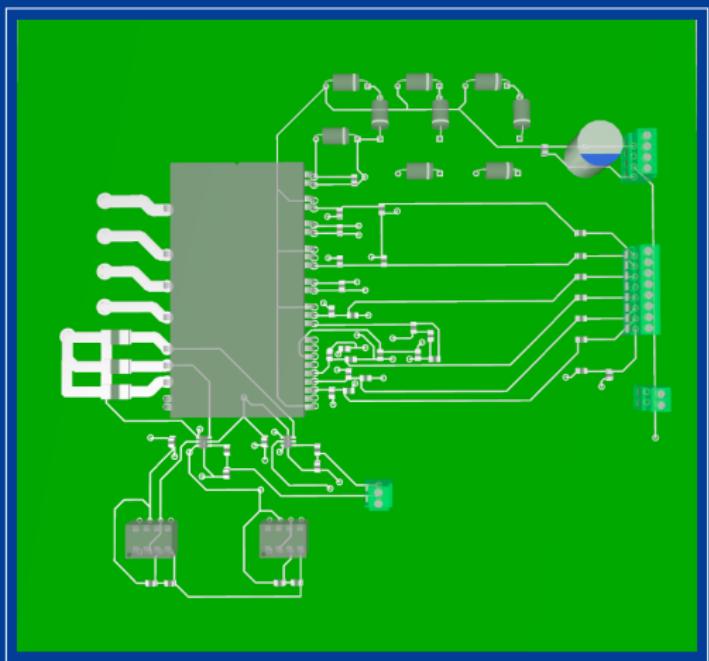


Figure: 3D View of PCB Layout Design in Ultiboard

## Current Sensing Circuit

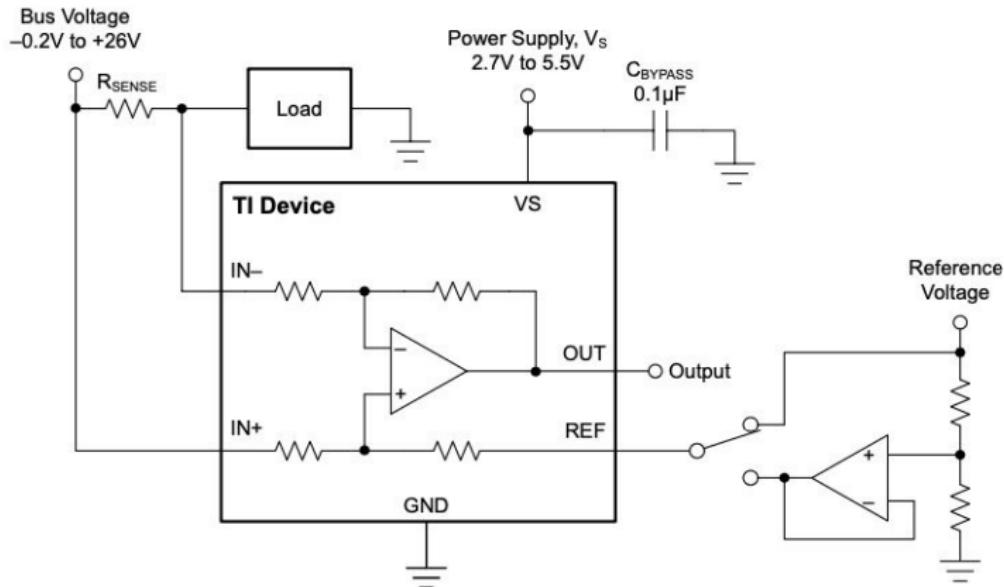


Figure 8-7. Measuring Bidirectional Current

Figure: Current Sensing Circuit

# Current Measurement

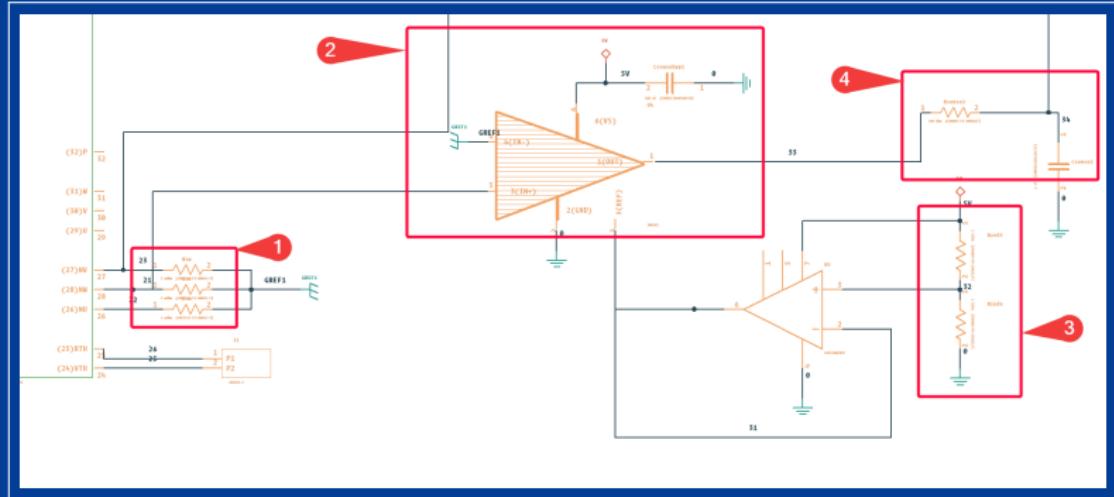


Figure: Current Sensing Circuit in Multisim (one phase shown)

# ePWM Module



www.ti.com

Enhanced Pulse Width Modulator (ePWM)

## 15.7 Dead-Band Generator (DB) Submodule

Figure 15-33 illustrates the dead-band submodule within the ePWM.

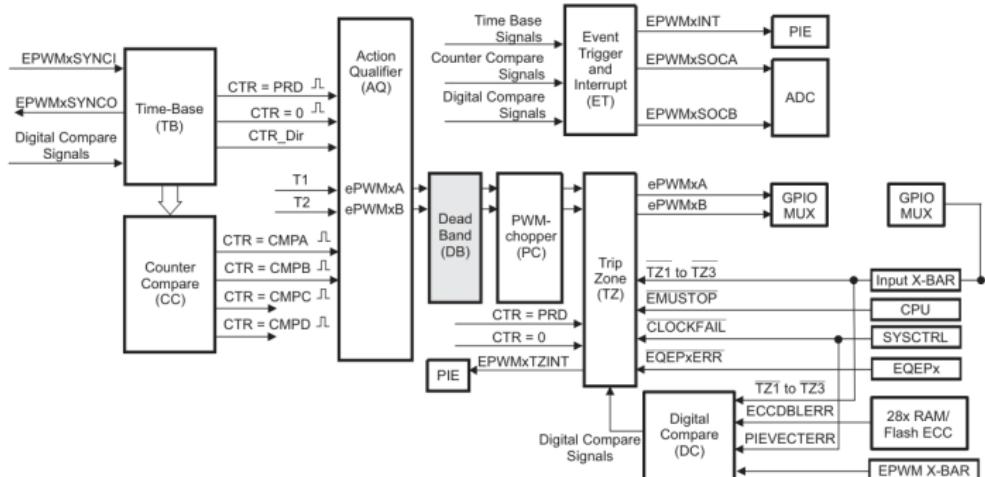


Figure 15-33. Dead\_Band Submodule

Figure: ePWM Module

# Space Vector Pulse Width Modulation



Figure: ePWM block in Simulink

## Counter Compare and Timer Period Visualization

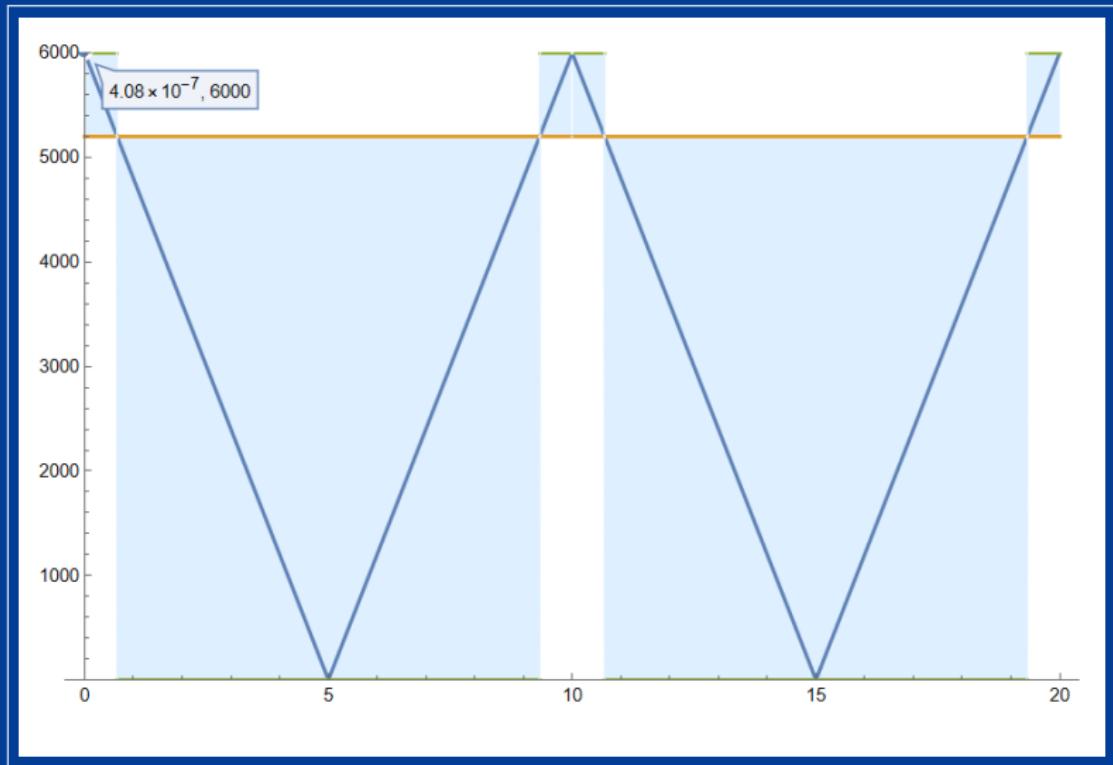


Figure: Counter Compare High

## Counter Compare and Timer Period Visualization

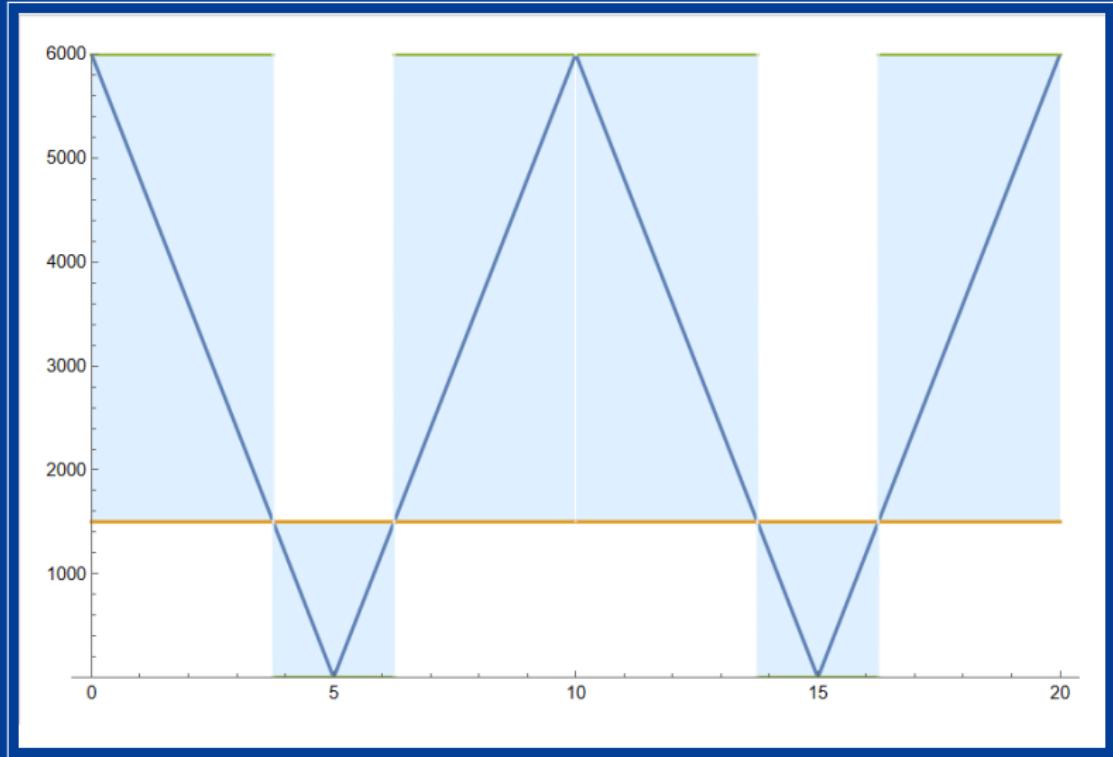


Figure: Counter Compare Low

# Counter Compare and Timer Period Visualization

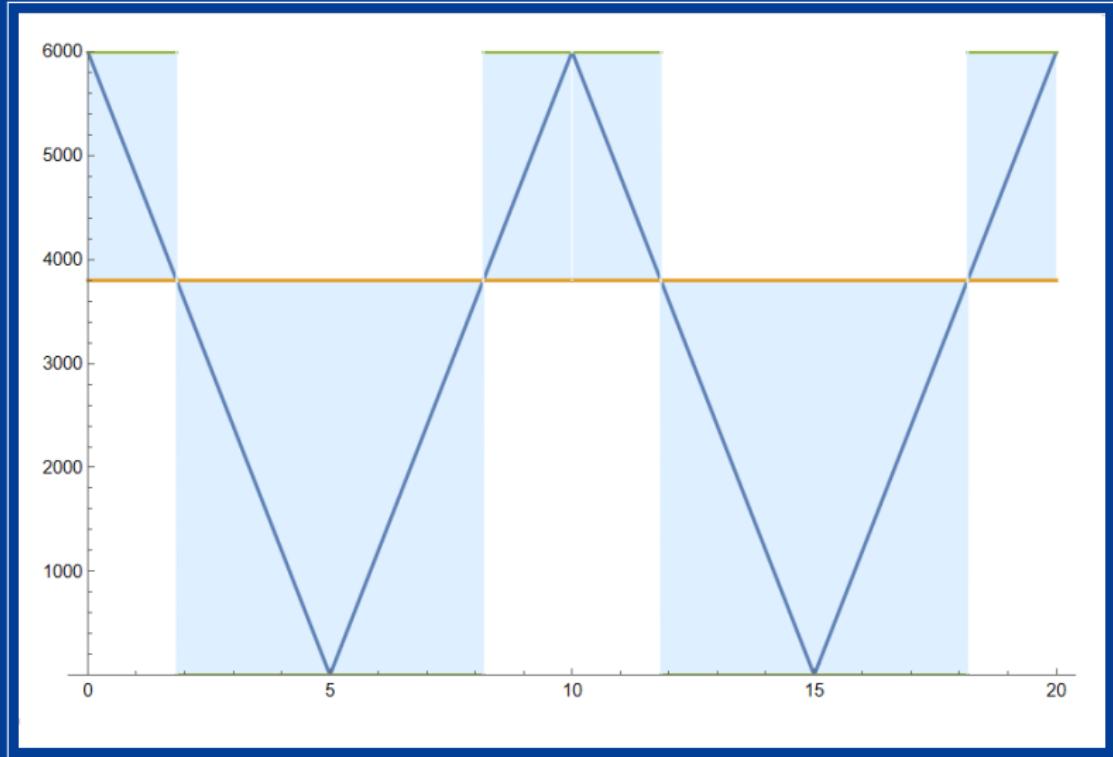


Figure: Counter Compare half

## TBPRD Calculation

- ▶ PWM Frequency ( $F_{PWM}$ ):  
15 kHz (recommended by  
FSAM20SH60A datasheet)
- ▶ System Clock (SYSCLK):  
200 MHz
- ▶ High Speed Clock Divider  
(HSPCLKDIV): 1
- ▶ Clock Divider (CLKDIV): 1

$$T_{PWM} = \frac{1}{F_{PWM}}$$

$$T_{TBCLK} = \frac{SYSCLK}{HSPCLKDIV \times CLKDIV}$$

$$TBPRD = \frac{T_{PWM}}{2 \times T_{TBCLK}}$$

$$T_{PWM} = \frac{1}{15 \times 10^3} \text{ seconds}$$

$$T_{TBCLK} = \frac{200 \times 10^6}{1 \times 1} = 200 \times 10^6 \text{ Hz}$$

$$TBPRD = \frac{\frac{1}{15 \times 10^3}}{2 \times 200 \times 10^6} \approx 6667$$

Therefore, the Timer Period (TBPRD) is 6667.

# SVPWM Simulink Model

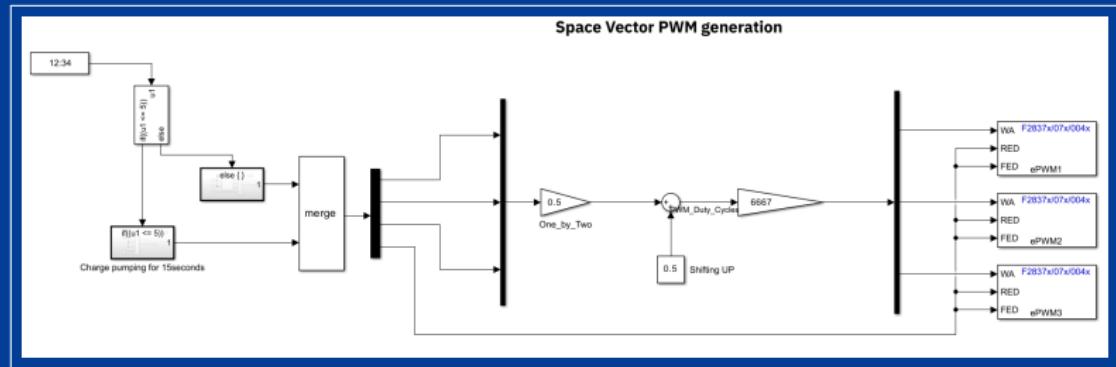


Figure: SVPWM Simulink Model

# ePWM Configuration

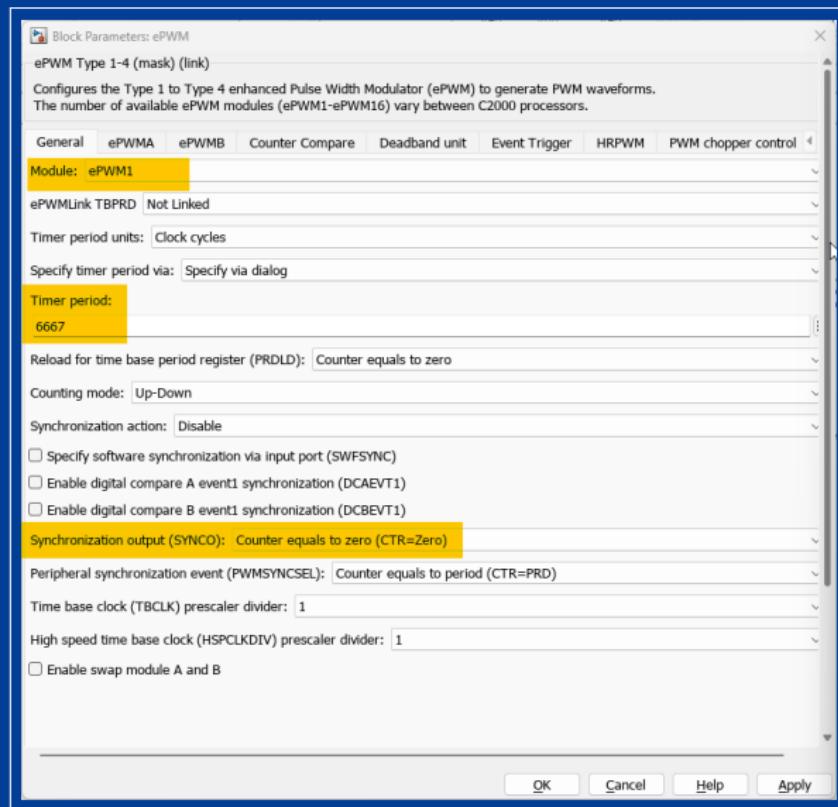


Figure: ePWM configuration in Simulink

# SVPWM with Low Pass Filter

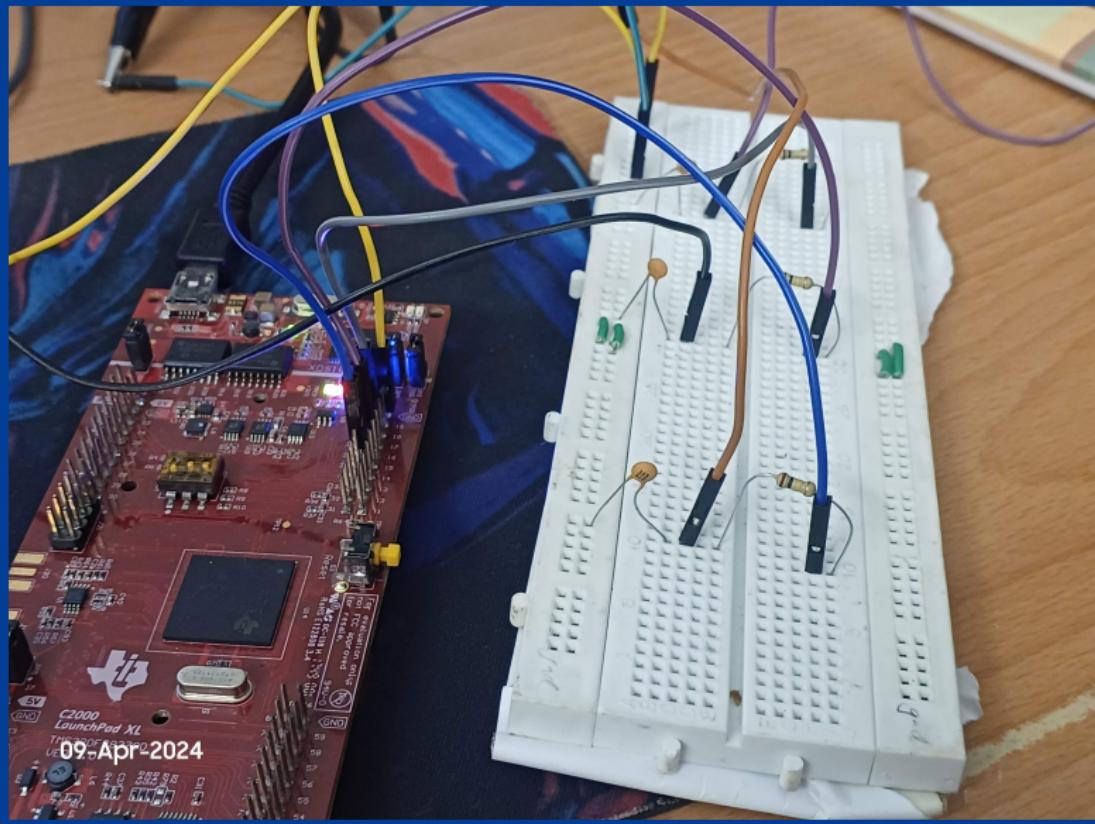


Figure: Hardware setup with RC filter and Launchpad

# Output of SVPWM with LPF

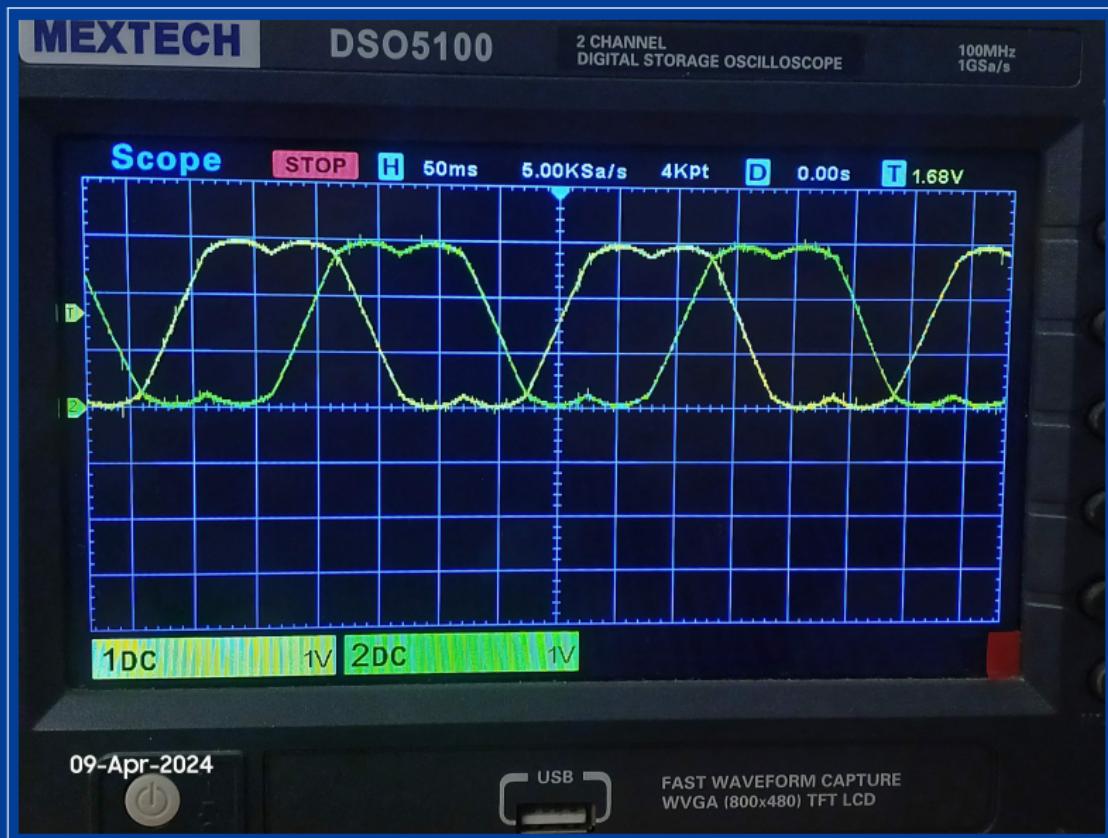


Figure: Output of SVPWM with low pass filter

# Dead Band Configuration

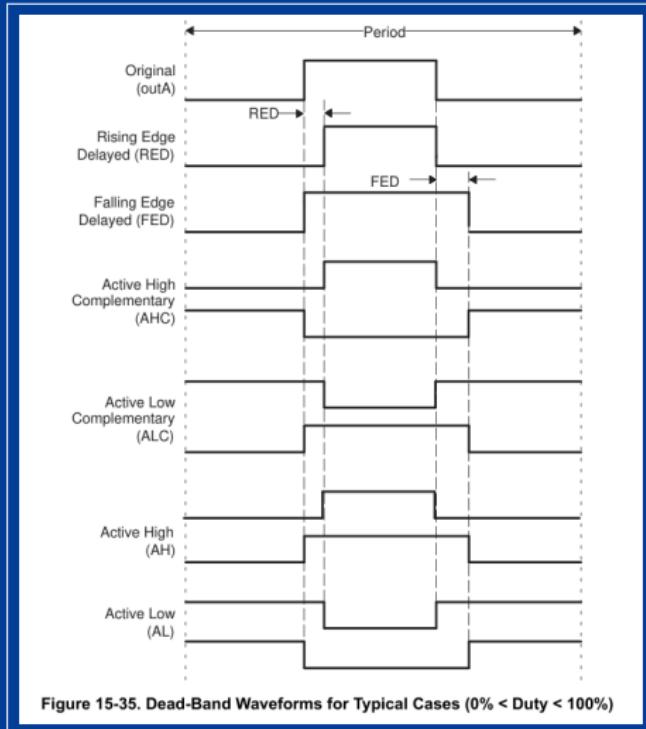


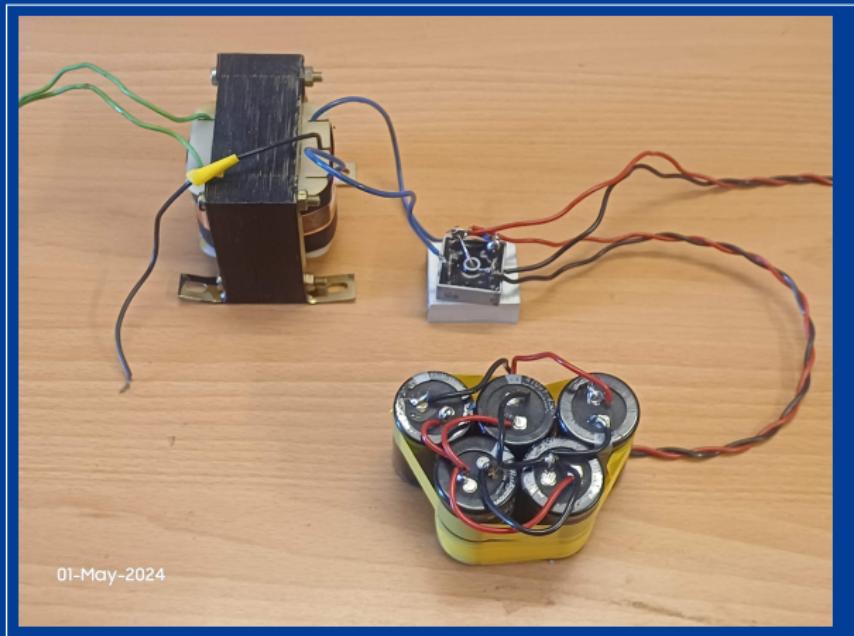
Figure: Dead band time

# Dead Band Configuration



Figure: Dead band time

## DC Bus Setup



**Figure:** DC Bus Setup: 230V AC to 48V DC conversion with capacitor banks for stable power delivery

# Inverter and Controller

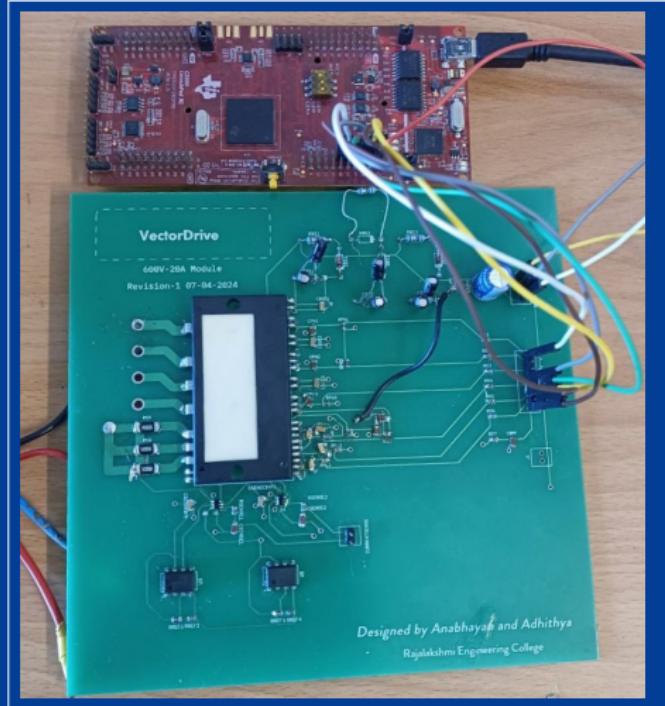
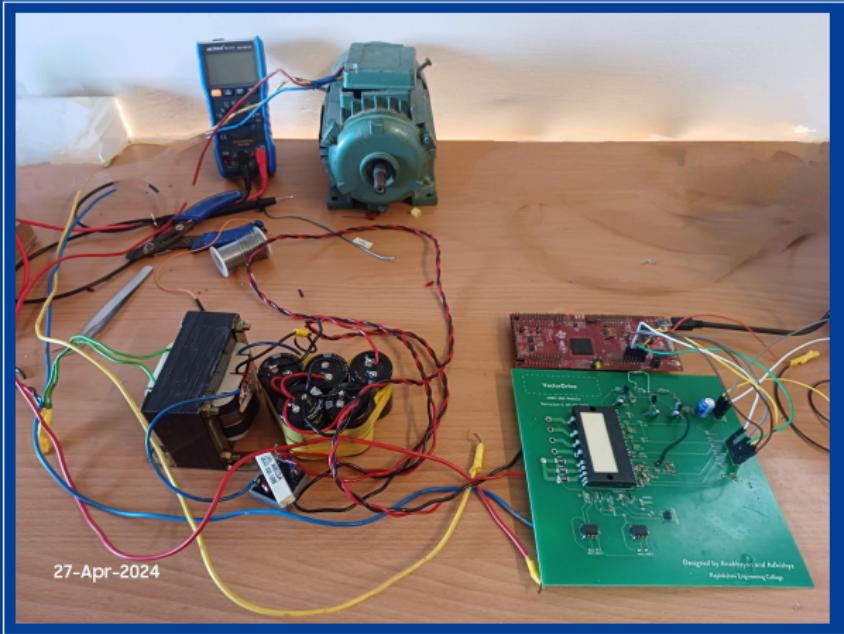


Figure: Inverter (FSAM20SH60A) and Controller (F28379D Launchpad) Setup

## Complete Hardware Setup



**Figure:** Experimental Setup for Motor Control System with Induction Motor, DC Bus, Inverter, and Controller

## Challenges: False Positives from Fault Alarm

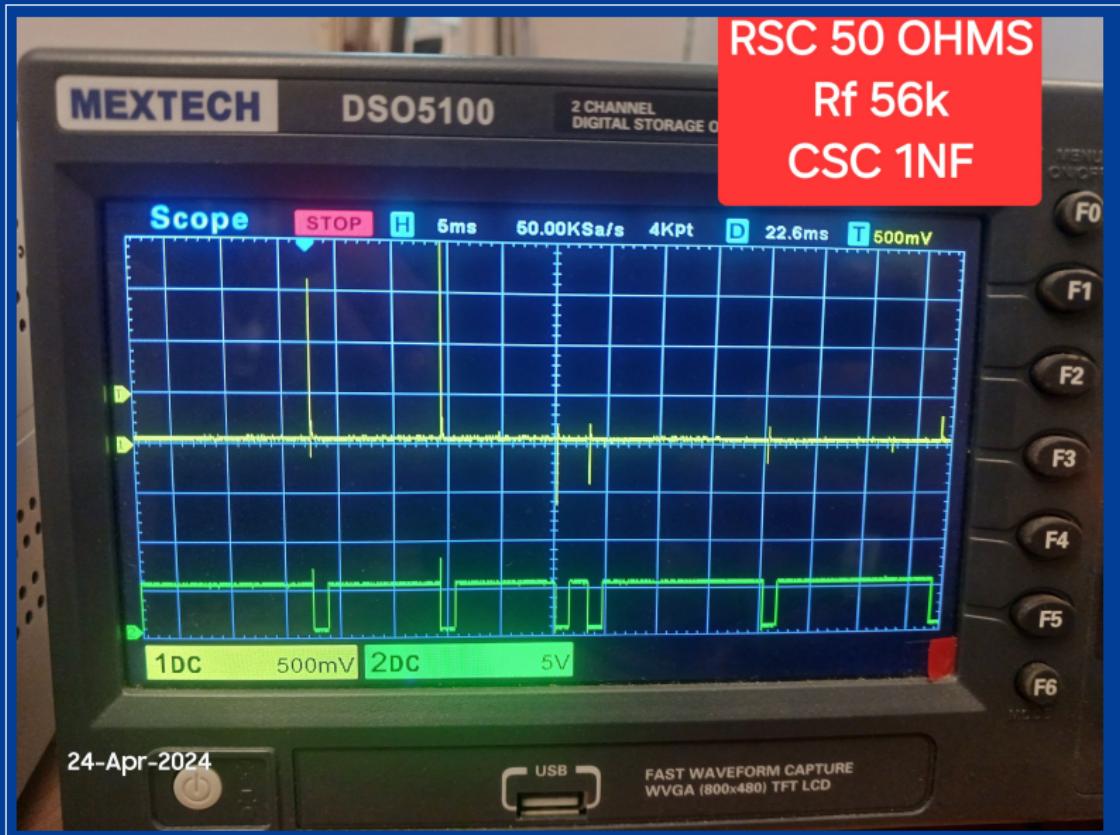


Figure: Vcc Noise and Fault Alarm Signal

# Mitigation Strategies

## ► Isolation Attempts:

- ▶ Separate control and power stage grounds using separate transformers and rectifiers.
- ▶ Temporarily shorted RSC and CSC pins to ground to assess external noise influence.

## ► Noise Reduction Techniques:

- ▶ Added metal film capacitors across the DC bus to suppress switching transients.
- ▶ Reduced switching frequency to minimize voltage/current change rate and noise.

## ► Future Considerations:

- ▶ Further noise reduction through filtering on control signals and power supply lines.
- ▶ Improved PCB layout to minimize noise coupling paths and optimize component placement.

# Conclusion

## ► **Achievements:**

- ▶ Successful simulation of FOC system demonstrating significant performance improvements.
- ▶ Design and development of hardware setup including PCB design and component integration.
- ▶ Identification and analysis of challenges related to noise and false alarms.

## ► **Challenges:**

- ▶ Persistent false positives from the IPM's fault alarm despite implemented mitigation strategies.
- ▶ Limited hardware validation due to the unresolved fault alarm issue.

## ► **Future Work:**

- ▶ Explore additional noise reduction techniques and PCB layout optimization.
- ▶ Investigate alternative IPM modules or fault detection mechanisms.
- ▶ Implement and validate the closed-loop FOC system in hardware upon resolving the challenges.