0.1 Space Vector Pulse Width Modulation

Space Vector PWM has several advantages over Sine PWM

- Higher voltage utilization: SVPWM can utilize up to 15% more DC bus voltage compared to SPWM. This means for the same DC supply voltage, an inverter with SVPWM can provide a higher output voltage.
- Better harmonic performance: SVPWM results in lower total harmonic distortion (THD) compared to SPWM. This leads to a better quality of the output voltage and current waveforms, which is particularly important in applications like drives where harmonics can cause heating and torque pulsations.
- Reduced switching losses: SVPWM requires fewer switching operations for the inverter switches compared to SPWM. This results in lower switching losses, leading to higher efficiency and reduced heating of the inverter switches.
- Improved dynamic response: The space vector representation used in SVPWM allows for a more precise control of the output voltage vector, leading to an improved dynamic response. This is particularly beneficial in applications like motor drives where a fast dynamic response is required.
- Vector control capability: SVPWM allows for vector control of the output voltage, which is not possible with SPWM. This enables more complex control strategies, such as field-oriented control (FOC), which can provide better performance in applications like motor drives.
- Flexibility: SVPWM allows for flexible control of the output voltage magnitude and frequency, as well as the phase relationship

between the output voltage and current. This flexibility makes it suitable for a wide range of applications.

0.1.1 Generation of Space Vector PWM with C2000 microcontroller

To generate space vector PWM wave for the switches C2000 series microcontroller offers a hardware level module called ePWM or enhanced PWM module. It enables to generate PWM waves with high flexibility.

To generate symmetrical waveform, the ePWM's internal timer is configured in up-down count mode.

0.1.2 PWM Frequency Calculation

Variable Definitions

Symbol	Description
F_{PWM}	Frequency of PWM (Hz)
T_{PWM}	Time period of PWM (seconds)
$TBCLK$	Time base clock (Hz)
T_{TBCLK}	Time period of time base clock (in seconds)
$TBPRD$	Timer period (in clock cycles)
$EPWMCLK$	ePWM module clock (in Hz)
$HSPCLKDIV$	High speed clock divider
$CLKDIV$	Clock divider

The period of the PWM signal can be calculated using the formula:

$$T_{\text{PWM}} = 2 \times TBPRD \times T_{\text{TBCLK}}$$

where $TBPRD$ is the time base period.

0.2 PWM Frequency (F_{PWM})

The frequency of the PWM signal is defined as the inverse of the PWM period:

$$F_{\text{PWM}} = \frac{1}{T_{\text{PWM}}}$$

0.3 Time Base Clock (T_{TBCLK})

The time base clock is given by:

$$T_{\text{TBCLK}} = \frac{\text{EPWMCLK}}{\text{HSPCLKDIV} \times \text{CLKDIV}}$$

- EPWMCLK is the clock frequency dedicated to the PWM module.
- HSPCLKDIV and CLKDIV are the dividers for the high-speed PWM clock.

0.4 Timer Period ($TBPRD$)

$$TBPRD = \frac{T_{\text{PWM}}}{2 \times T_{\text{TBCLK}}}$$

According to the FSAM20SH60A datasheet, a 15 kHz switching frequency is recommended for optimal performance. The dividers HSPCLKDIV and CLKDIV are both set to 1. Given that the EPWMCLK is derived from the system clock (SYSCLK) which operates at 200 MHz, the time base clock can be calculated as follows:

Given the PWM period T_{PWM} and the TBCLK frequency T_{TBCLK}, we need to solve for $TBPRD$ (Time Base Period Register). The calculations are as follows:

1. **Calculation of $T_{\mathbf{PWM}}$:**

$$T_{\text{PWM}} = \frac{1}{15 \times 10^3} \text{ seconds}$$

This represents the period of the PWM.

2. **Calculation of $T_{\mathbf{TBCLK}}$:**

$$TBCLK = \frac{200 \times 10^6}{1 \times 1} = 200 \times 10^6 \text{ Hz}$$

This is the frequency of the TBCLK (Time Base Clock).

3. **Solving for $TBPRD$:** With T_{PWM} and T_{TBCLK} known, we get 6667.

Figure 0.1 below shows the ePWM block in Simulink, which is used generate PWM waveforms from microcontroller.

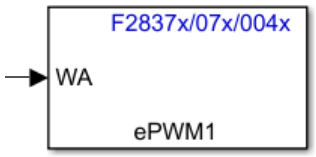

Figure 0.1: ePWM block in Simulink

Figure 0.2 below shows the ePWM module configuration.

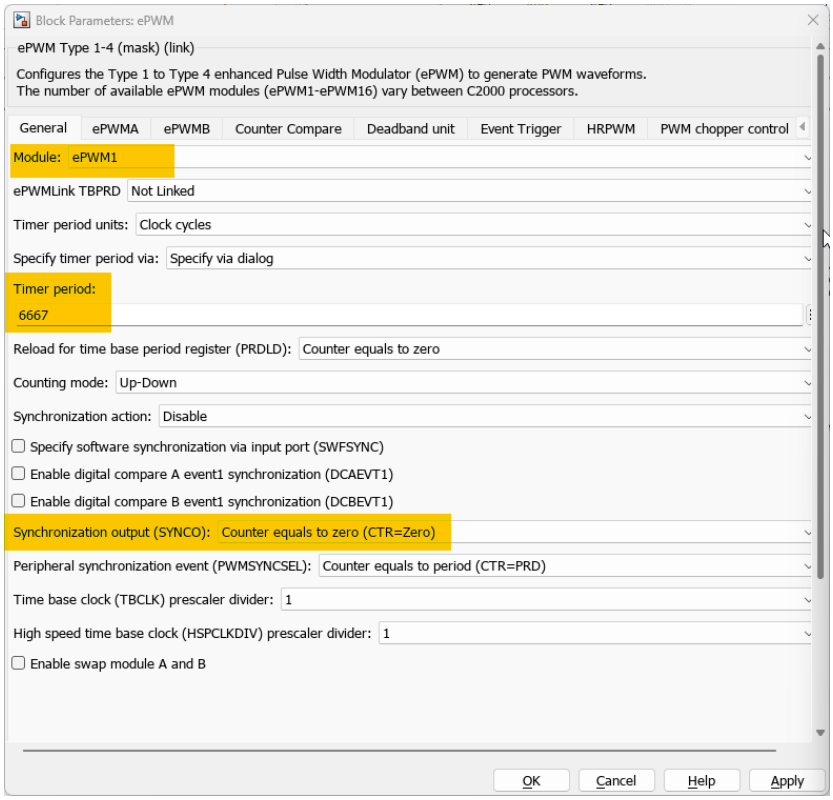

Figure 0.2: ePWM configuration in Simulink

0.4.1 Output of SVPWM with low pass filter

The fundamental low frequency wave is buried within the 15 kHz carrier wave. Thus passed through a low pass filter to extract the fundamental frequency and hardware setup is shown in Figure 0.3.

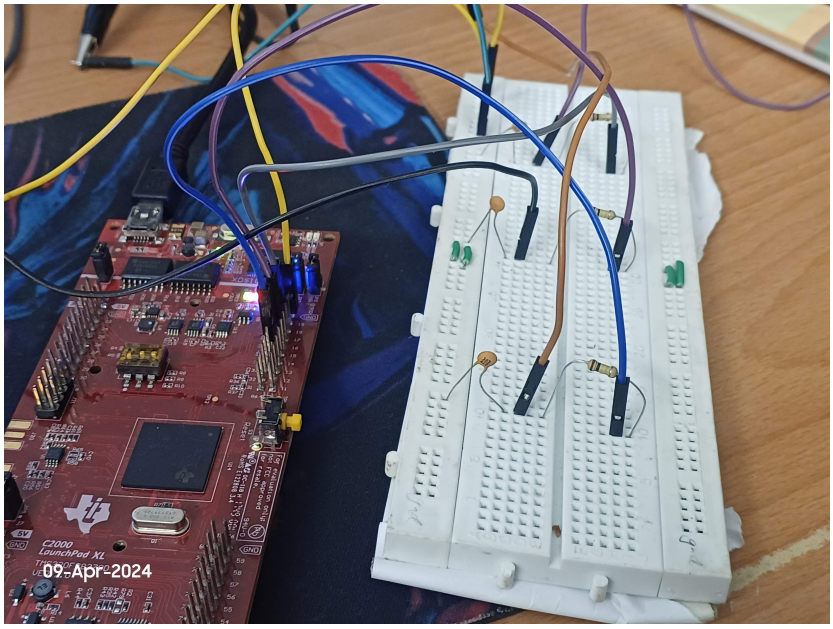

Figure 0.3: Hardware setup with RC filter and Launchpad

The output of the SVPWM with low pass filter is shown in Figure 0.4.

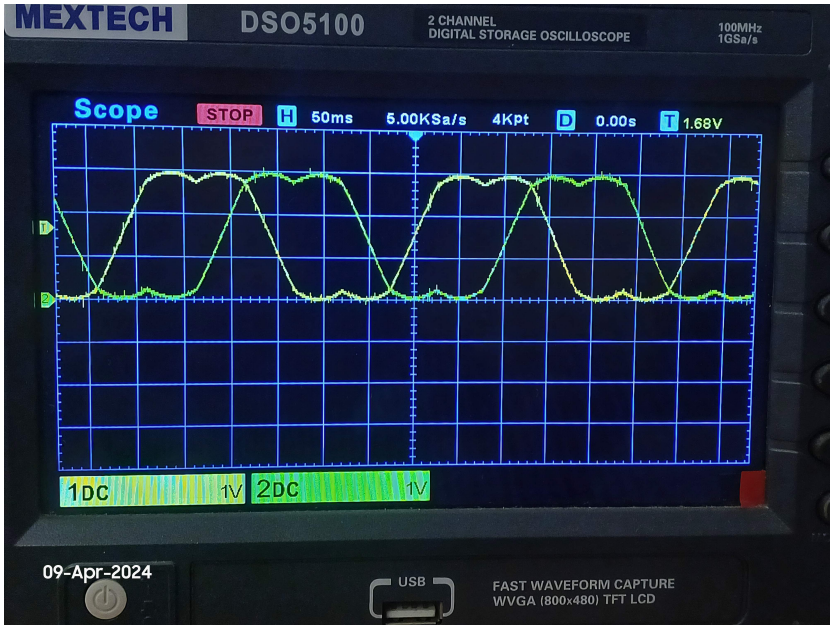

Figure 0.4: Output of SVPWM with low pass filter

0.4.2 Dead band

Dead band is a time delay between the switching of the upper and lower switches in the inverter. This is necessary to prevent short circuiting of the DC bus. The dead band time is set in the ePWM module. The dead band time can be configured in the ePWM module, and it can be specified in terms of the number of clock cycles or in terms of time. The datasheet of FSAM20SH60A smart power module recommends a dead band time of atleast 3us.

An example of 20us dead band time is shown in Figure 0.5. The two waveforms shown are output of ePWM 1A and 1B which will be given to the upper and lower switches of the inverter respectively.

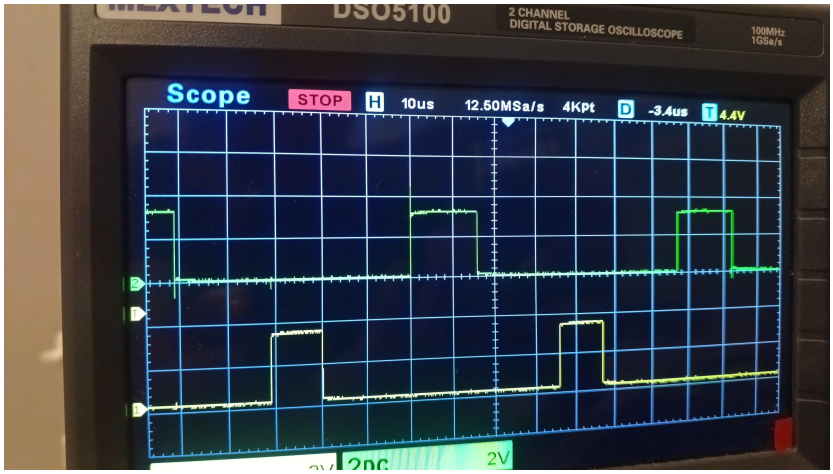

Figure 0.5: Dead band time