

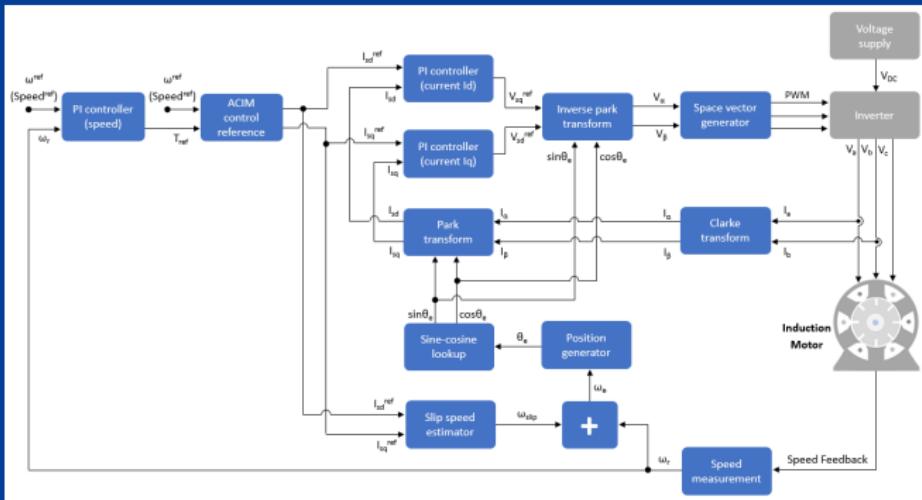
D.S.P. based Field Oriented Control of Induction motor

Adhithya S 200901002
Anabhayan S P 200901008

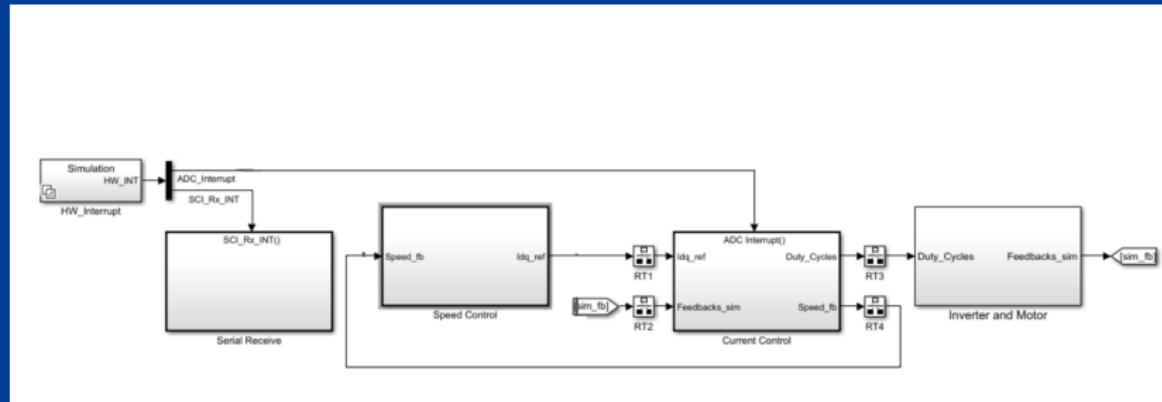
Under the guidance of Dr S Rama Reddy
Dean - Electrical sciences

*Department of Electrical and Electronics Engineering
Rajalakshmi Engineering college*

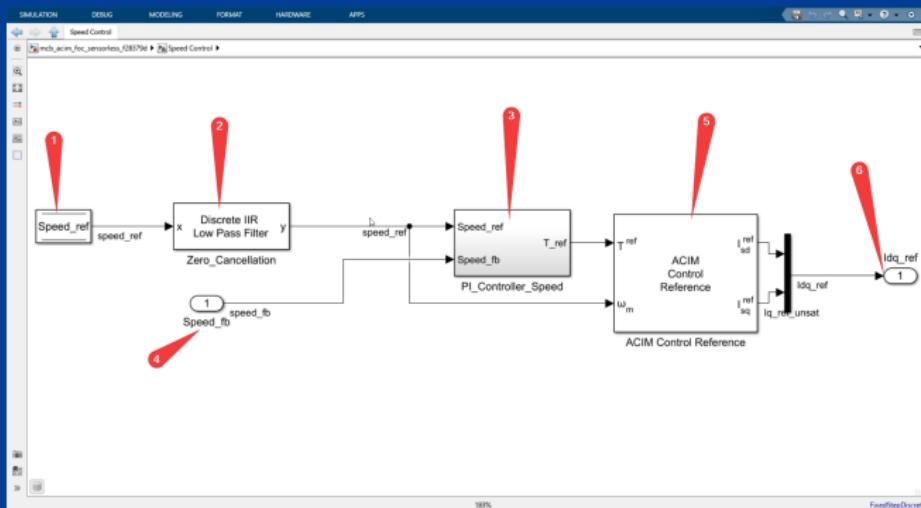
Block Diagram of Field Oriented Control



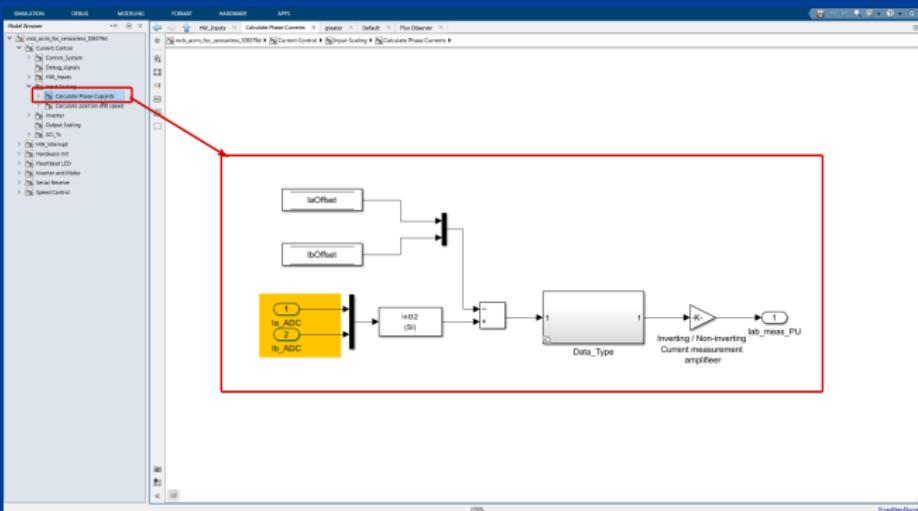
Block Diagram of the System



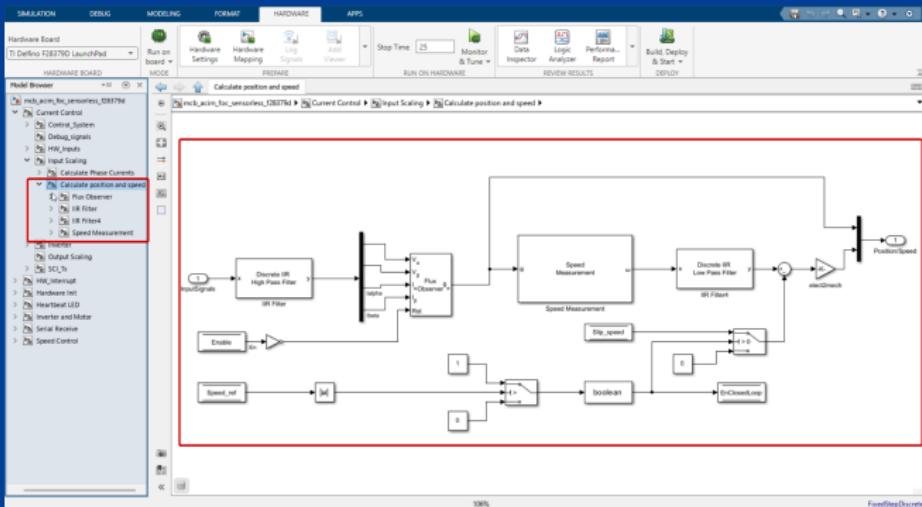
Speed Control Subsystem



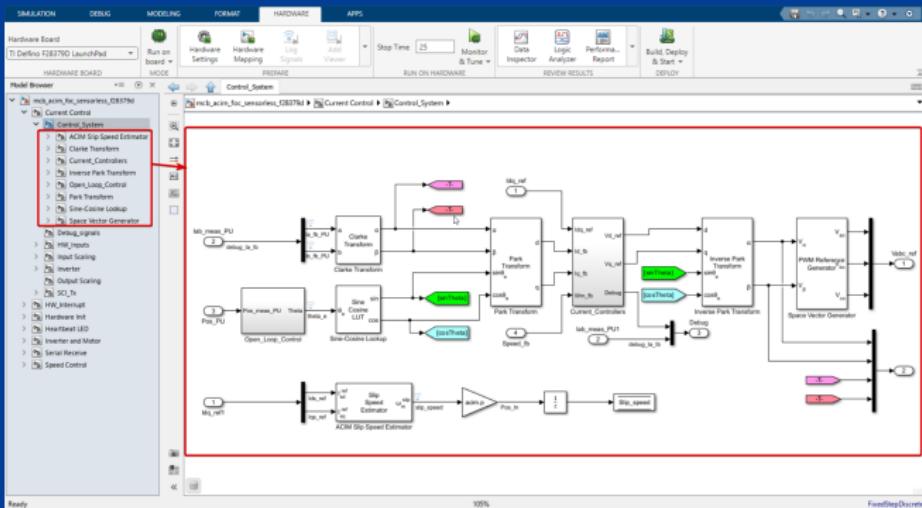
Current Measurement



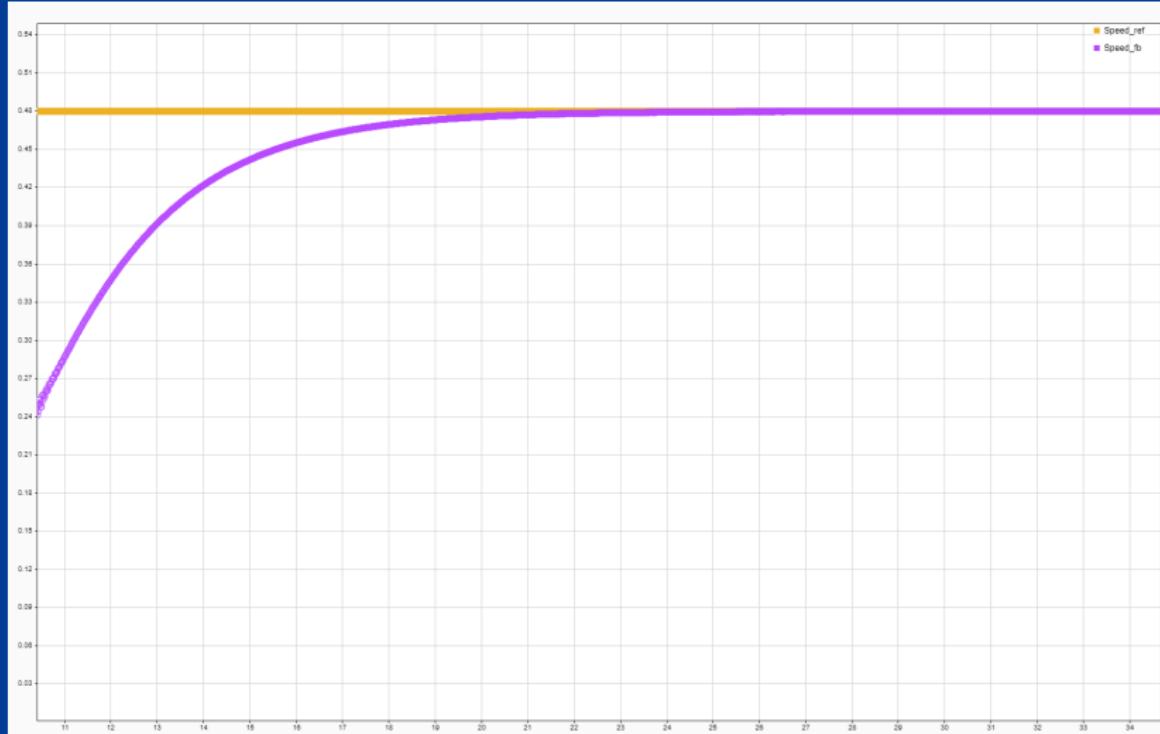
Position and Speed Estimation



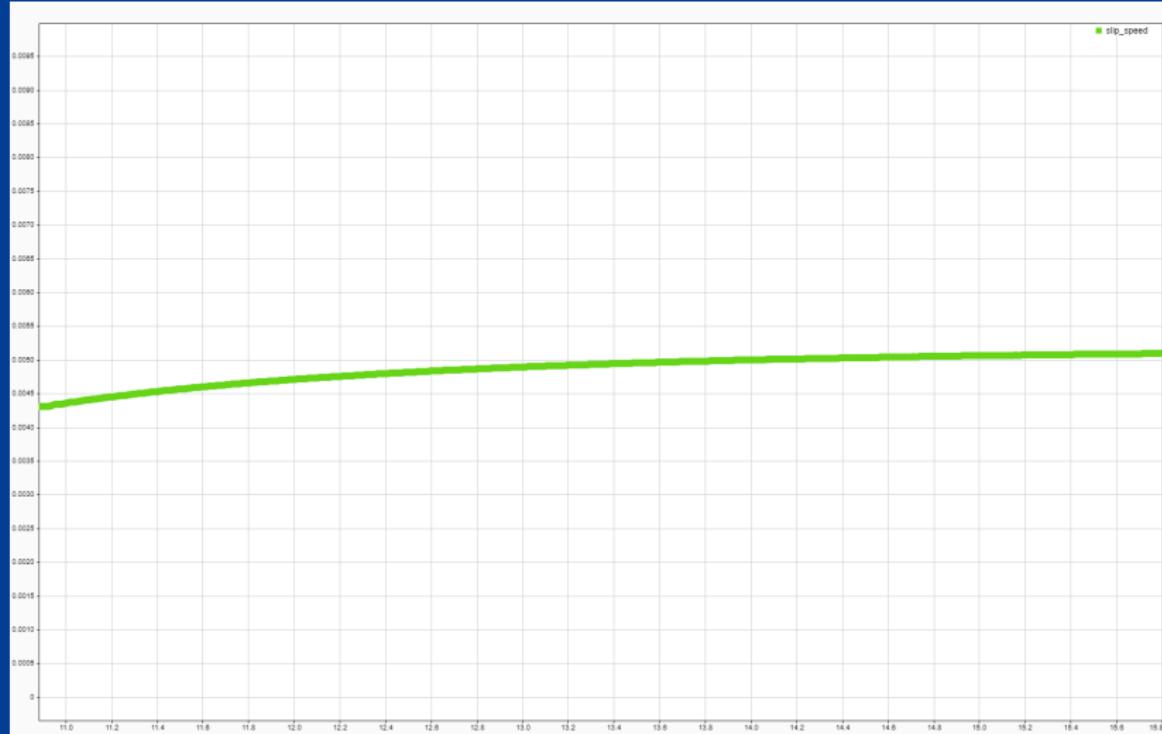
Current Control System



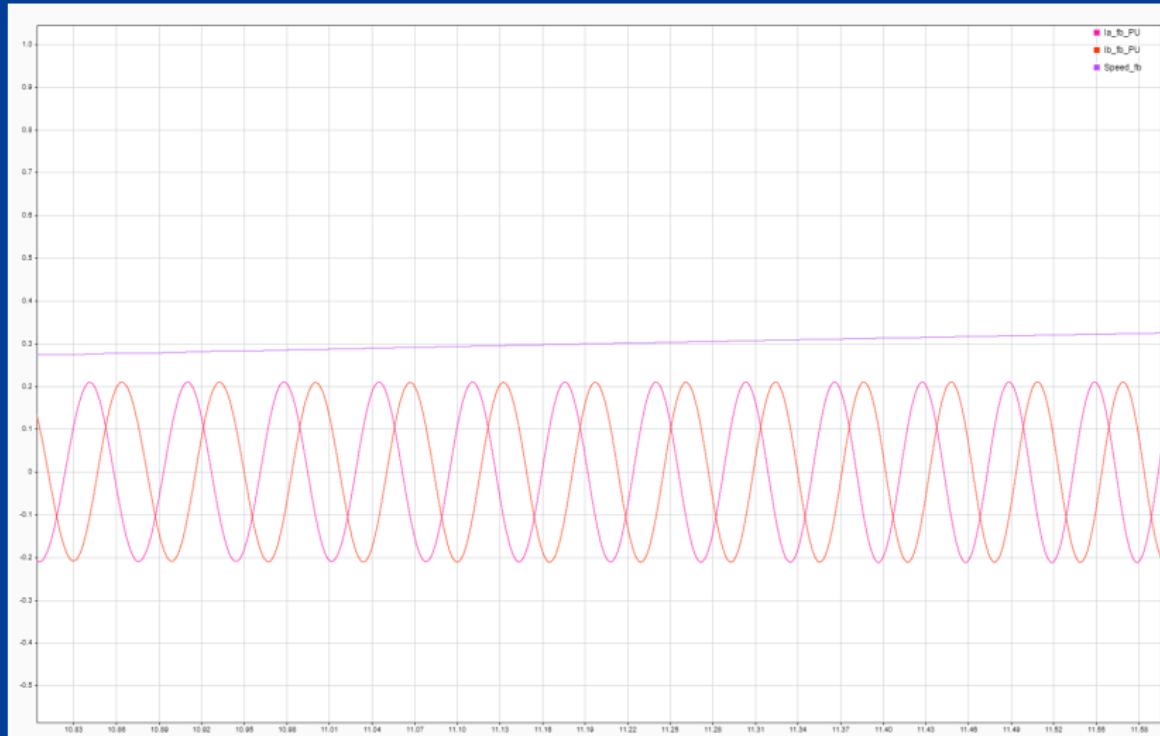
Speed Response



Slip Speed



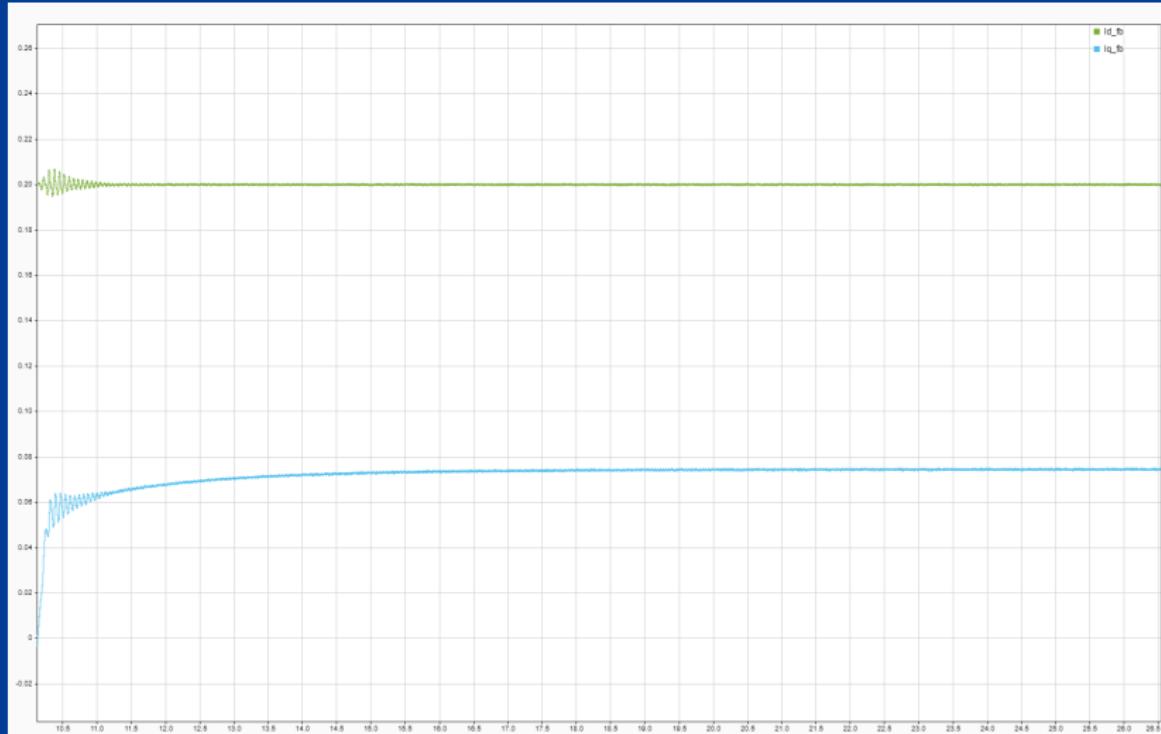
Ia and Ib Feedback/Measured Currents



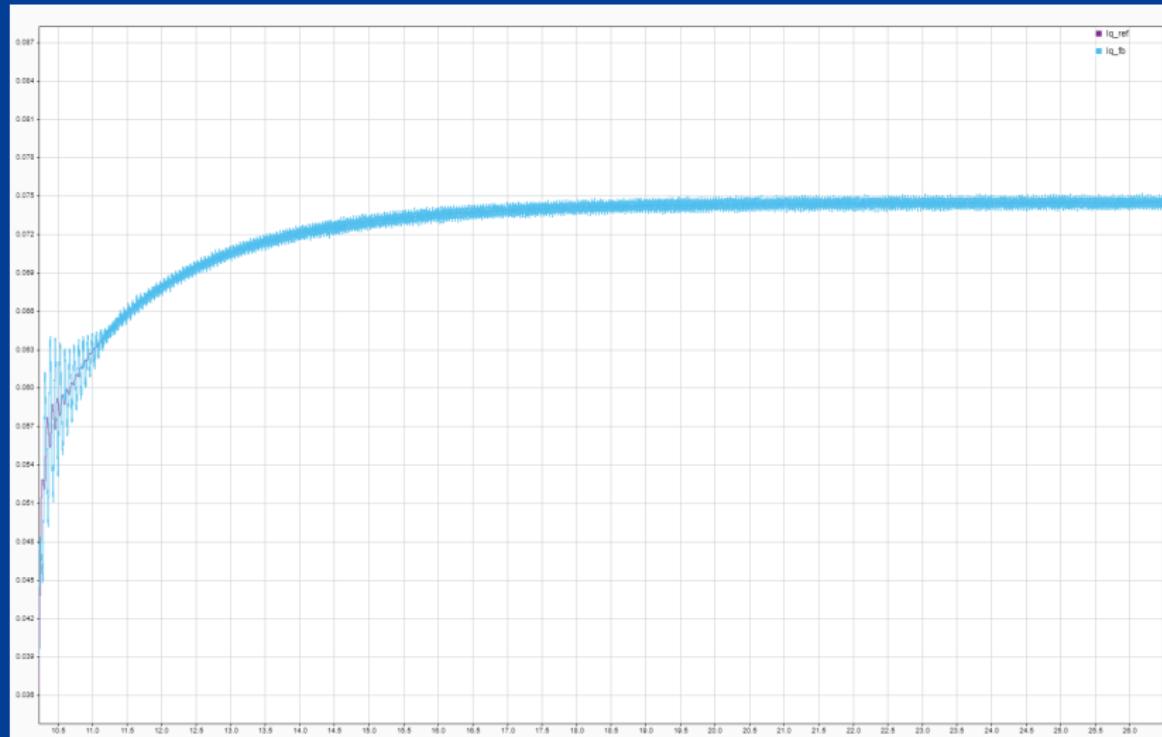
Id and Iq Reference Currents



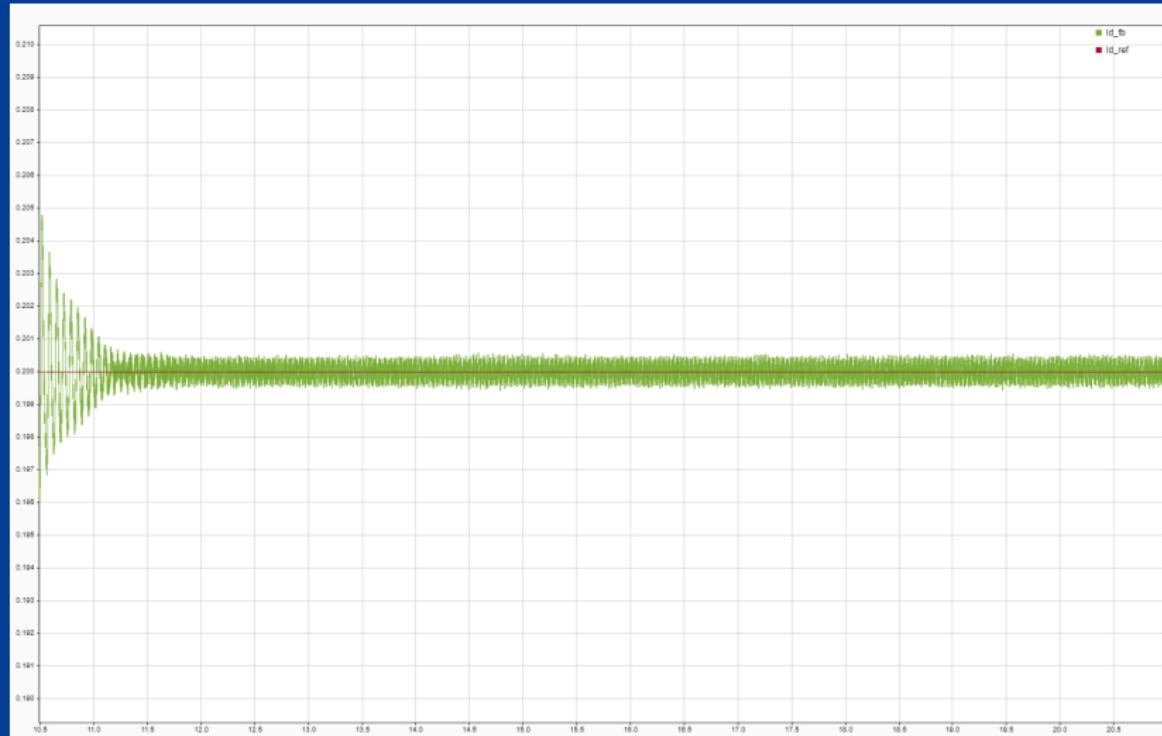
Id and Iq Feedback Currents



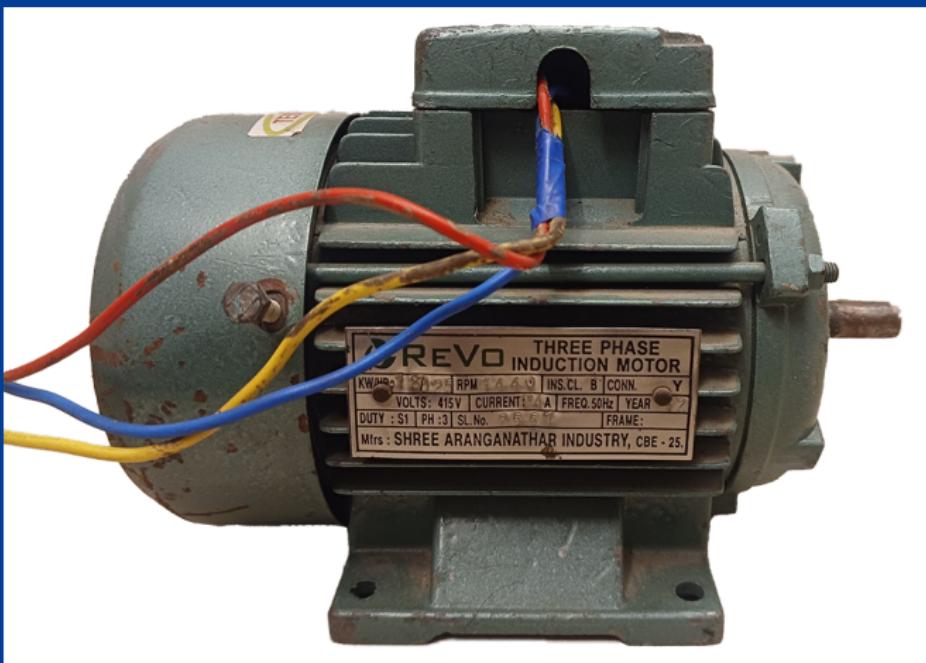
Iq Reference and Feedback Currents (Torque producing current)



Id Reference and Feedback Currents (Magnetizing current)



Induction Motor



F23879d Launchpad

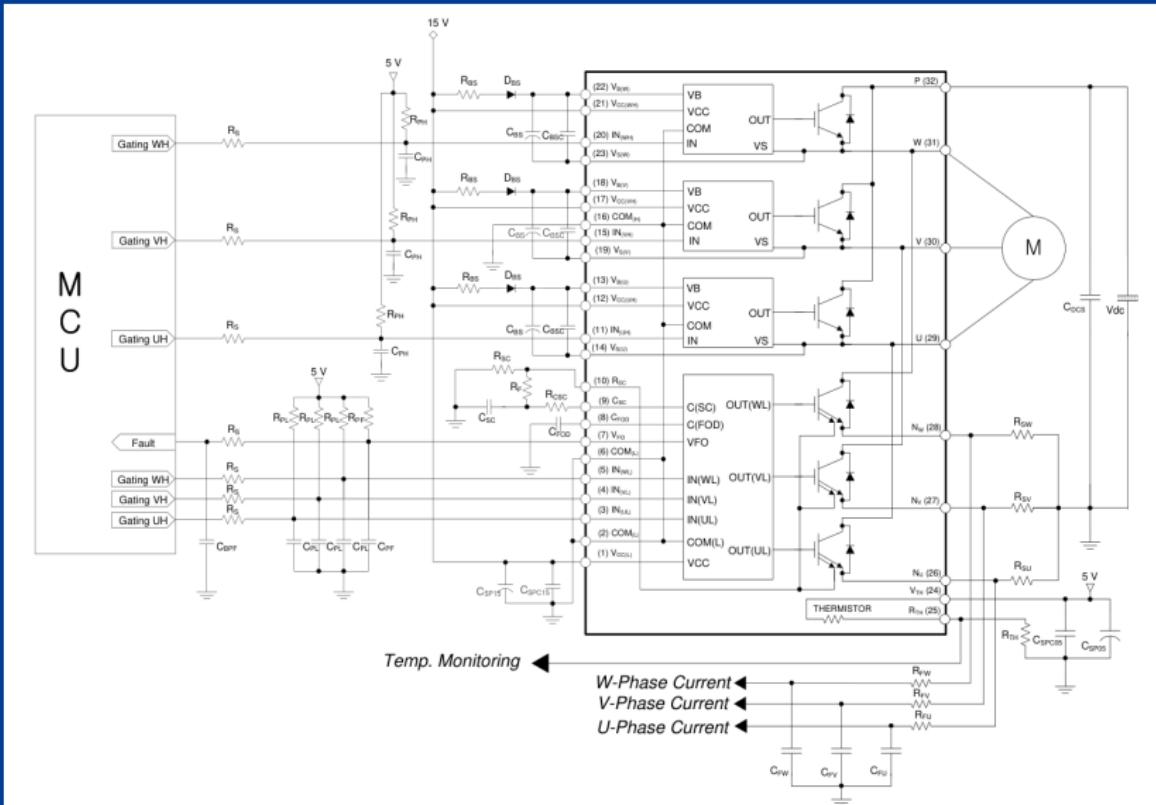


Intelligent Power Module Fsam20sh60a

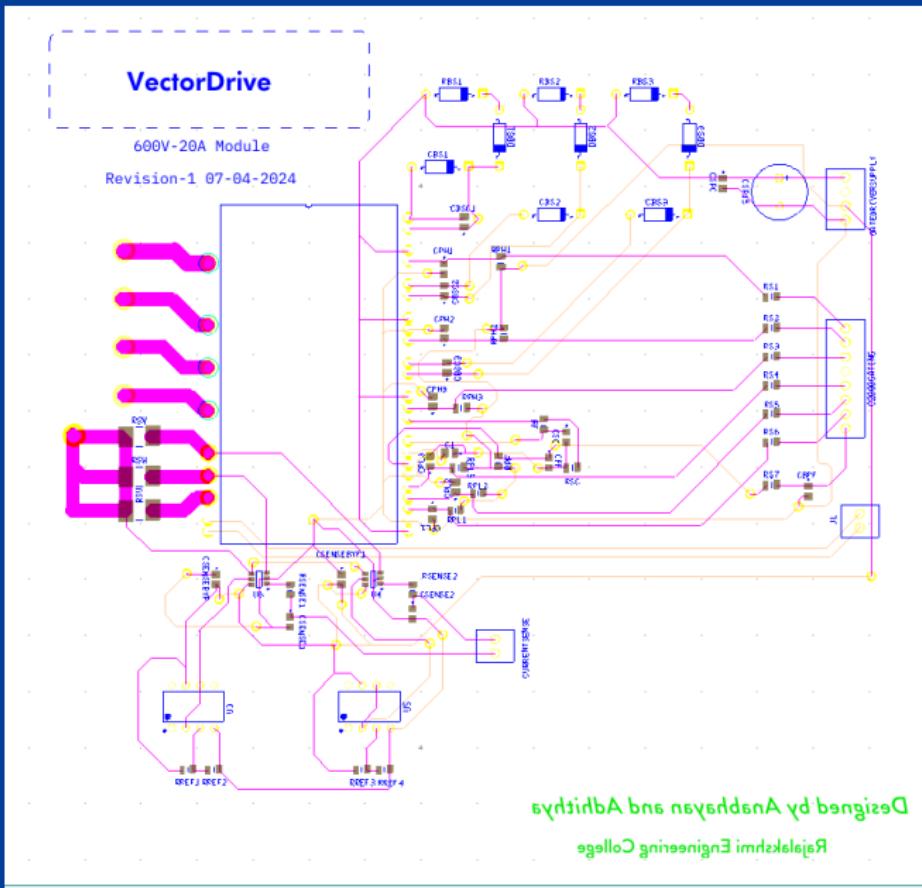


Figure 1. Package Overview

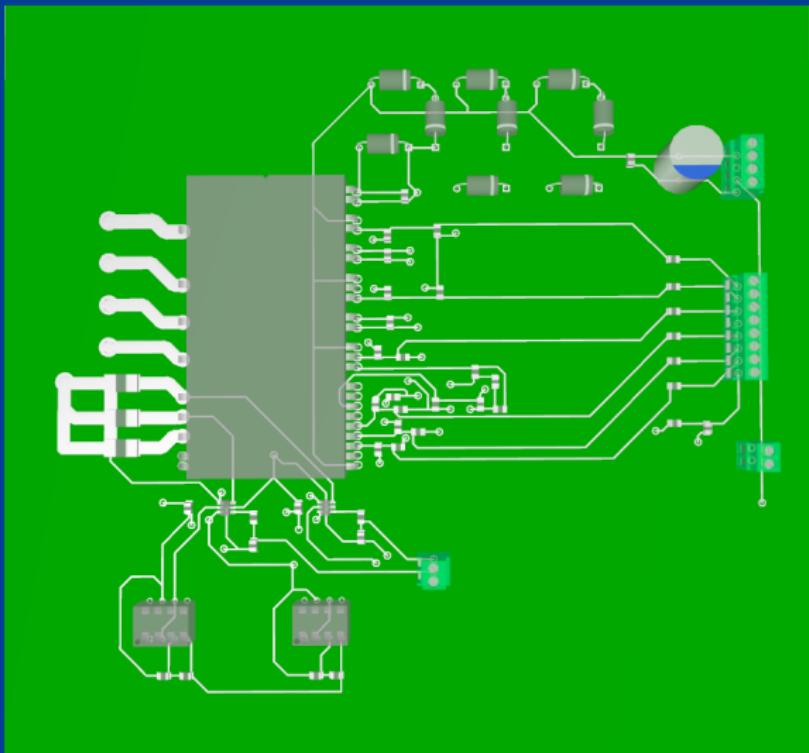
Pcb Design



PCB Layout Design



3D View of PCB Layout



Current Measurement

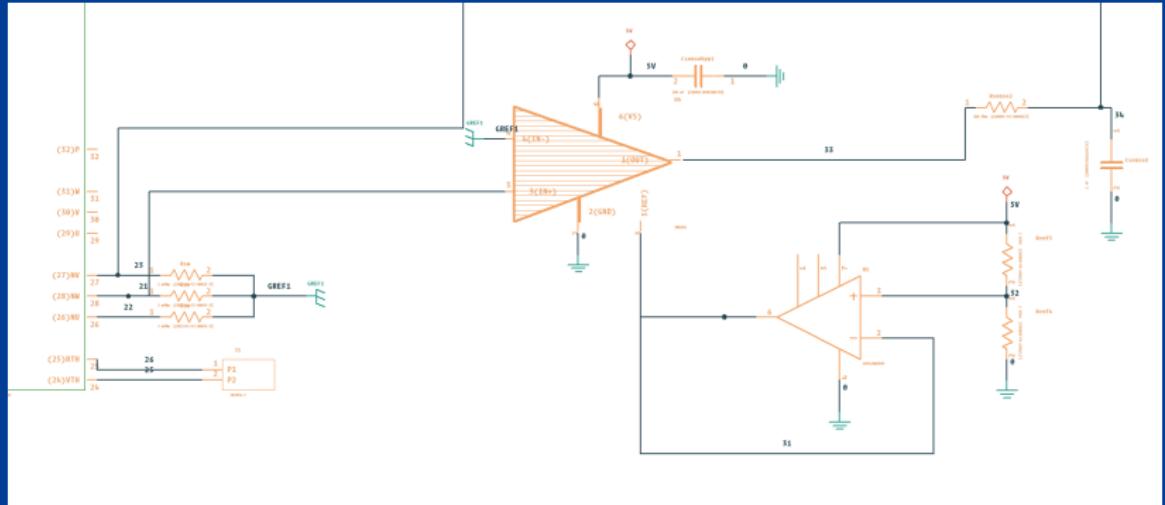


Figure: Current Sensing Circuit in Multisim (one phase shown)

ACIM Parameter Estimation: No-Load Test

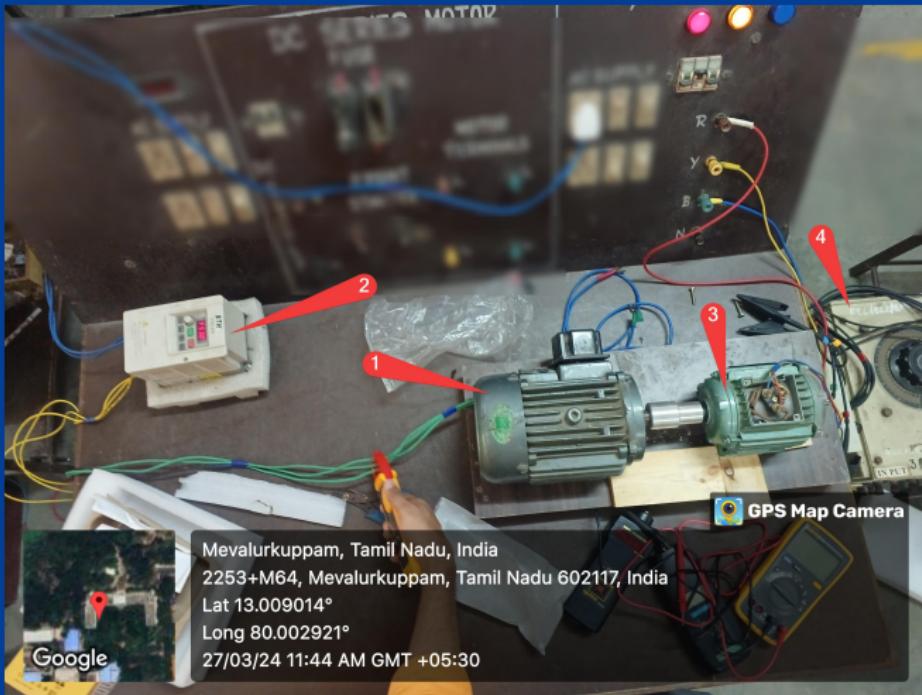


Figure: No-load test setup

Fluke 434 Power Analyzer



Figure: Fluke 434 power analyzer

No-load Test Circuit

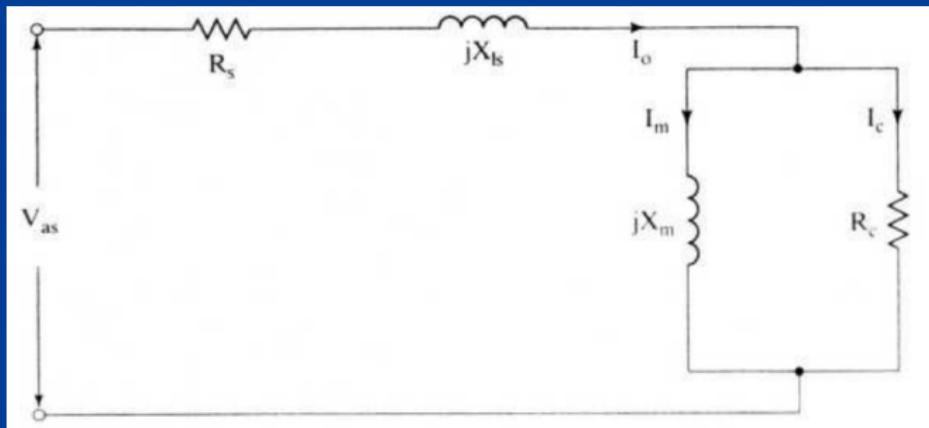


Figure: No-load test circuit

ACIM Parameter Estimation: Blocked Rotor Test

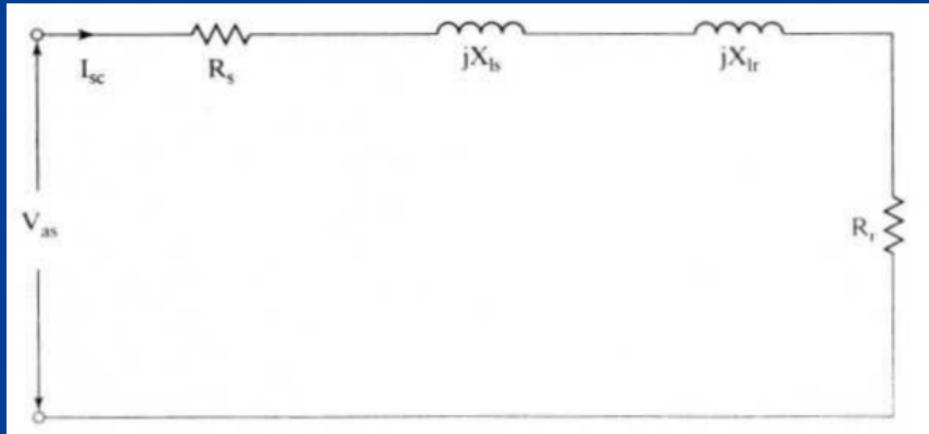


Figure: Blocked rotor test circuit

Space Vector Pulse Width Modulation



Figure: ePWM block in Simulink

ePWM Configuration

Block Parameters: ePWM

ePWM Type 1-4 (mask) (link)

Configures the Type 1 to Type 4 enhanced Pulse Width Modulator (ePWM) to generate PWM waveforms. The number of available ePWM modules (ePWM1-ePWM16) vary between C2000 processors.

General ePWMA ePWMB Counter Compare Deadband unit Event Trigger HRPWM PWM chopper control

Module: ePWM1

ePWMLink TBPRD Not Linked

Timer period units: Clock cycles

Specify timer period via: Specify via dialog

Timer period: 6667

Reload for time base period register (PRDLD): Counter equals to zero

Counting mode: Up-Down

Synchronization action: Disable

Specify software synchronization via input port (SWFSYNC)

Enable digital compare A event1 synchronization (DCAEVT1)

Enable digital compare B event1 synchronization (DCBEVT1)

Synchronization output (SYNCO): Counter equals to zero (CTR=Zero)

Peripheral synchronization event (PWMSYNCSEL): Counter equals to period (CTR=PRD)

Time base clock (TBCLK) prescaler divider: 1

High speed time base clock (HSPCLKDIV) prescaler divider: 1

Enable swap module A and B

SVPWM with Low Pass Filter

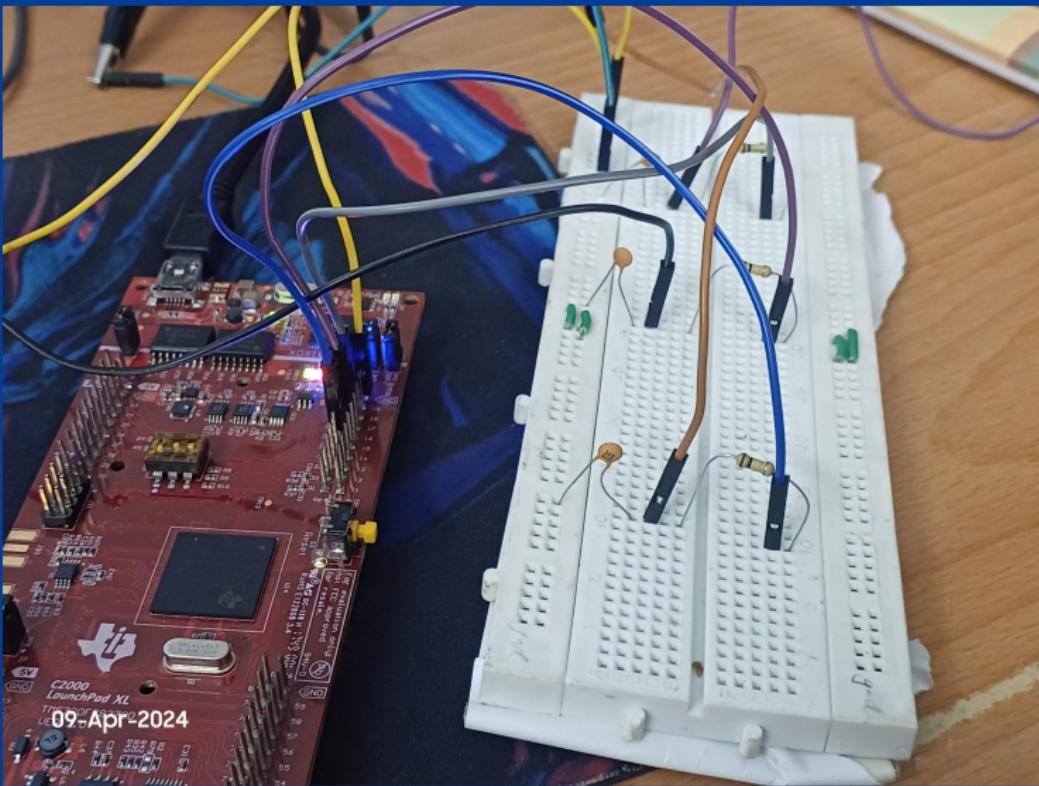


Figure: Hardware setup with RC filter and Launchpad

Output of SVPWM with LPF

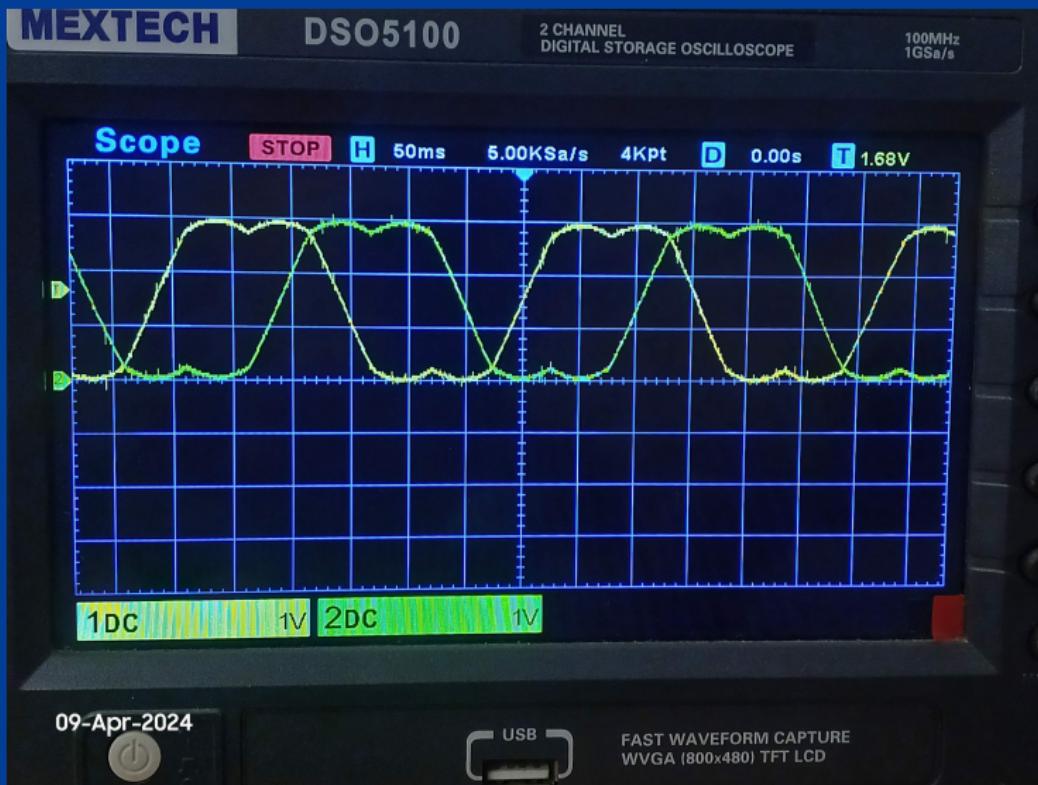


Figure: Output of SVPWM with low pass filter

Dead Band Implementation

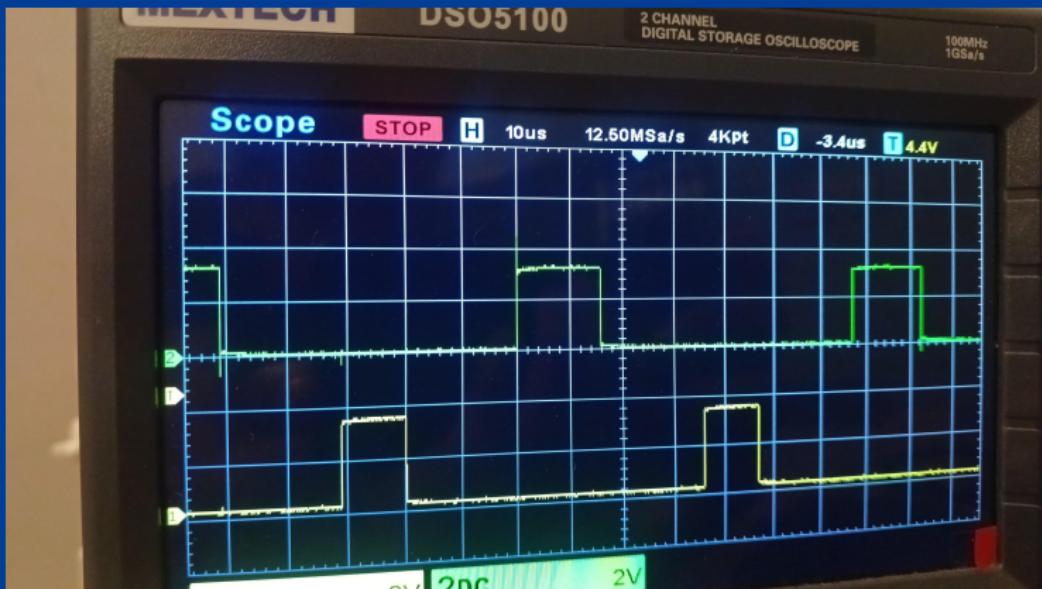


Figure: Dead band time

Conclusion