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Question Paper Code : 10295

M.C.A. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Elective

(Bridge Course)

BX 4003 — INTRODUCTION TO COMPUTER ORGANIZATION AND OPERATING SYSTEMS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Which operations can isolate a field in a word?

   (a) AND

   (b) A shift left followed by a shift right. Illustrate with examples.

2. For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, and i are given and could be considered 32-bit integers as declared in a C program. Use a minimal number of MIPS assembly instructions. f = g+ (h–5);

3. When does overflow occur during arithmetic operation? How it is handled?

4. What do you mean by data hazard and control hazard?

5. How many 32-bit integers can be stored in a 16-byte cache block?

6. Why RD and WR signal is bidirectional in DMA controller?

7. Can we have more than one ready queue? Why it is necessary to have more than one queue?

8. "The evolution of OSs has resulted in the present state in which most modern OSs are virtual machine OSs". – Comment on this statement.

9. What is a Thread?

10. How does the use of preemption and priority levels affect the behavior and the performance of CPU scheduling algorithms?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Implement the following C code in MIPS assembly. What is the total numbers of MIPS instructions needed to execute the function?

```
int fib(int n) {
    if (n==0)
        return 0;
    else if (n == 1)
        return 1;
    else
        return fib(n–1) + fib(n–2);
```

(ii) Explain division algorithm with the given numbers 7 and 2(7/2)?

Or

(b) Explain floating point addition algorithm with a flowchart by adding the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ in binary.

12. (a) Explain the memory hierarchy n detail. For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31–10	9–5	4–0

What is the cache block size (in words)?

How many entries does the cache have?

What is the ratio between total bits required for such a cache implementation over the data storage bits?

Or

(b) Explain 5 stage pipeline in explain. Examine how data dependences affect execution in the basic 5-stage pipeline for the following sequence of instructions;

or r1,r2,r3

or r2,r1,r4

or r1,r1,r2

Also, assume the following cycle times for each of the options related to forwarding:

13. (a) Discuss in detail the mapping procedures during the organization of cache memory.

Or

(b) Explain DMA controller in detail.

14. (a) Explain the seven-state model of a process and also explain the queuing diagram for the same. Is it possible to have the more than one blocked queue, if so can a process reside in more than one queue?

Or

(b) Consider the various definitions of OS and discuss each of them.

Discuss the essential properties of the following types of OS.

(i) Batch (ii) Real time

(iii) Time sharing

15. (a) Consider the following three processes that arrive in a system at the specified times, along with the duration of their CPU bursts. Process P1 arrives at time t=0, and has a CPU burst of 10 time units. P2 arrives at t=2, and has a CPU burst of 2 units. P3 arrives at t=3, and has a CPU burst of 3 units. Assume that the processes execute only once for the duration of their CPU burst, and terminate immediately. Calculate the time of completion of the three processes under each of the following scheduling policies. For each policy, you must state the completion time of all three processes, P1, P2, and P3. Assume there are no other processes in the scheduler's queue. For the preemptive policies, assume that a running process can be immediately preempted as soon as the new process arrives (if the policy should decide to premempt. (i) Shortest Job First (non-preemptive) (ii) Shortest Remaining Time First(preemptive) (iii) Round robin (preemptive) with a time slice of (atmost) 5 units per process.

Or

(b) State and explain process synchronization. Also explain the algorithm and the importance of Dekker's algorithm and dining philosophers' problem.

PART C — (1 × 15 = 15 marks)

16. (a) What are hazards. Explain various hazards using suitable illustrative examples. Also Explain how pipeline hazards are handled with proper illustrations.

Or

(b) Differentiate short term and long term scheduling. The following table shows the list of processes and their associated running times. All of the processes arrive in numerical order at time 0.

Process ID	CPU Running Time
Process 1	6
Process 2	1
Process 3	2
Process 4	4
Process 5	3

Show the scheduling order for these processes under First-In-First-Out (FIFO), Shortest-Job First (SJF), and Round-Robin (RR) scheduling with a timeslice quantum = 1 time unit.