Adhithyavaradhan

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OBJECTIVE

Aspiring RTL Design Engineer with strong hands-on experience in finite state machine (FSM) based control logic, timing-aware digital design, RTL simulation, and FPGA implementation. Seeking entry-level opportunities to contribute to front-end chip design, synthesis and timing analysis, and functional verification in semiconductor product development teams.

TECHNICAL SKILLS

HDL & RTL Design: Verilog HDL, SystemVerilog (RTL), synthesizable coding practices, modular and parameterized RTL design, FSM (Mealy/Moore), clean reset handling

Digital Logic Design: Combinational and sequential logic, FSM modeling, state transition analysis, datapath and control-path separation

Timing & Clocking: Synthesis & Timing (basic), setup and hold time concepts, critical path identification, timing-aware RTL coding, synchronous and asynchronous reset architectures

Clock Domain Crossing: CDC fundamentals, two-flop synchronizers, metastability awareness, safe data transfer techniques

Interfaces & Control: Handshake-based data transfer (valid–ready), control logic design for reliable communication

Verification & Debugging: RTL Simulation, Verilog Testbench development, waveform-based debugging using Xilinx Vivado

FPGA & Tools: FPGA implementation flow, Xilinx Vivado, ISE Design Suite, ModelSim/Questa, Linux

ACADEMIC PROJECTS

FSM-Based Handshake Data Transfer Controller Designed a finite state machine controlled data transfer module using valid–ready handshake to ensure reliable and timing-safe communication between producer and consumer blocks. Implemented fully synthesizable Verilog RTL using Mealy/Moore FSM styles with synchronous reset and glitch-free control signals. Verified functional correctness through RTL simulation and Verilog testbench execution using Xilinx Vivado.

Asynchronous FIFO with Clock Domain Crossing Designed and implemented a dual-clock asynchronous FIFO architecture to safely transfer data between independent clock domains. Used Gray-code based read/write pointers and two-flop synchronizers to prevent metastability and ensure correct full/empty flag generation. Validated CDC behavior, timing conditions, and data integrity through extensive RTL simulation.

Parameterized Pipelined ALU Developed a parameterized pipelined ALU supporting arithmetic and logical operations with configurable data width. Introduced pipeline stages to break long combinational paths and improve achievable clock frequency. Performed basic synthesis and timing analysis and verified correct operation using RTL simulation.

EDUCATION

B.E. Electronics and Communication Engineering 2022 – 2026 (Pursuing)
Erode Sengunthar Engineering College
CGPA: 7.5

AREA OF INTEREST

Digital Design & RTL Development
FSM and Timing-Critical Logic