CMOS Inverter Characterization Report

[Your Name]Roll No: 230616Technology: 45nm CMOSVDD: 1.8V

July 3, 2025

1 Objective

To design and characterize a CMOS inverter using Cadence Virtuoso. The project includes analysis of voltage transfer characteristics (VTC), noise margins, propagation delays, rise/fall times, and dynamic power.

2 Technology and Simulation Details

The CMOS inverter is designed using the Cadence Virtuoso environment with 45nm technology node. The following setup was used:

- **PDK Used:** GPDK045v5
- **Library:** analogLib
- **Simulation Tool:** ADE L
- **Waveform Viewer:** ViVA
- **Supply Voltage (VDD):** 1.8V

Transistor Parameters

Device	Width (W)	Length (L)
NMOS	0.265 μm	0.045 μm
PMOS	0.385 μm	0.045 μm

Table 1: MOSFET Dimensions

3 Schematic and Simulation Setup

Inverter Schematic

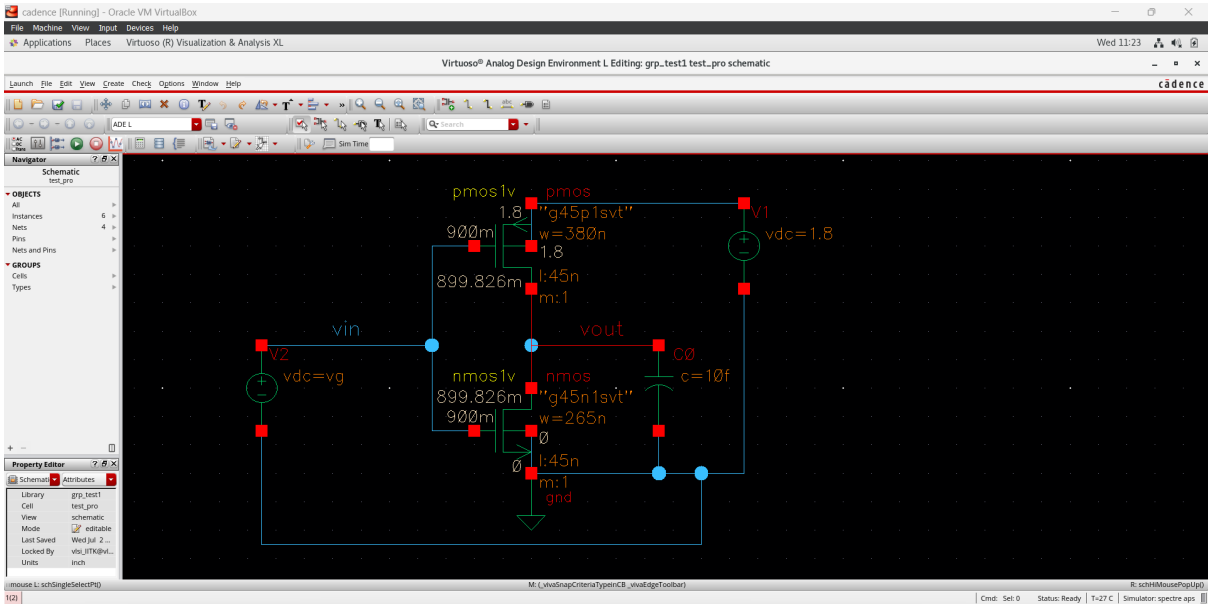

Figure 1: CMOS Inverter Schematic in Virtuoso

ADE Setup

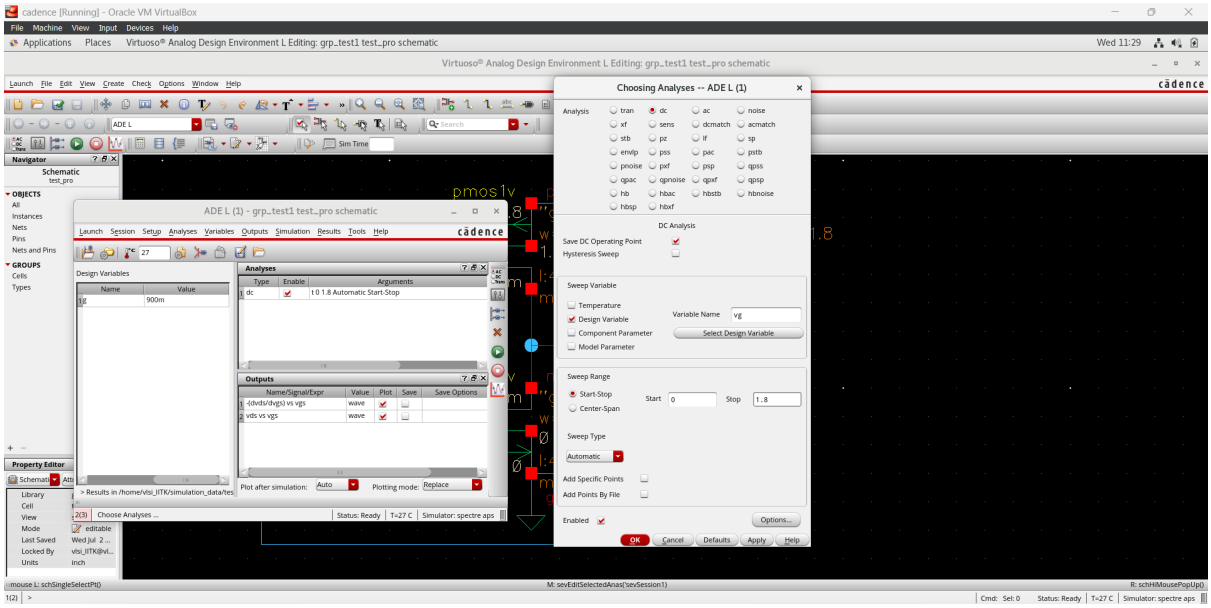

Figure 2: Simulation Setup in ADE

4 Voltage Transfer Characteristics (VTC)

VTC Plot

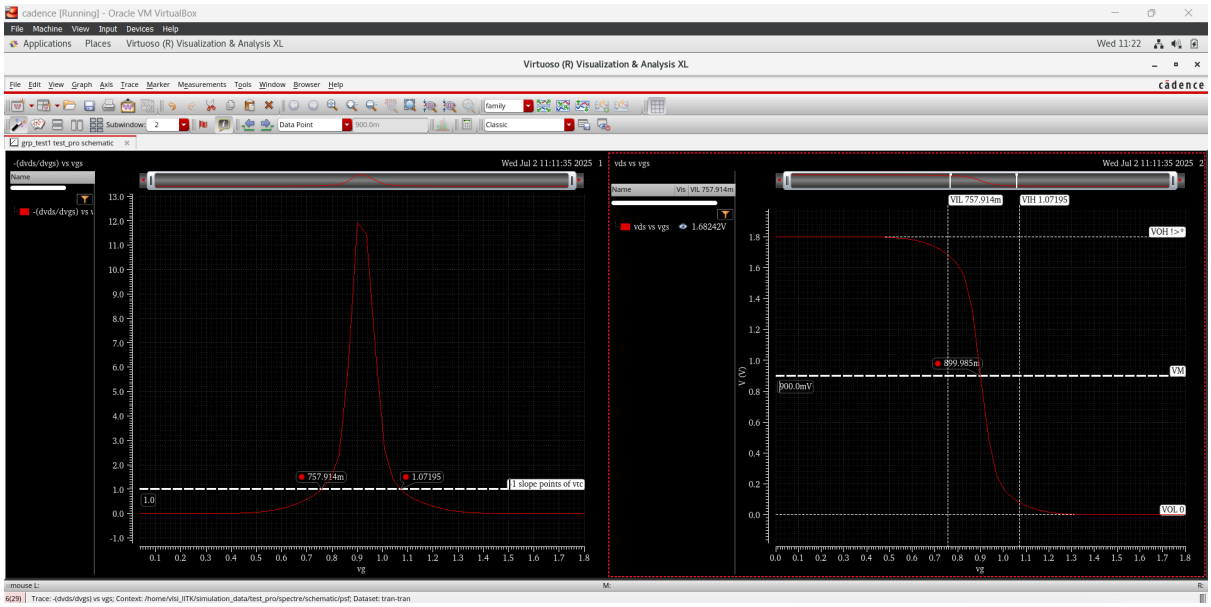

Figure 3: Voltage Transfer Characteristics (VTC)

Extracted VTC Parameters

Parameter	Value (V)
VOH	1.8
VOL	0.0
VM	0.9
VIL	0.758
VIH	1.072

Table 2: VTC Measurements

Noise Margins

Margin	Value (V)
Noise Margin High (NMH = VOH - VIH)	0.728
Noise Margin Low (NML = VIL - VOL)	0.758

Table 3: Noise Margin Values

Simulation Settings

Parameter	Value	Unit
DC Sweep Range	0 to 1.8	V
Pulse Rise Time	50	ps
Pulse Fall Time	50	ps
Pulse Width	1	ns
Pulse Period	2	ns
Total Simulation Time	6	ns
For Power Simulation Time	10	ns

Table 4: Transient and DC Simulation Parameters

5 Transient Analysis

Propagation Delay Measurement

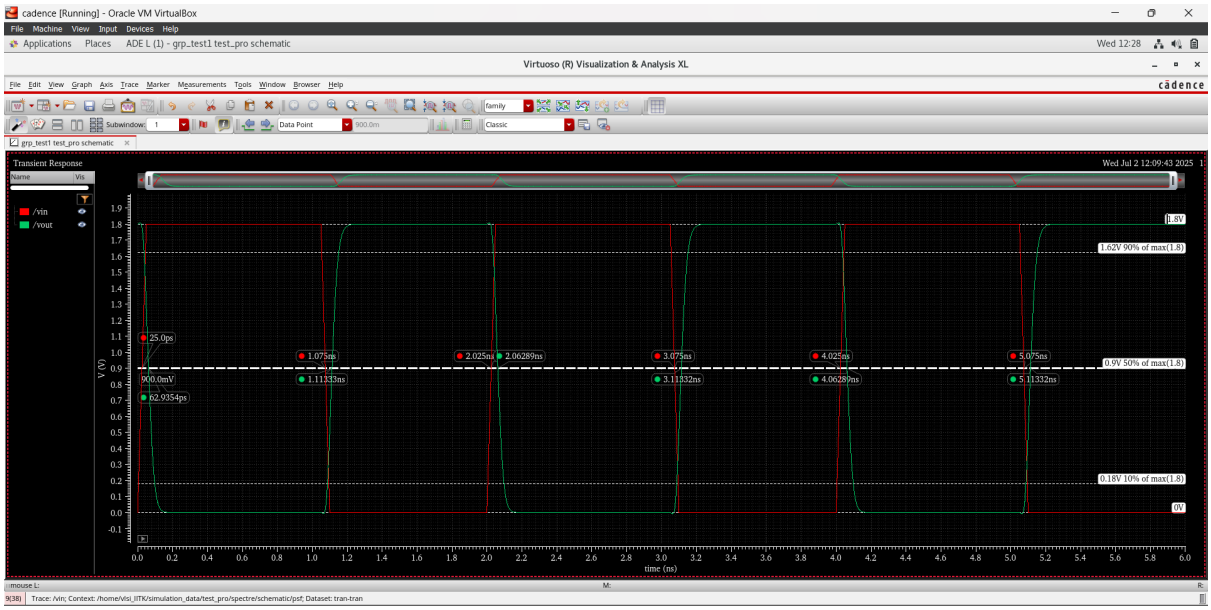

Figure 4: Measurement of tpHL and tpLH

Delay Type	Value (ns)
tpHL	0.0379
tpLH	0.0383
Average Delay (tpd)	0.0381

Table 5: Propagation Delays

Rise and Fall Time

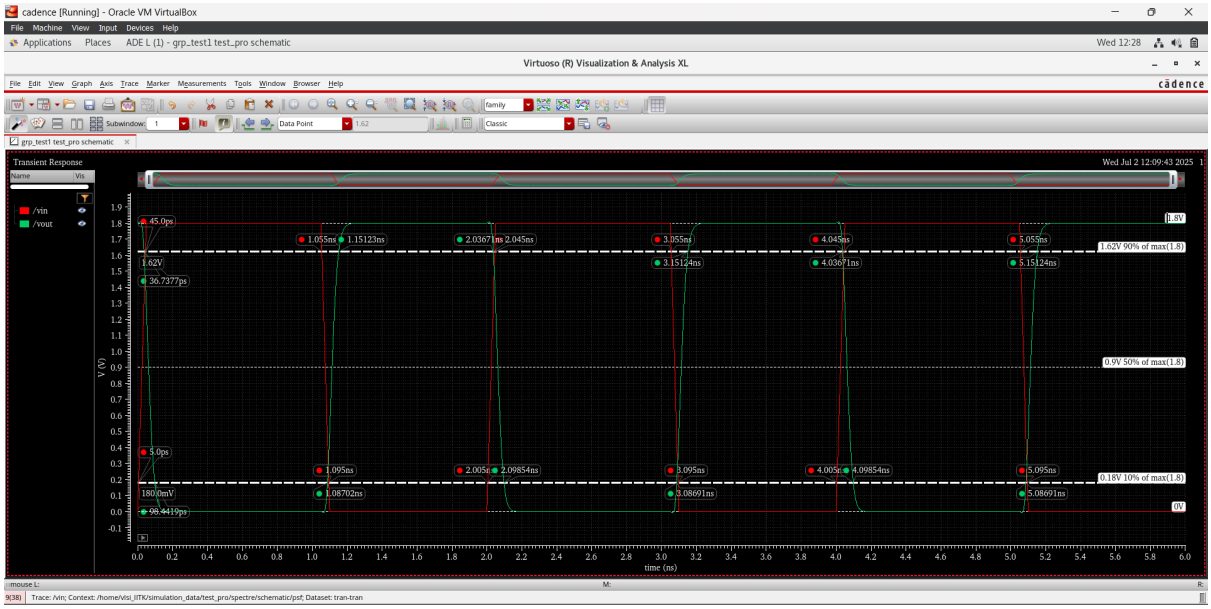

Figure 5: Rise and Fall Time Measurement

Transition	Time (ns)
Rise Time (tr)	0.0643
Fall Time (tf)	0.0618

Table 6: Rise and Fall Times

6 Dynamic Power Analysis

Instantaneous Power vs Time

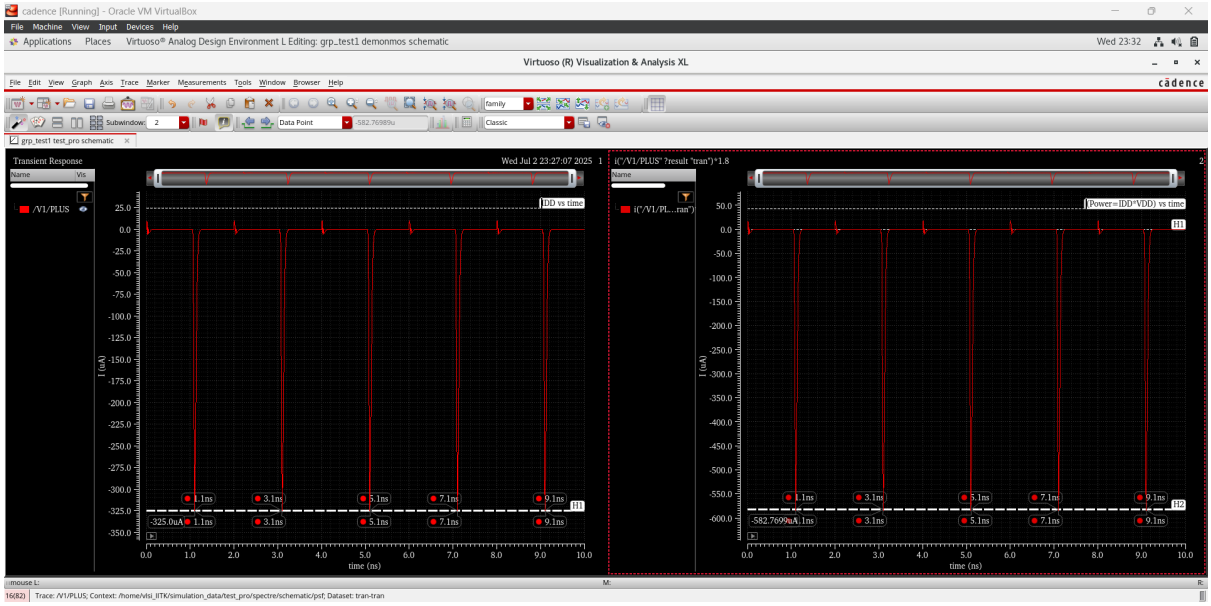

Figure 6: Power vs Time Plot

Average Power

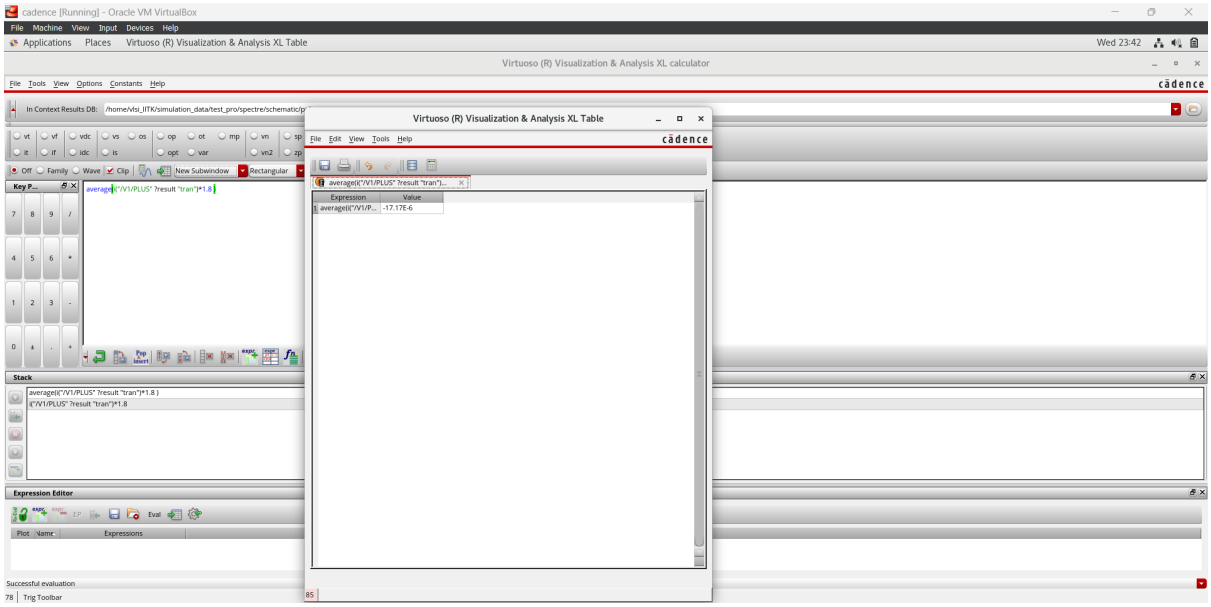

Figure 7: Average Power Calculation in ViVA

Parameter	Value
Average Dynamic Power	17.17 μW

Table 7: Dynamic Power Result

7 Conclusion

The CMOS inverter was successfully designed and simulated using Cadence Virtuoso. All key parameters were extracted and analyzed, including VTC behavior, noise margins, propagation delays, rise/fall times, and power. The results align with theoretical expectations for 45nm CMOS.