CMOS Inverter Characterization Report

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Roll Number: 230616
Technology Node: 45 nm CMOS
Supply Voltage: $V_{DD} = 1.8\,V$

1 Objective

To design and characterize a CMOS inverter using Cadence Virtuoso. The project includes analysis of voltage transfer characteristics (VTC), noise margins, propagation delays, rise/fall times, and dynamic power.

2 Technology and Simulation Details

The CMOS inverter is designed using the Cadence Virtuoso environment with 45nm technology node. The following setup was used:

- **PDK Used:** GPDK045v5
- **Library:** analogLib
- **Simulation Tool:** ADE L
- **Waveform Viewer:** ViVA
- **Supply Voltage (VDD):** 1.8V

Transistor Parameters

Device	Width (W)	Length (L)
NMOS	0.265 μm	0.045 μm
PMOS	0.385 μm	0.045 μm

Table 1: MOSFET Dimensions

3 CMOS Inverter Characterization: Procedure and Observations

In the CMOS inverter characterization project, I began by placing one PMOS and one NMOS transistor from the `gpdk45` library in the schematic. I connected the drains of

both transistors together and labeled this node as the output. The gates of both transistors were connected and set as the input. The source of the PMOS was connected to a DC voltage source of 1.8 V, while the source of the NMOS was connected to ground. Additionally, I connected a capacitor of 10 fF to the output node to simulate load conditions.

Inverter Schematic

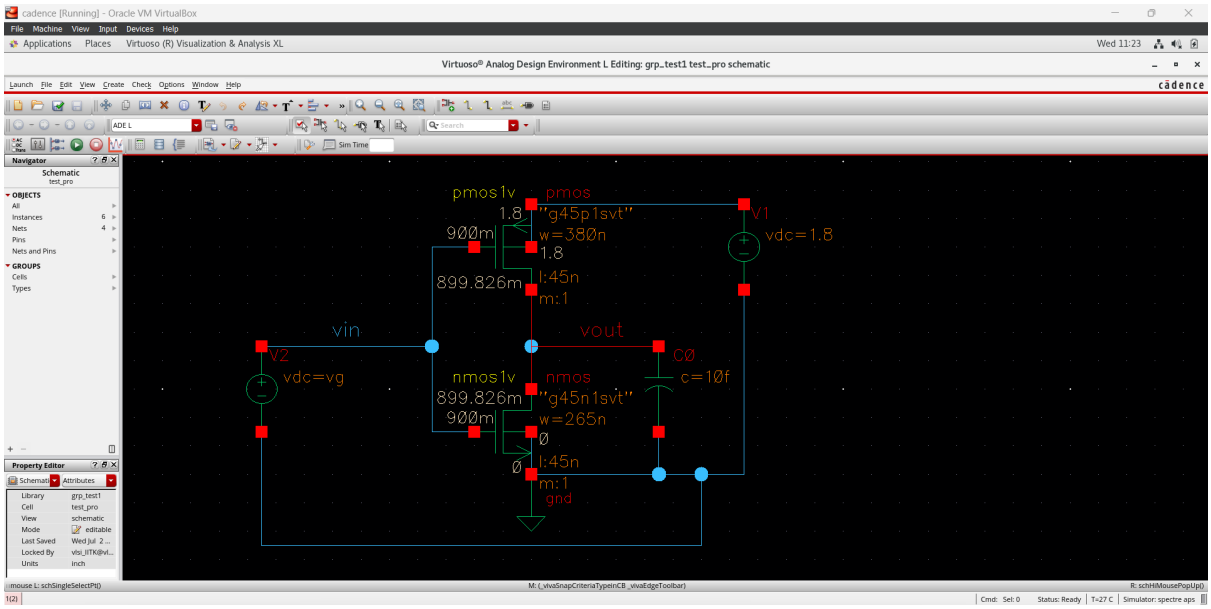

Figure 1: CMOS Inverter Schematic in Virtuoso

Step 1: Voltage Transfer Characteristics (VTC)
To find the Voltage Transfer Characteristics, I used the ADE L window to run a DC analysis. The input voltage was swept from 0 V to 1.8 V, and I observed the output voltage. Theoretically, at the logic threshold, the input and output voltages (VM) should be equal, ideally around 0.9 V for a symmetric inverter. However, on the first run, this condition was not met, and I observed an incorrect switching point — for example, input at 0.9 V produced output around 1.3 V.

To fix this, I adjusted the transistor width and length values (W/L ratios) to shift the switching threshold and match the expected VTC behavior. After tuning, the desired curve was achieved. I then marked the key points on the curve:

- VOH = 1.8 V (maximum output voltage)
- VOL = 0.0 V (minimum output voltage)
- VM = 0.9 V (switching threshold, where $V_{\text{in}} = V_{\text{out}}$)

To find VIL and VIH, I located the points on the curve where the slope was equal to -1. These were marked as the lower and higher switching thresholds, respectively. Using these values, I calculated the noise margins:

- NMH = VOH − VIH
- NML = VIL − VOL

For a robust inverter, NMH should be greater than NML. However, in my case, NML was slightly greater than NMH. Therefore, this inverter can be considered average — neither poor nor excellent — and functionally acceptable for digital logic.

ADE Setup

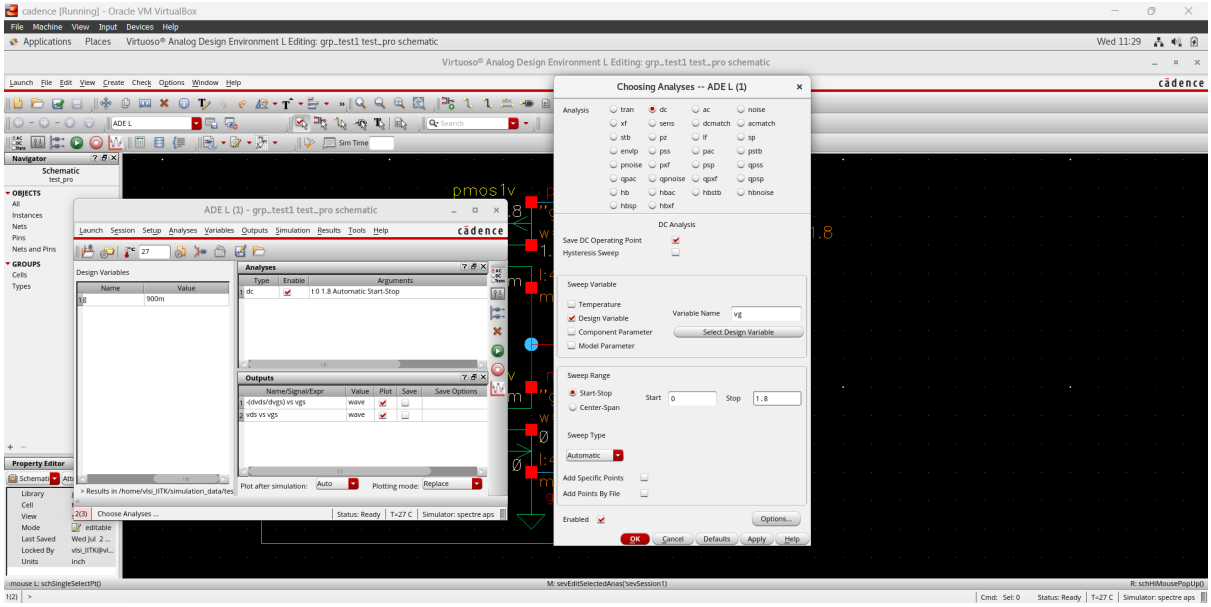

Figure 2: Simulation Setup in ADE

VTC Plot

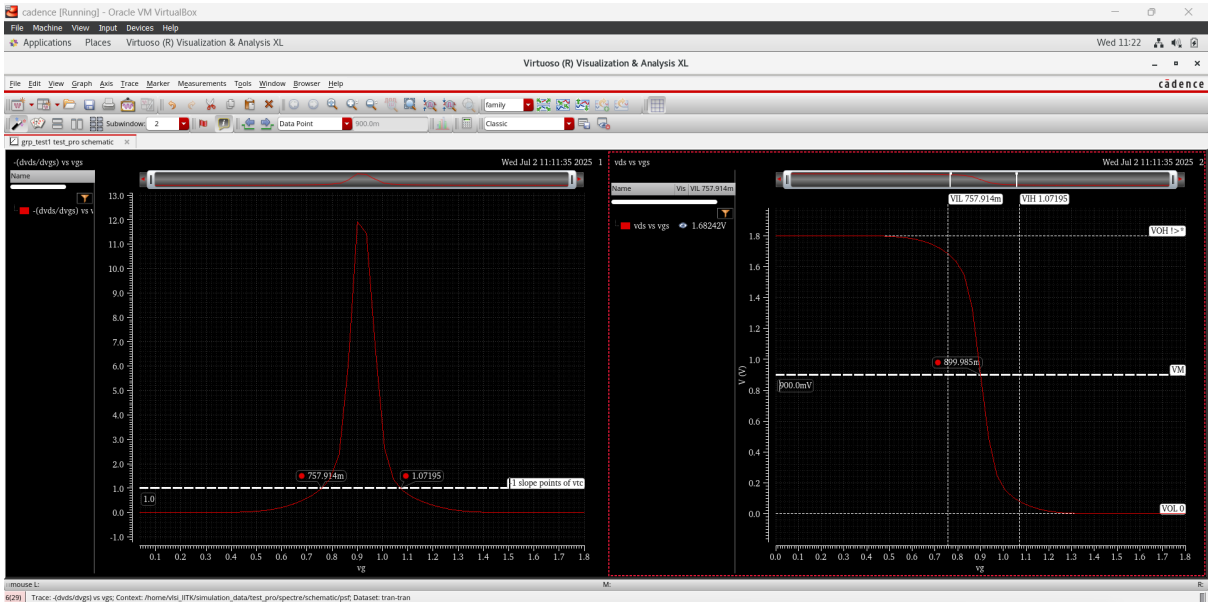

Figure 3: Voltage Transfer Characteristics (VTC)

Extracted VTC Parameters

Parameter	Value (V)
VOH	1.8
VOL	0.0
VM	0.9
VIL	0.758
VIH	1.072

Table 2: VTC Measurements

Noise Margins

Margin	Value (V)
Noise Margin High (NMH = VOH - VIH)	0.728
Noise Margin Low (NML = VIL - VOL)	0.758

Table 3: Noise Margin Values

Simulation Settings

Parameter	Value	Unit
DC Sweep Range	0 to 1.8	V
Pulse Rise Time	50	ps
Pulse Fall Time	50	ps
Pulse Width	1	ns
Pulse Period	2	ns
Total Simulation Time	6	ns
For Power Simulation Time	10	ns

Table 4: Transient and DC Simulation Parameters

Step 2: Propagation Delay, Rise Time, and Fall Time
After completing the VTC analysis, I proceeded to measure propagation delays and timing parameters. I replaced the DC input with a square pulse source, setting parameters such as frequency, delay, rise time, and fall time. Then, I performed a transient analysis with a stop time of 6 ns to capture full signal transitions.

I calculated the propagation delays as follows:

- tpHL: Time difference between the input rising and the output falling when the input crosses 50% of VDD.
- tpLH: Time difference between the input falling and the output rising under similar conditions.

Propagation Delay Measurement

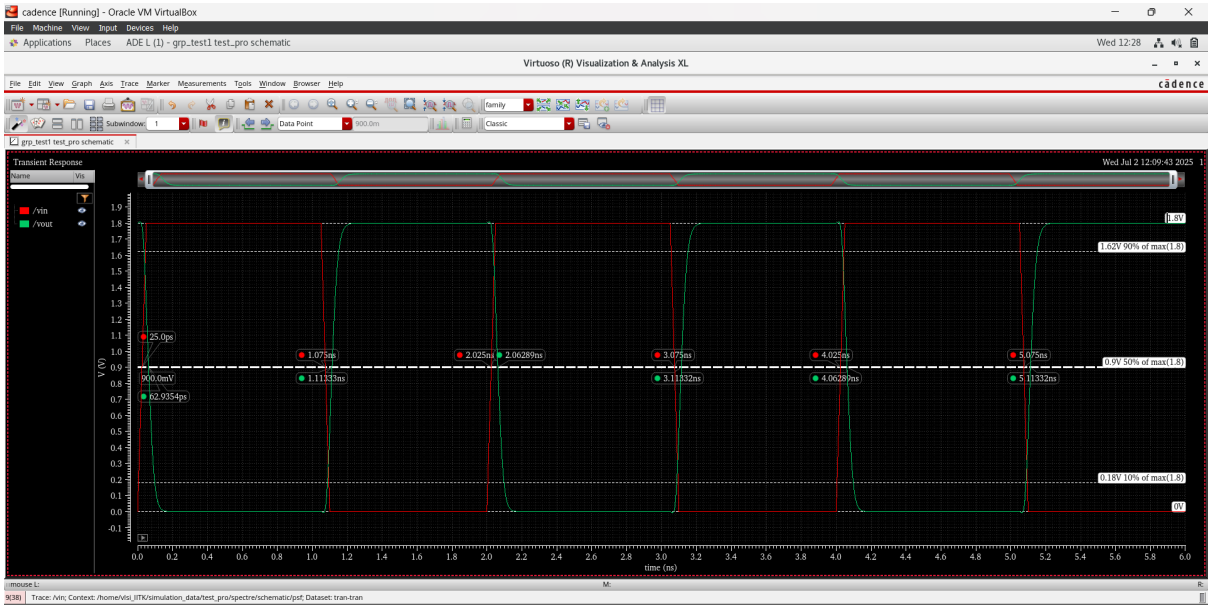

Figure 4: Measurement of tpHL and tpLH

Delay Type	Value (ns)
tpHL	0.0379
tpLH	0.0383
Average Delay (tpd)	0.0381

Table 5: Propagation Delays

I also calculated the rise and fall times of the output signal:

- Rise Time (tr): Time taken for the output to rise from 10% to 90% of its maximum value.
- Fall Time (tf): Time taken for the output to fall from 90% to 10% of its maximum value.

Rise and Fall Time

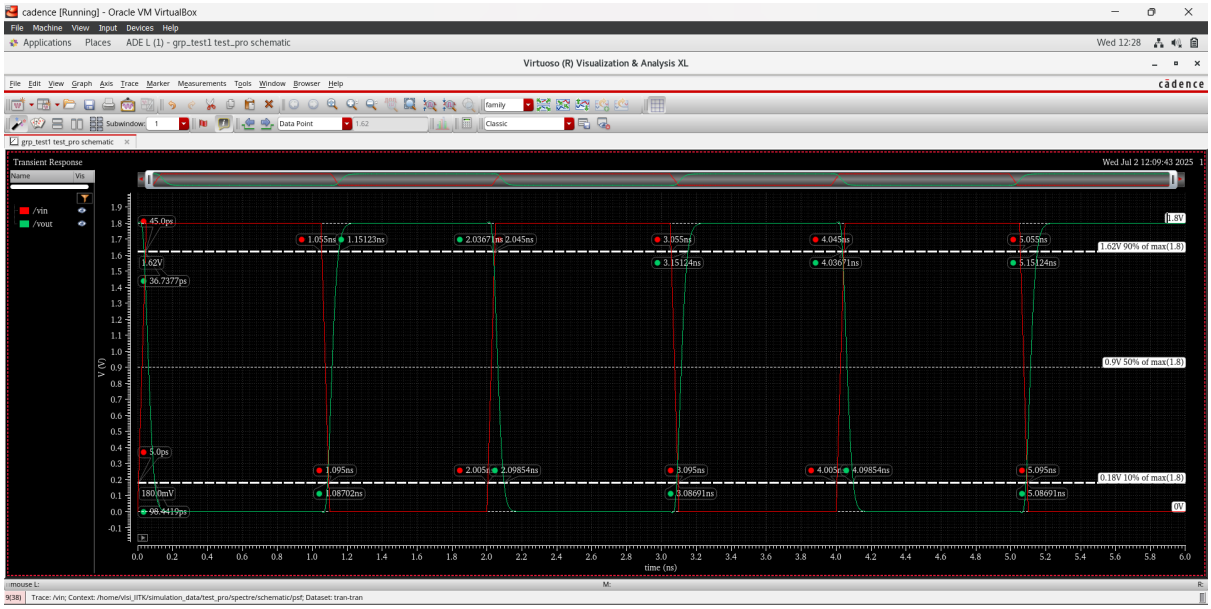

Figure 5: Rise and Fall Time Measurement

Transition	Time (ns)
Rise Time (tr)	0.0643
Fall Time (tf)	0.0618

Table 6: Rise and Fall Times

Step 3: Power Analysis

Instantaneous Power vs Time

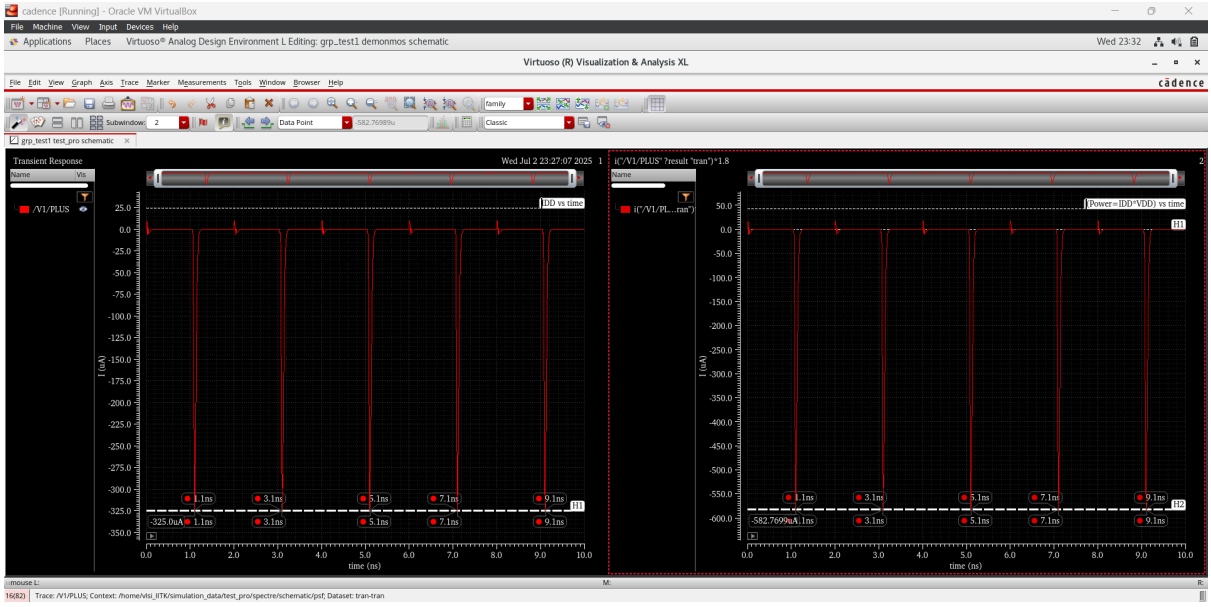

Figure 6: Power vs Time Plot

Average Power

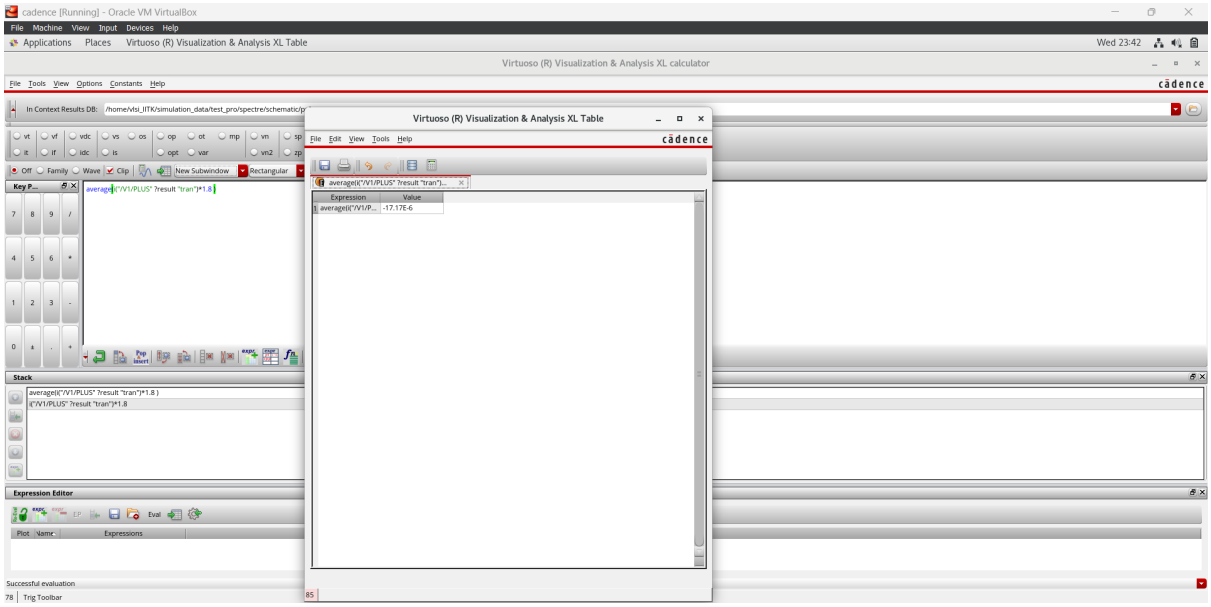

Figure 7: Average Power Calculation in ViVA

Finally, I analyzed the dynamic power consumption of the inverter. Using the same square pulse input, I plotted the instantaneous power delivered to the circuit over a 10 ns simulation time. Then, I used the ADE calculator to compute the average power consumed during switching.

Parameter	Value
Average Dynamic Power	17.17 μW

Table 7: Dynamic Power Result

4 Conclusion

The CMOS inverter was successfully designed, simulated, and characterized using Cadence Virtuoso with 45nm technology. Key performance parameters were thoroughly extracted and analyzed, including the voltage transfer characteristics (VTC), noise margins, propagation delays, rise and fall times, and dynamic power consumption. The simulation results closely matched theoretical predictions, validating the accuracy of the design and methodology.

Based on the complete analysis, it can be concluded that the designed inverter exhibits reliable switching behavior, acceptable delay performance, and reasonable power efficiency. Although the noise margins showed slight asymmetry—with the low-level margin marginally exceeding the high-level margin—the inverter remains functionally robust. Overall, it meets the fundamental criteria for use in digital logic applications and serves as a solid representation of a well-constructed CMOS inverter.