# COMPUTATIONAL PHYSICS: INCLUDES PARALLEL COMPUTING/PARALLEL PROGRAMMING

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ABSTRACT. Everything about Computational Physics, including Parallel computing/ Parallel programming.

### Part 1. Introduction

References

#### 1. Parallel Computing

- 1.1. Udacity Intro to Parallel Programming: Lesson 1 The GPU Programming Model. Owens and Luebki pound fists at the end of this video. =)))) Intro to the class.
- 1.1.1. Running CUDA locally. Also, Intro to the class, in Lesson 1 The GPU Programming Model, has  $n_{\text{vecop}} \equiv (n_{\text{vecop}} \text{wide axial vector operations}/core \text{ core})$ links to documentation for running CUDA locally; in particular, for Linux: http://docs.nvidia.com/cuda/ cuda-getting-started-guide-for-linux/index.html. That guide told me to go download the NVIDIA CUDA Toolkit, which is the https://developer.nvidia.com/cuda-downloads.

For Fedora, I chose Installer Type runfile (local).

Afterwards, installation of CUDA on Fedora 23 workstation had been nontrivial. Go see either my github repository MLgrabbag (which will be updated) or my wordpress blog (which may not be upgraded frequently).

 $P = VI = I^2R$  heating.

Date: 23 mai 2016.

Key words and phrases. Computational Physics, Parallel Computing, Parallel Programming.

1.1.2. Definitions of Latency and throughput (or bandwidth). cf. Building a Power Efficient Processor

Latency vs Bandwidth

latency [sec]. From the title "Latency vs. bandwidth", I'm thinking that throughput = bandwidth (???), throughput = job/time (of job).

13

15

Given total task, velocity v,

total task /v = latency. throughput = latency/(jobs per total task).

Also, in Building a Power Efficient Processor. Owens recommends the article David Patterson, "Latency..."

cf. GPU from the Point of View of the Developer

 $n_{\rm core} \equiv \text{number of cores}$ 

 $n_{\rm thread} \equiv {\rm threads/core} \ ({\rm hyperthreading})$ 

 $n_{\rm core} \cdot n_{\rm vecop} \cdot n_{\rm thread}$  parallelism

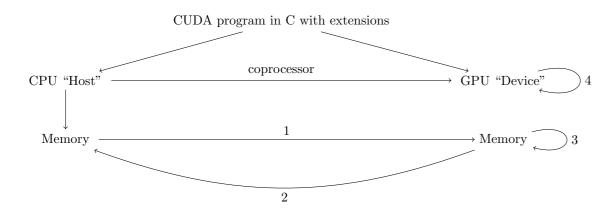
There were various websites that I looked up to try to find out the capabilities of my video card, but so far, I've only found these commands (and I'll print out the resulting output):

\$ lspci -vnn | grep VGA -A 12

03:00.0 VGA compatible controller [0300]: NVIDIA Corporation GM200 [GeForce GTX 980 Ti] [10de:17c8] (rev a1) (prog-if 00 [VC Subsystem: eVga.com. Corp. Device [3842:3994]

```
Physical Slot: 4
       Flags: bus master, fast devsel, latency 0, IRQ 50
       Memory at fa000000 (32-bit, non-prefetchable) [size=16M]
       Memory at e0000000 (64-bit, prefetchable) [size=256M]
       Memory at f0000000 (64-bit, prefetchable) [size=32M]
        I/O ports at e000 [size=128]
        [virtual] Expansion ROM at fb0000000 [disabled] [size=512K]
        Capabilities: <access denied>
        Kernel driver in use: nvidia
        Kernel modules: nouveau, nvidia
$ lspci | grep VGA -E
03:00.0 VGA compatible controller: NVIDIA Corporation GM200 [GeForce GTX 980 Ti] (rev a1)
$ grep driver /var/log/Xorg.0.log
     18.087] (WW) Hotplugging is on, devices using drivers 'kbd', 'mouse' or 'vmmouse' will be disabled
              X.Org XInput driver: 22.1
     18.192] (II) Loading /usr/lib64/xorg/modules/drivers/nvidia_drv.so
     19.088] (II) NVIDIA(GPU-0): Found DRM driver nvidia-drm (20150116)
                               ACPI event daemon is available, the NVIDIA X driver will
     19.102] (II) NVIDIA(0):
     19.174] (II) NVIDIA(0): [DRI2] VDPAU driver: nvidia
     19.284]
              ABI class: X.Org XInput driver, version 22.1
$ lspci -k | grep -A 8 VGA
03:00.0 VGA compatible controller: NVIDIA Corporation GM200 [GeForce GTX 980 Ti] (rev a1)
       Subsystem: eVga.com. Corp. Device 3994
       Kernel driver in use: nvidia
       Kernel modules: nouveau, nvidia
03:00.1 Audio device: NVIDIA Corporation GM200 High Definition Audio (rev a1)
       Subsystem: eVga.com. Corp. Device 3994
        Kernel driver in use: snd_hda_intel
        Kernel modules: snd_hda_intel
05:00.0 USB controller: VIA Technologies, Inc. VL805 USB 3.0 Host Controller (rev 01)
```

# CUDA Program Diagram



CPU "host" is the boss (and issues commands) -Owen. Coprocessor: CPU "host"  $\rightarrow$  GPU "device"

Coprocessor: CPU process  $\mapsto$  (co)-process out to GPU

With

1 data cpu  $\rightarrow$  gpu

```
2 data gpu \rightarrow cpu
                            (initiated by cpu host)
```

1., 2., uses cudaMemcpy

3 allocate GPU memory: cudaMalloc

4 launch kernel on GPU

Remember that for 4., this launching of the kernel, while it's acting on GPU "device" onto itself, it's initiated by the boss, the CPU "host".

Hence, cf. Quiz: What Can GPU Do in CUDA, GPUs can respond to CPU request to receive and send Data CPU  $\rightarrow$  GPU and Data GPU  $\rightarrow$  CPU, respectively (1,2, respectively), and compute a kernel launched by the CPU (3).

A CUDA Program A typical GPU program

- cudaMalloc CPU allocates storage on GPU
- 18.074] Kernel command line: BOOT.IMAGE=/vmlinuz-4.2.3-300.fc23.x86\_64 root=/dev/mapper/fedora-root ro rd.lvm.lv=fedora-fedora-root ro rd.lvm.lv=fedora-fedora-fedora-root ro rd.lvm.lv=fedora-
  - kernel launch CPU launches kernel(s) on GPU to process the data
  - cudaMemcpy CPU copies results back to CPU from GPU

Owens advises minimizing "communication" as much as possible (e.g. the cudaMemcpy between CPU and GPU), and do a lot of computation in the CPU and GPU, each separately.

Defining the GPU Computation

Owens circled this

### BIG IDEA

This is Important

Kernels look like serial programs

Write your program as if it will run on **one** thread

The GPU will run that program on many threads

### Squaring A Number on the CPU

Note

- (1) Only 1 thread of execution: ("thread" := one independent path of execution through the code) e.g. the for loop
- (2) no explicit parallelism; it's serial code e.g. the for loop through 64 elements in an array

GPU Code A High Level View

CPU:

- Allocate Memory
- Copy Data to/from GPU
- Launch Kernel species degree of parallelism

GPU:

• Express Out = In · In - says nothing about the degree of parallelism

Owens reiterates that in the GPU, everything looks serial, but it's only in the CPU that anything parallel is specified. pseudocode: CPU code: square kernel <<< 64 >>> (outArray,inArray)

Squaring Numbers Using CUDA Part 3

From the example

```
// launch the kernel
square <<<1, ARRAY_SIZE>>>(d_out, d_in)
```

we're introduced to the "CUDA launch operator", initiating a kernel of 1 block of 64 elements (ARRAY\_SIZE is 64) on the GPU. Remember that d\_ prefix (this is naming convention) tells us it's on the device, the GPU, solely.

With CUDA launch operator ≡<<<>>>, then also looking at this explanation on stackexchange (so surely others are confused as well, of those who are learning this (cf. CUDA kernel launch parameters explained right?). From Eric's answer,

threads are grouped into blocks, all the threads will execute the invoked kernel function.

Certainly,

$$<<<>>>: (n_{block}, n_{threads}) \times kernel functions \mapsto kernel function <<< n_{block}, n_{threads} >>> \in End : Dat_{GPU}$$
  
 $<<<>>>: \mathbb{N}^+ \times \mathbb{N}^+ \times Mor_{GPU} \rightarrow EndDat_{GPU}$ 

where I propose that GPU can be modeled as a category containing objects  $Dat_{GPU}$ , the collection of all possible data inputs and outputs into the GPU, and  $Mor_{GPU}$ , the collection of all kernel functions that run (exclusively, and this *must* be the class, as reiterated by Prof. Owen) on the GPU.

Next,

```
kernelfunction <<< n_{\rm block}, n_{\rm threads}>>>: \dim \mapsto \operatorname{dout} (as given in the "square" example, and so I propose) kernelfunction <<< n_{\rm block}, n_{\rm threads}>>>: (\mathbb{N}^+)^{n_{\rm threads}} \to (\mathbb{N}^+)^{n_{\rm threads}}
```

But keep in mind that dout, din are pointers in the C program, pointers to the place in the memory. cudaMemcopy is a functor category, s.t. e.g.  $Obj_{CudaMemcopy} \ni cudaMemcpyDevicetoHost$  where

 $\operatorname{cudaMemcopy}(-, -, n_{\operatorname{thread}}, \operatorname{cudaMemcpyDeviceToHost}) : \operatorname{Memory}_{\operatorname{GPU}} \to \operatorname{Memory}_{\operatorname{CPU}} \in \operatorname{Hom}(\operatorname{Memory}_{\operatorname{GPU}}, \operatorname{Memory}_{\operatorname{CPU}})$ 

## Squaring Numbers Using CUDA 4

Note the C language construct declaration specifier - denotes that this is a kernel (for the GPU) and not CPU code. Pointers need to be allocated on the GPU (otherwise your program will crash spectacularly -Prof. Owen).

1.1.3. What are C pointers? Is  $\langle$  type  $\rangle$ \*, a pointer, then a mapping from the category, namely the objects of types, to a mapping from the specified value type to a memory address?
e.g.

$$\langle \rangle * : \text{float} \mapsto \text{float} *$$
  
float  $* : \text{din} \mapsto \text{some memory address}$ 

and then we pass in mappings, not values, and so we're actually declaring a square functor.

What is threadIdx? What is it mathematically? Consider that ∃ 3 "modules":

threadIdx.x threadIdx.y threadIdx.z

And then the line

says that idx is an integer, "declares" it to be so, and then assigns idx to thread Idx.x which surely has to also have the same type, integer. So (perhaps)

$$idx \equiv \text{threadIdx.} x \in \mathbb{Z}$$

is the same thing.

Then suppose threadIdx  $\subset$  FinSet, a subcategory of the category of all (possible) finite sets, s.t. threadIdx has 3 particular morphisms,  $x, y, z \in MorthreadIdx$ ,

$$x: \operatorname{threadIdx} \mapsto \operatorname{threadIdx}.x \in \operatorname{Obj}_{\operatorname{FinSet}}$$
  
 $y: \operatorname{threadIdx} \mapsto \operatorname{threadIdx}.x \in \operatorname{Obj}_{\operatorname{FinSet}}$   
 $z: \operatorname{threadIdx} \mapsto \operatorname{threadIdx}.x \in \operatorname{Obj}_{\operatorname{FinSet}}$ 

### Configuring the Kernel Launch Parameters Part 1

 $n_{\text{blocks}}$ ,  $n_{\text{threads}}$  with  $n_{\text{threads}} \ge 1024$  (this maximum constant is GPU dependent). You should pick the  $(n_{\text{blocks}}, n_{\text{threads}})$  that makes sense for your problem, says Prof. Owen.

1.1.4. Memory layout of blocks and threads.  $\forall (n_{\text{blocks}}, n_{\text{threads}}) \in \mathbb{Z} \times \{1 \dots 1024\}, \{1 \dots n_{\text{block}} \times \{1 \dots n_{\text{threads}}\} \text{ is now an ordered index (with lexicographical ordering)}$ . This is just 1-dimensional (so possibly there's a 1-to-1 mapping to a finite subset of  $\mathbb{Z}$ ).

I propose that "adding another dimension" or the 2-dimension, that Prof. Owen mentions is being able to do the Cartesian product, up to 3 Cartesian products, of the block-thread index.

Quiz: Configuring the Kernel Launch Parameters 2

Most general syntax:

Configuring the kernel launch

```
kernel <<< grid of blocks, block of threads >>>(...)

// for example
square <<< dim3(bx,by,bz), dim3(tx,ty,tz), shmem>>>(...)
where dim3(tx,ty,tz) is the grid of blocks bx · by · bz
{dim3}(tx,ty,tz) is the block of threads tx · ty · tz
shmem is the shared memory per block in bytes
```

Problem Set 1 "Also, the image is represented as an 1D array in the kernel, not a 2D array like I mentioned in the video.' Here's part of that code for squaring numbers:

```
--global_- void square(float *d_out, float *d_in) {
  int idx = threadIdx.x;
  float f = d_in[idx];
  d_out[idx] = f*f;
}
```

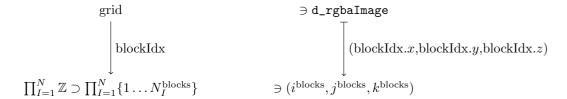
1.1.5. Grid of blocks, block of threads, thread that's indexed; (mathematical) structure of it all. Let

$$\operatorname{grid} = \prod_{I=1}^{N} (\operatorname{block})^{n_I^{\operatorname{block}}}$$

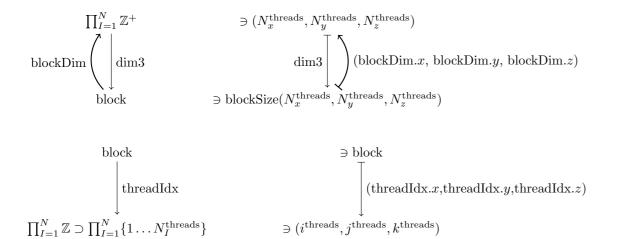
where 
$$N=1,2,3$$
 (for CUDA) and by naming convention  $egin{aligned} I=1\equiv x\\ I=2\equiv y\\ I=3\equiv z \end{aligned}$ 

Let's try to make it explicity (as others had difficulty understanding the grid, block, thread model, cf. colored image to greyscale image using CUDA parallel processing, Cuda gridDim and blockDim) through commutative diagrams and categories (from math):

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and then similar relations (i.e. arrows, i.e. relations) go for a block of threads:



gridsize help assignment 1 Pp explains how threads per block is variable, and remember how Owens said Luebki says that a GPU doesn't get up for more than a 1000 threads per block.

1.1.6. Generalizing the model of an image. Consider vector space V, e.g.  $\dim V = 4$ , vector space V over field  $\mathbb{K}$ , so  $V = \mathbb{K}^{\dim V}$ . Each pixel represented by  $\forall v \in V$ .

Consider an image, or space, M.  $\dim M = 2$  (image),  $\dim M = 3$ . Consider a local chart (that happens to be global in our case):

Consider a "coarsing" of underlying M:

$$\begin{array}{c} M\times V & \xrightarrow{\mathrm{proj}} & \operatorname{proj}(M)\times\operatorname{proj}(V) \\ \pi \downarrow & & \downarrow \operatorname{proj}(\pi) \\ M = \{1\dots N_1\}\times\{1\dots N_2\}\times \dots \times \{1\dots N_{\dim M}\} & \xrightarrow{\mathrm{proj}} \operatorname{proj}(M) = \{1\dots \frac{N_1}{N_1^{\mathrm{threads}}}\}\times\{1\dots \frac{N_2}{N_2^{\mathrm{threads}}}\}\times \dots \times \{1\dots \frac{N_{\dim M}}{N_{\dim M}^{\mathrm{threads}}}\} \end{array}$$

e.g. 
$$N_1^{\text{thread}} = 12$$
  
 $N_2^{\text{thread}} = 12$ 

Just note that in terms of syntax, you have the "block" model, in which you allocate blocks along each dimension. So in

$$const\ dim 3\ blockSize(n_x^b, n_y^b, n_z^b) \\ const\ dim 3\ gridSize(n_x^{\rm gr}, n_y^{\rm gr}, n_z^{\rm gr})$$

Then the condition is  $n_x^b/\mathrm{dim}V, n_y^b/\mathrm{dim}V, n_z^b/\mathrm{dim}V \in \mathbb{Z}$  (condition),  $(n_x^{\mathrm{gr}}-1)/\mathrm{dim}V, n_y^{\mathrm{gr}}/\mathrm{dim}V, n_z^{\mathrm{gr}}/\mathrm{dim}V \in \mathbb{Z}$ Transpose Part 1

Now

$$\operatorname{Mat}_{\mathbb{F}}(n,n) \xrightarrow{T} \operatorname{Mat}_{\mathbb{F}}(n,n)$$
  
 $A \mapsto A^{T} \text{ s.t. } (A^{T})_{ij} = A_{ji}$   
 $\operatorname{Mat}_{\mathbb{F}} \xrightarrow{T} \mathbb{F}^{n^{2}}$   
 $A_{ij} \mapsto A_{ij} = A_{in+j}$ 

$$\begin{array}{ccc}
\operatorname{Mat}_{\mathbb{F}}(n,n) & \longrightarrow \mathbb{F}^{n^2} & A_{ij} & \longmapsto & A_{in+j} \\
T & & \downarrow T & & T \downarrow & & \downarrow T \\
\operatorname{Mat}_{\mathbb{F}}(n,n) & \longrightarrow \mathbb{F}^{n^2} & (A^T)_{ij} = A_{ji} & \longmapsto & A_{jn+i}
\end{array}$$

#### Transpose Part 2

Possibly, transpose is a functor.

Consider struct as a category. In this special case, Objstruct = {arrays} (a struct of arrays). Now this struct already has a hash table for indexing upon declaration (i.e. "creation"): so this category struct will need to be equipped with a "diagram" from the category of indices J to struct:  $J \rightarrow$  struct.

So possibly

$$\begin{array}{ccc} \text{struct} \xrightarrow{T} & \text{array} \\ \text{ObjStruct} = \{ \text{ arrays } \} \xrightarrow{T} & \text{Objarray} = \{ \text{ struct } \} \\ J \rightarrow \text{ struct } \xrightarrow{T} & J \rightarrow \text{ array} \end{array}$$

Quiz: What Kind Of Communication Pattern This quiz made a few points that clarified the characteristics of these so-called communication patterns (amongst the memory?)

- map is bijective, and map :  $Idx \rightarrow Idx$
- gather not necessarily surjective
- scatter not necessarily surjective
- stencil surjective
- transpose (see before)

### Parallel Communication Patterns Recap

- map bijective
- transpose bijective
- gather not necessarily surjective, and is many-to-one (by def.)
- scatter one-to-many (by def.) and is not necessarily surjective
- stencil several-to-one (not injective, by definition), and is surjective
- $\bullet$  reduce all-to-one
- scan/sort all-to-all

### Programmer View of the GPU

thread blocks: group of threads that cooperate to solve a (sub)problem

Thread Blocks And GPU Hardware

CUDA GPU is a bunch of SMs:

Streaming Multiprocessors (SM)s

SMs have a bunch of simple processors and memory.

Dr. Luebki:

Let me say that again because it's really important GPU is responsible for allocating blocks to SMs

Programmer only gives GPU a pile of blocks.

Quiz: What Can The Programmer Specify

I myself thought this was a revelation and was not intuitive at first:

Given a single kernel that's launched on many thread blocks include X, Y, the programmer cannot specify the sequence the blocks, e.g. block X, block Y, run (same time, or run one after the other), and which SM the block will run on (GPU does all this).

### Quiz: A Thread Block Programming Example

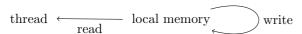
Open up hello blockIdx.cu in Lesson 2 Code Snippets (I got the repository from github, repo name is cs344).

At first, I thought you can do a single file compile and run in Eclipse without creating a new project. No. cf. Eclipse creating projects every time to run a single file?.

I ended up creating a new CUDA C/C++ project from File -; New project, and then chose project type Executable, Empty Project, making sure to include Toolchain CUDA Toolkit (my version is 7.5), and chose an arbitrary project name (I chose cs344single). Then, as suggested by Kenny Nguyen, I dragged and dropped files into the folder, from my file directory program.

I ran the program with the "Play" triangle button, clicking on the green triangle button, and it ran as expected. I also turned off Build Automatically by deselecting the option (no checkmark).

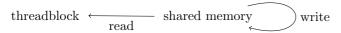
GPU Memory Model



Then consider threadblock  $\equiv$  thread block

Objthreadblock  $\supset \{ \text{ threads } \}$ 

 $FinSet \xrightarrow{threadIdx} thread \in Morthreadblock$ 



 $\forall$  thread



Synchronization - Barrier

Quiz: The Need For Barriers

3 barriers were needed (wasn't obvious to me at first). All threads need to finish the write, or initialization, so it'll need a barrier.

While

$$array[idx] = array[idx+1];$$

is 1 line, it'll actually need 2 barriers; first read. Then write.

So actually we'll need to rewrite this code:

```
int temp = array[idx+1];
__syncthreads();
array[idx] = temp;
__syncthreads();
```

kernels have implicit barrier for each.

Writing Efficient Programs

(1) Maximize arithmetic intensity arithmetic intensity :=  $\frac{\text{math}}{\text{memory}}$ 

video: Minimize Time Spent On Memory

local memory is fastest; global memory is slower

kernel we know (in the code) is tagged with \_\_global\_\_

quiz: A Quiz on Coalescing Memory Access

Work it out as Dr. Luebki did to figure out if it's coalesced memory access or not.

**Atomic Memory Operations** 

Atomic Memory Operations

atomicadd atomicmin atomicXOR atomicCAS Compare And Swap

2. Pointers in C; Pointers in C categorified (interpreted in Category Theory)

Suppose  $v \in \text{ObjData}$ , category of data **Data**,

e.g.  $v \in \text{Int} \in \text{ObjType}$ , category of types Type.

Data 
$$\xrightarrow{\&}$$
 Memory

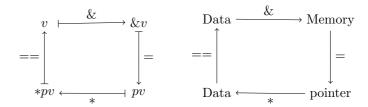
with address  $\&v \in Memory$ .

With

assignment pv = &v,

 $pv \in \text{Objpointer}$ , category of pointers, pointer  $pv \in \text{Memory}$  (i.e. not  $pv \in \text{Dat}$ , i.e.  $pv \notin \text{Dat}$ )

pointer 
$$\ni pv \stackrel{*}{\mapsto} *pv \in Dat$$



Examples. Consider  ${\tt passfunction.c}$  in Fitzpatrick [5].

Consider the type double, double  $\in$  ObjTypes. fun1, fun2  $\in$  MorTypes namely

 $\mathrm{fun1},\,\mathrm{fun2}\in\mathrm{Hom}(\mathrm{double},\mathrm{double})\equiv\mathrm{Hom}_{\mathrm{Types}}(\mathrm{double},\mathrm{double})$ 

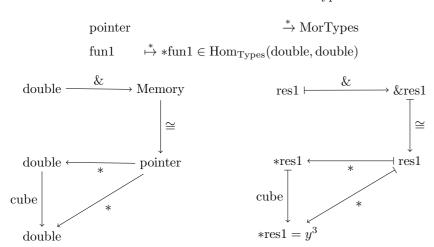
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Recall that

pointer 
$$\stackrel{*}{\rightarrow}$$
 Dat pointer  $\stackrel{\&}{\rightarrow}$  Memory

\*, & are functors with domain on the category pointer.

Pointers to functions is the "extension" of functor \* to the codomain of MorTypes:



It's unclear to me how void cube can be represented in terms of category theory, as surely it cannot be represented as a mapping (it acts upon a functor, namely the \* functor for pointers). It doesn't return a value, and so one cannot be confident to say there's explicitly a domain and codomain, or range for that matter.

But what is going on is that

pointer , double , pointer 
$$\xrightarrow{\text{cube}}$$
 pointer , pointer   
fun1,  $x$ , res1  $\xrightarrow{\text{cube}}$  fun1, res1

s.t. 
$$*res1 = y^3 = (*fun1(x))^3$$

So I'll speculate that in this case, cube is a functor, and in particular, is acting on \*, the so-called deferencing operator:

$$\begin{array}{ccc} \text{pointer} & \stackrel{*}{\rightarrow} \text{float} \in \text{Data} & \underset{\text{cube}}{\xrightarrow{\text{cube}}} & \text{pointer} & \stackrel{\text{cube}(*)}{\longrightarrow} \text{float} \in \text{Data} \\ & \text{res1} & \stackrel{*}{\mapsto} & \text{res1} & \xrightarrow{\text{cube}(*)} & \text{cube}(*\text{res1}) = y^3 \end{array}$$

cf. Arrays, from Fitzpatrick [5]

Types 
$$\xrightarrow{\text{declaration}}$$
 arrays

If  $x \in \text{Objarrays}$ ,

$$\&x[0] \in \text{Memory} \xrightarrow{==} x \in \text{pointer (to 1st element of array)}$$

cf. Section 2.13 Character Strings from Fitzpatrick [5]

- cf. C++ extensions for C according to Fitzpatrick [5]
- simplified syntax to pass by reference pointers into functions
- inline functions
- variable size arrays

```
int n:
double x[n];
```

• complex number class

```
Part 2. C++ and Computational Physics
  cf. 2.1.1 Scientific hello world from Hjorth-Jensen (2015) [6]
  in C.
  int main (int argc, char* argv[])
argc stands for number of command-line arguments
argy is vector of strings containing the command-line arguments with
    argv[0] containing name of program
    argv[1], argv[2], ... are command-line args, i.e. the number of lines of input to the program
  "To obtain an executable file for a C++ program" (i.e. compile (???)),
  gcc -c -Wall myprogram.c
  gcc -o myprogram myprogram.o
-Wall means warning is issued in case of non-standard language
-c means compilation only
-o links produced object file myprogram. o and produces executable myprogram
  # General makefile for c - choose PROG = name of given program
  # Here we define compiler option, libraries and the target
  CC = c ++ -Wall
  PROG= myprogram
  # Here we make the executable file
  PROG :
                        ${PROG}.o
                        ${CC} ${PROG}.o -o ${PROG}
```

# whereas here we create the object file

$$\#\{PROG\}.o: \$\{PROG\}.cpp \\ \$\{CC\} -c \$\{PROG\}.cpp$$

Here's what worked for me:

 ${CC} -c {PROG}.cpp$ 

# EY: 20160602 notice the different suffixes, and we see the pattern for the syntax

# (note: the <tab> in the command line is necessary formake towork)

# target: dependency1 dependency2 ...

# <tab> command

cf. 2.3.2 Machine numbers of Hjorth-Jensen (2015) [6]

cf. 2.5.2 Pointers and arrays in C++ of Hjorth-Jensen (2015) [6]

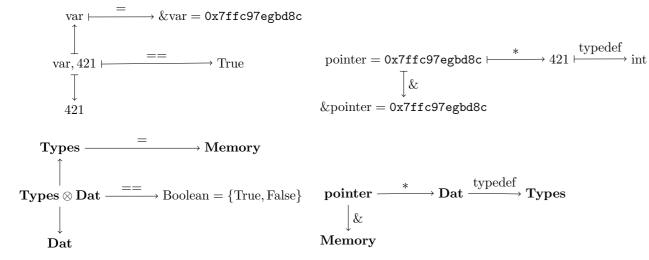
Initialization (diagram):

$$\& var = 0x7ffc97efbd8c \longmapsto pointer = \& var = 0x7ffc97efbd8c$$

$$Memory \longmapsto pointer$$

$$(memory) addresses \longmapsto Obj(pointer)$$

Referencing and deferencing operations on pointers to variables



2.1. Numerical differentiation and interpolation (in C++). cf. Chapter 3 "Numerical differentiation and interpolation" of Hjorth-Jensen (2015) [6].

This is how I understand it.

Consider the Taylor expansion for  $f(x) \in C^{\infty}(\mathbb{R})$ :

$$f(x) = f(x_0) + \sum_{j=1}^{\infty} \frac{f^{(j)}(x_0)}{j!} h^j$$

For  $x = x_0 \pm h$ ,

$$f(x) = f(x_0 \pm h) = f(x_0) + \sum_{i=1}^{\infty} \frac{f^{(2j)}(x_0)}{(2j)!} h^{2j} \pm \sum_{i=1}^{\infty} \frac{f^{(2j-1)}(x_0)}{(2j-1)!} h^{2j-1}$$

Then

$$f(x_0 + 2^k h) - f(x_0 - 2^k h) = 2 \sum_{j=1}^{\infty} \frac{f^{(2j-1)}}{(2j-1)!} (x_0) 2^{k(2j-1)} h^{2j-1} =$$

$$= 2 \left[ f^{(1)}(x_0) 2^k h + \sum_{j=2}^{\infty} \frac{f^{(2j-1)}(x_0)}{(2j-1)!} 2^{k(2j-1)} h^{2j-1} \right] =$$

$$= 2 \left[ f^{(1)}(x_0) 2^k h + \frac{f^{(3)}(x_0)}{3!} 2^{k(3)} h^3 + \sum_{j=3}^{\infty} \frac{f^{(2j-1)}(x_0)}{(2j-1)!} 2^{k(2j-1)} h^{2j-1} \right]$$

So for k = 1,

$$f(x_0 + h) - f(x_0 - h) = 2 \left[ f^{(1)}(x_0)h + \sum_{j=1}^{\infty} \frac{f^{(2j+1)}(x_0)}{(2j+1)!} h^{2j+1} \right]$$

Now

$$f(x_0 + 2^k h) + f(x_0 - 2^k h) - 2f(x_0) =$$

$$= 2 \sum_{j=1}^{\infty} \frac{f^{(2j)}(x_0)}{(2j)!} 2^{2jk} h^{2j} =$$

$$= 2 \left[ \frac{f^{(2)}(x_0)}{2} 2^{2k} h^2 + \sum_{j=2}^{\infty} \frac{f^{(2j)}(x_0)}{(2j)!} 2^{2jk} h^{2j} \right] =$$

$$= 2 \left[ \frac{f^{(2)}(x_0)}{2} 2^{2k} h^2 + \frac{f^{(4)}(x_0)}{4!} 2^{4k} h^4 + \sum_{j=3}^{\infty} \frac{f^{(2j)}(x_0)}{(2j)!} 2^{2jk} h^{2j} \right]$$

Thus for the case of k = 1,

$$f(x_0 + h) + f(x_0 - h) - 2f(x_0) = f^{(2)}(x_0)h^2 + 2\sum_{j=2}^{\infty} \frac{f^{(2j)}(x_0)}{(2j)!}h^{2j}$$

$$\frac{f(x_0 + h) - f(x_0 - h)}{2h} = f^{(1)}(x_0) + \sum_{j=1}^{\infty} \frac{f^{(2j+1)}(x_0)}{(2j+1)!}h^{2j}$$

$$\frac{f(x_0 + h) + f(x_0 - h) - 2f(x_0)}{h^2} = f^{(2)}(x_0) + 2\sum_{j=2}^{\infty} \frac{f^{(2(j+1))}(x_0)}{(2(j+1))!}h^{2j}$$

A pattern now emerges on how to include more calculations at points  $x_0, x_0 \pm 2^k h$  so to obtain better accuracy  $O(h^l)$ . For astance,

Given 5 pts.  $\{x_0, x_0 \pm h, x_0 \pm 2h\}$ ,

$$f(x_0 + 2h) - f(x_0 - 2h) = 2[f^{(1)}(x_0)2^1h + \frac{f^{(3)}(x_0)}{3!}2^3h^3 + O(h^5)]$$

$$f(x_0 + h) - f(x_0 - h) = 2[f^{(1)}(x_0)h + \frac{f^{(3)}(x_0)}{3!}h^3 + O(h^5)]$$

$$\implies f'(x_0) = \frac{f(x_0 - 2h) - 8f(x_0 - h) + 8f(x_0 + h) - f(x_0 + 2h)}{12h} + O(h^4)$$

Hjorth-Jensen (2015) [6] argues, on pp. 46-47, that the additional evaluations are time consuming, to obtain further accuracy, so it's a balance.

To summarize, for  $O(h^2)$  accuracy.

$$\frac{f(x_0+h)-f(x_0-h)}{2h} = f^{(1)}(x_0) + \sum_{j=1}^{\infty} \frac{f^{(2j+1)}(x_0)}{(2j+1)!} h^{2j}$$
  $O(h^2)$ 

$$\frac{f(x_0+h)+f(x_0-h)-2f(x_0)}{h^2}=f^{(2)}(x_0)+2\sum_{j=1}^{\infty}\frac{f^{(2j+2)}(x_0)}{(2j+2)!}h^{2j}$$
  $O(h^2)$ 

### 3. Interpolation

cf. 3.2 Numerical Interpolation and Extrapolation of Hjorth-Jensen (2015) [6]

$$y_0 = f(x_0)$$
 Given  $N+1$  pts.  $y_1 = f(x_1)$  ,  $x_i$ 's distinct (none of  $x_i$  values equal) 
$$\vdots$$
 
$$y_N = f(x_N)$$

We want a polynomial of degree n s.t.  $p(x) \in \mathbb{R}[x]$ 

$$p(x_i) = f(x_i) = y_i$$
  $i = 0, 1 ... N$ 

$$p(x) = a_0 + a_1(x - x_0) + \dots + a_i \prod_{j=0}^{i-1} (x - x_j) + \dots + a_N(x - x_0) \dots (x - x_{N-1}) = a_0 + \sum_{i=1}^{N} a_i \prod_{j=0}^{i-1} (x - x_j)$$

$$a_0 = f(x_0)$$

$$a_0 + a_1(x_1 - x_0) = f(x_1)$$

$$\vdots$$

$$a_0 + \sum_{i=1}^{k} a_i \prod_{j=0}^{i-1} (x_k - x_j) = f(x_k)$$

Hjorth-Jensen (2015) [6] mentions this Lagrange interpolation formula (I haven't found a good proof for it).

(1) 
$$p_N(x) = \sum_{i=0}^{N} \prod_{k \neq i} \frac{x - x_k}{x_i - x_k} y_i$$

# 4. Classes (C++)

# cf. C++ Operator Overloading in expression

Take a look at this link: C++ Operator Overloading in expression. This point isn't emphasized enough, as in Hjorth-Jenser (2015) [6]. This makes doing something like

$$d = a * c + d/b$$

work the way we expect. Kudos to user fredoverflow for his answer:

"The expression (e\_x\*u\_c) is an rvalue, and references to non-const won't bind to rvalues.

Also, member functions should be marked const as well.'

# 4.1. What are Ivalues and rvalues in C and C++? C++ Rvalue References Explained

Original definition of lvalues and rvalues from C:

lvalue - expression e that may appear on the left or on the right hand side of an assignment rvalue - expression that can only appear on right hand side of assignment =.

Examples:

```
int a = 42;
int b = 43;

// a and b are both l-values
a = b; // ok
b = a; // ok
a = a * b; // ok

// a * b is an rvalue:
int c = a * b; // ok, rvalue on right hand side of assignment
a * b = 42; // error, rvalue on left hand side of assignment
```

In C++, this is still useful as a first, intuitive approach, but

lvalue - expression that refers to a memory location and allows us to take the address of that memory location via the & operator.

rvalue - expression that's not a lyalue

So & reference functor can't act on rvalue's.

### 5. Numerical Integration

### 5.0.1. Trapezoid rule (or trapezoidal rule). See Integrate.ipynb.

From there, consider integration on [a, b], considering  $h := \frac{b-a}{N}$ , and N+1 (grid) points,  $\{a, a+h, a+2h, \dots, a+jh, \dots, a+Nh = b\}_{j=0\dots N}$ .

Then 
$$\frac{N}{2}$$
 pts. are our " $x_0$ ";  $x_0$ 's =  $\{a+h, a+3h, \ldots, a+(2j-1)h, \ldots, a+(\frac{2N}{2}-1)h\}_{j=1\ldots\frac{N}{2}}$ .

Notice how we really need to care about if N is even or not. If N is not even, then we'd have to deal with the integration at the integration limits and choosing what to do.

Ther

$$\int_{a}^{b} f(x)dx = \sum_{j=1}^{N/2} \int_{a+(2j-1)h-h}^{a+(2j-1)h+h} f(x)dx = \sum_{j=1}^{N/2} \frac{h}{2} (2f(a+(2j-1)h) + f(a+2(j-1)h) + f(a+2jh)) = h(f(a)/2 + f(a+h) + \dots + f(b-h) + \frac{f(b)}{2}) = h\left(\frac{f(a)}{2} + \sum_{j=1}^{N-1} f(a+jh) + \frac{f(b)}{2}\right)$$

5.0.2. Midpoint method or rectangle method. .

Let  $h := \frac{b-a}{N}$  be the step size. The grid is as follows:

$${a, a+h, \dots, a+jh, \dots, a+Nh = b}_{j=0\dots N}$$

The desired midpoint values are at the following N points:

$$\{a+\frac{h}{2}, a+\frac{3}{2}h, \dots, a+\frac{(2j-1)h}{2}, \dots, a+\left(N-\frac{1}{2}\right)h\}_{j=1\dots N}$$

and so

(2) 
$$\int_{a}^{b} f(x)dx \approx \sum_{j=1}^{N} f(x_{j})h = \sum_{j=1}^{N} f\left(a + \frac{(2j-1)h}{2}\right)h$$

5.0.3. Simpson rule. The idea is to take the next "order" in the Lagrange interpolation formula, the second-order polynomial, and then we can rederive Simpson's rule. The algebra is worked out in Integrate.ipynb.

From there, then we can obtain Simpson's rule,

$$\int_{a}^{b} f(x)dx = \sum_{j=1}^{N/2} \int_{a+2(j-1)h}^{a+2jh} f(x)dx = \sum_{j=1}^{N/2} \frac{h}{3} (4f(a+(2j-1)h) + f(a+2(j-1)h) + f(a+2jh)) =$$

$$= \frac{h}{3} \left[ f(a) + f(b) + \sum_{j=1}^{N/2} 4f(a+(2j-1)h) + 2 \sum_{j=1}^{N/2-1} f(a+2jh) \right]$$

5.1. Gaussian Quadrature. cf. Hjorth-Jensen (2015) [6], Section 5.3 Gaussian Quadrature, Chapter 5 Numerical Integration

6. Call by reference - Call by Value, Call by reference (in C and in C++)

cf. pp. 58, 2.10 Pointers Ch. 2 Scientific Programming in C, Fitzpatrick [5] printfact3.c, printfact3.c pass pointer, pass by reference, call by pointer, call by reference In C:

• function prototype -

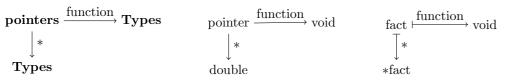


 $\Longrightarrow$ 

void factorial(double \*)

where for factorial, it's just your choice of name for function.

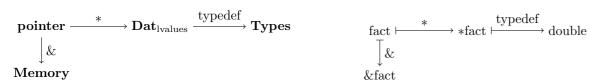
• function definition -



=

void function(double \*fact) { ... }

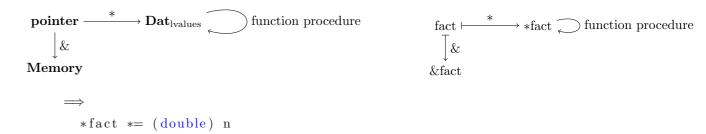
*Inside* the function definition,



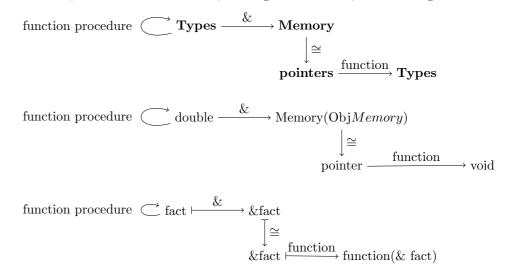
and so, for instance, in the function definition, you can do things like this:

and so notice that from \*fact = 1, \*fact is a lvalue.

- function procedure



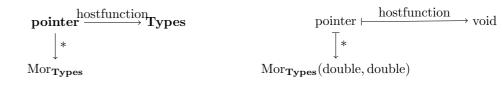
• "Using" the function, function "instantiation", "calling" the function, i.e. "running" the function



where, again simply note the notation, that we're using function and factorial, fact for nameofpointer, interchangeably: see printfact3.c for the example I'm referring to.

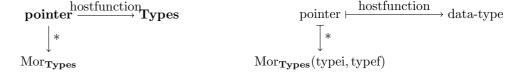
Again, in C, consider a pointer to a function passed to another function as an argument. Take a look at passfunction.c simultaneously.

• function prototype -



 $\Longrightarrow$ 

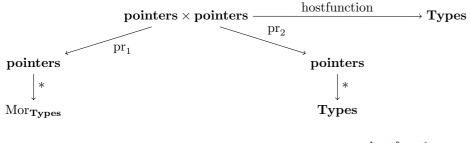
We could further generalize this syntax, simply for syntax and notation sake, as such:

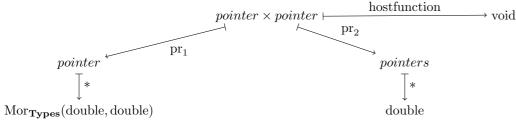


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 $\Longrightarrow$ 

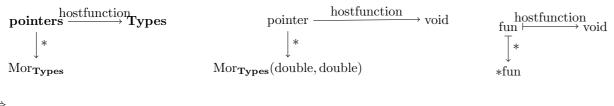
For practice, consider more than 1 argument in our function, and the other argument, for practice, is a pointer, we're "passing by reference."





 $\Longrightarrow$ 

• function definition



 $\Longrightarrow$ 

• *Inside* the function definition,

Types 
$$\xrightarrow{*\text{fun}}$$
 Types  $\xrightarrow{=}$  Types

double  $\xrightarrow{*\text{fun}}$  double  $\xrightarrow{=}$  double

 $x \mapsto (*\text{fun})(x) \mapsto y = (*\text{fun})(x)$ 

 $\Longrightarrow$ 

$$y = (*fun)(x)$$

• "Using" the function - the *actual* syntax for "passing" a function into a function is interesting (peculiar?): you only need the *name* of the function.

Let's quickly recall how a function is prototyped, "declared" (or, i.e., defined), and used:

- function prototype -

$$\mathbf{Types} \xrightarrow{-fun1} \mathbf{Types}$$

double 
$$\xrightarrow{\text{fun1}}$$
 double

 $\Longrightarrow$ 

- function definition -

$$\mathbf{Types} \xrightarrow{\quad fun1 \quad} \mathbf{Types}$$

$$double \xrightarrow{\quad fun1 \quad} double$$

$$z \stackrel{\text{fun1}}{\longrightarrow} 3.0z * z - z (= 3z^2 - z)$$

 $\Longrightarrow$ 

– Using function - fun1(z) and so

$$fun1 \in Mor_{\mathbf{Types}}(double, double)$$

And so again, it's interesting in terms of syntax that all you need is the *name* of the function to pass into the arguments of the "host function" when using the host function:

$$\operatorname{Mor}_{\mathbf{Types}} \xrightarrow{\operatorname{hostfunction}} \mathbf{Types}$$

$$\operatorname{Mor}_{\mathbf{Types}}(\operatorname{double},\operatorname{double}) \overset{hostfunction}{\longmapsto} \operatorname{void}$$

$$\begin{array}{c}
\text{hostfunction} \\
\text{fun1} & \longrightarrow \text{hostfunction(fun1)}
\end{array}$$

\_

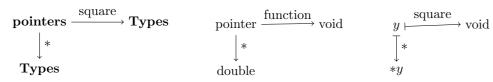
6.0.1. C++ extensions, or how C++ pass by reference (pass a pointer to argument) vs. C. Recall how C passes by reference, and look at Fitzpatrick [5], pp. 83-84 for the square function:

 $\bullet \ \ function \ prototype \ \text{-}$ 

 $\Longrightarrow$ 

void square(double \*)

• function definition -



void square(double \*y) { ... }

*Inside* the function definition,

$$\mathbf{pointer} \xrightarrow{\quad * \quad} \mathbf{Dat_{lvalues}} \xrightarrow{\quad typedef} \mathbf{Types} \qquad \qquad y \models \xrightarrow{\quad * \quad} y \models \xrightarrow{\quad typedef} \mathbf{doubl}$$

and so, for instance, in the function definition, you can do things like this:

$$y = x * x$$

• "Using" the function, function "instantiation", "calling" the function, i.e. "running" the function

function procedure 
$$\longrightarrow$$
 **Types**  $\longrightarrow$  **Memory**

$$\downarrow \cong$$

$$\mathbf{pointers} \xrightarrow{\text{square}} \mathbf{Types}$$
function procedure  $\longrightarrow$  double  $\longrightarrow$  Memory(ObjMemory)

$$\downarrow \cong \text{square}$$
pointer  $\longrightarrow$  void

function procedure 
$$\subset$$
 res  $\longmapsto$  &res 
$$\downarrow \cong$$
 
$$\downarrow \cong$$
 
$$\& res \longmapsto square (\& res)$$

6.0.2. C++ syntax for dealing with passing pointers (and arrays) into functions. However, in C++, a lot of the dereferencing \* and referencing & is not explicitly said so in the syntax. In this syntax, passing by reference is indicated by prepending the & ampersand to the variable name, in function declaration (prototype and definition). We don't have to explicitly deference the argument in the function (it's done behind the scene) and syntax-wise (it seems), we only have to refer to the argument by regular local name.

Indeed, the syntax appears "shortcutted" greatly:

• function prototype -

$$\mathbf{pointer} \times \mathbf{Types} \xrightarrow{\mathrm{function}} \mathbf{Types}$$
 pointer, double  $\stackrel{\mathrm{function}}{\longmapsto}$  void

 $\Longrightarrow$ 

void function (double &)

• function definition -

$$\begin{array}{ccc} \mathbf{pointers} \times \mathbf{Types} & \xrightarrow{\mathrm{square}} \mathbf{Types} & \mathrm{pointer, double} & \xrightarrow{\mathrm{function}} \mathrm{void} & \&, y & \xrightarrow{\mathrm{function}} \mathrm{function}(\mathrm{double} & \& y) \\ \Longrightarrow & \end{array}$$

void function (double &y) { ... }

*Inside* the function definition,

$$\begin{array}{ccc} \operatorname{End}(\operatorname{double},\operatorname{double}) & \operatorname{End}(\operatorname{double},\operatorname{double}) \\ \operatorname{double} & y \longmapsto y = x * x \\ \end{array}$$

and so, for instance, in the function definition, you can do things like this:

$$y = x * x$$

with no deferencing needed.

• "Using" the function, function "instantiation", "calling" the function, i.e. "running" the function

$$\mathbf{Types} \xrightarrow{\mathrm{function}} \mathbf{Types} \qquad \qquad \mathrm{double} \xrightarrow{\mathrm{function}} \mathrm{void} \qquad \qquad \mathrm{res} \xrightarrow{\mathrm{function}} \mathrm{function}(\mathrm{res})$$

6.0.3. C++ note on arrays. For dealing with arrays, Stroustrup (2013) [7], on pp. 12 of Chapter 1 The Basics, Section 1.8 Pointers, Arrays, and References, does the following:

• array declaration -

• "Using" arrays in function prototypes, i.e. passing into arguments of functions for function prototypes

• "Using" arrays when "using" functions, i.e. passing into arguments when a function is "called" or "executed"

```
function (arrayname)
```

Fitzpatrick [5] mentions using inline for short functions, no more than 3 lines long, because of memory cost of calling a function.

6.0.4. Need a CUDA, C, C++, IDE? Try Eclipse! This website has a clear, lucid, and pedagogical tutorial for using Eclipse: Creating Your First C++ Program in Eclipse. But it looks like I had to pay. Other than the well-written tips on the webpage. I looked up stackexchange for my Eclipse questions (I had difficulty with the Eclipse documentation).

Others, like myself, had questions on how to use an IDE like Eclipse when learning CUDA, and "building" (is that the same as compiling?) and running only single files.

My workflow: I have a separate, in my file directory, folder with my github repository clone that's local.

I start a New Project, CUDA Project, in Eclipse. I type up my single file (I right click on the src folder and add a 'Source File'). I build it (with the Hammer, Hammer looking icon; yes there are a lot of new icons near the top) and it runs. I can then run it again with the Play, triangle, icon.

I found that if I have more than 1 (2 or more) file in the src folder, that requires the main function, it won't build right.

So once a file builds and it's good, I, in Terminal, cp the file into my local github repository. Note that from there, I could use the nvcc compiler to build, from there, if I wanted to.

Now with my file saved (for example, helloworldkernel.cu), then I can delete it, without fear, from my, say, cuda-workplace, from the right side, "C/C++ Projects" window in Eclipse.

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Take a look at 3.2.2 A Kernel Call, a Hello World in CUDA C, with a simple kernel, on pp. 23 of Sanders and Kandrot (2010) [8] and on github, [helloworldkernel.cu](https://github.com/ernestyalumni/CompPhys/blob/master/CUDA-By-Example/helloworldkernel.cu). Let's work out the functor interpretation for practice.

• function definition -

$$\begin{array}{c} \mathbf{Types} \xrightarrow{\mathrm{kernel}} \mathbf{Types} \\ \text{void} \xrightarrow{\mathrm{kernel}} \text{void} \end{array}$$

CUDA C adds the \_\_global\_\_ qualifier to standard C to alert the compiler that the function, kernelfunction, should be compiled to run on the device, not the host (pp. 24 [8]).

• "Using", "calling", "running" function -

$$<<<>>>: (n_{block}, n_{threads}) \times kernelfunction \mapsto kernelfunction <<< n_{block}, n_{threads} >>> \in End(Dat_{\mathbf{Types}})$$
 $<<<>>>: \mathbb{N}^{+} \times \mathbb{N}^{+} \times Mor_{GPU} \rightarrow End(Dat_{GPU})$ 
 $\Leftrightarrow$ 
 $kernel <<<1,1>>>();$ 

cf. 3.2.3 Passing Parameters of Sanders and Kandrot (2010) [8]

Taking a look at [add-passb.cu](https://github.com/ernestyalumni/CompPhys/blob/master/CUDA-By-Example/add-passb.cu), let's work out the functor interpretation of cudaMalloc, cudaMemcpy.

In main, "declaring" a pointer:

 $\Leftarrow$ 

 $\mathbf{pointers} \overset{*}{-\!\!\!-\!\!\!-\!\!\!-\!\!\!-} \mathbf{Dat}_{\mathrm{lvalues}} \overset{\mathrm{typedef}}{-\!\!\!\!-\!\!\!\!-\!\!\!\!-} \mathbf{Types}$ 

$$dev_c \longmapsto *dev_c \longmapsto typedef$$
 int

We can also do, note, the sizeof function (which is a well-defined mapping, for once) on ObjTypes:

$$\mathbf{pointers} \xrightarrow{\quad * \quad} \mathbf{Dat}_{\mathrm{lvalues}} \xrightarrow{\quad \mathrm{typedef} \quad} \mathbf{Types} \xrightarrow{\quad \mathrm{sizeof} \quad} \mathbb{N}^{+}$$

$$\mathtt{dev\_c} \longmapsto *\mathtt{dev\_c} \longmapsto \mathtt{int} \longmapsto \mathtt{sizeof} \mapsto \mathtt{sizeof(int)}$$

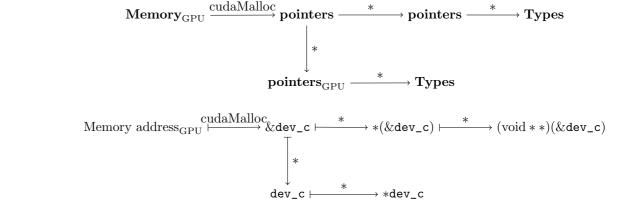
Consider what Sanders and Kandrot says about the pointer to the pointer that (you want to) holds the address of the newly allocated memory. [8] Consider this diagram:

I propose that what cudaMalloc does (actually) is the following:

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(3)

 $\Longrightarrow$ 



dev\_c is now a *device pointer*, available to kernel functions on the GPU. Syntax-wise, we can relate this diagram to the corresponding function "usage":

$$\begin{aligned} \mathbf{pointers} \times \mathbb{N}^{+} & \overset{\mathrm{cudaMalloc}}{\longrightarrow} & \mathrm{cudaError\_r} \\ & ((\mathrm{void} * *)(\&\mathtt{dev\_c}), (\mathrm{sizeof(int)})) & \overset{\mathrm{cudaMalloc}}{\longmapsto} & \mathrm{cudaSuccess} \ (\mathrm{for} \ \mathrm{example}) \end{aligned}$$

For practice, consider now cudaMemcpy in the functor interpretation, and its definition as such:

 $\textbf{cudaMemcpy} \ is \ a \ "functor \ category", \ s.t., \ we \ equip \ the \ functor \ \textbf{cudaMemcpy} \ with \ a \ collection \ of \ objects \ Obj_{cudaMemcpy}, \ s.t., \\ for \ example, \ cudaMemcpyDevicetoHost \ \in Obj_{cudaMemcpy}, \ where$ 

 $(\text{cudaMemcpy}(-, -, n_{\text{thread}}, \text{cudaMemcpyDevicetoHost}) : \mathbf{Memory}_{GPU} \to \mathbf{Memory}_{CPU}) \in \text{Hom}(\mathbf{Memory}_{GPU}, \mathbf{Memory}_{CPU})$ where  $\text{Obj}\mathbf{Memory}_{GPU} \equiv \text{collection of all possible memory (addresses) on GPU}$ .

It should be noted that, syntax-wise, & $c \in \text{ObjMemory}_{CPU}$  and &c belongs in the "first slot" of the arguments for cudaMemcpy, whereas  $\text{dev\_c} \in \text{pointers}_{GPU}$  a device pointer, is "passed in" to the "second slot" of the arguments for cudaMemcpy.

7.1. **Threads, Blocks, Grids.** cf. Chapter 5 Thread Cooperation, Section 5.2. Splitting Parallel Blocks of Sanders and Kandrot (2010) [8].

Consider first a 1-dimensional block.

• threadIdx.x  $\iff M_x \equiv$  number of threads per block in x-direction. Let  $j_x = 0 \dots M_x - 1$  be the index for the thread. Note that  $1 \le M_x \le M_x^{\max}$ , e.g.  $M_x^{\max} = 1024$ , max. threads per block

- blockIdx.x  $\iff N_x \equiv$  number of blocks in x-direction. Let  $i_x = 0 \dots N_x 1$
- blockDim stores number of threads along each dimension of the block  $M_{\tau}$ .

Then if we were to "linearize" or "flatten" in this x-direction,

$$k = j_x + i_x M_x$$

where k is the kth thread.  $k = 0 \dots N_x M_x - 1$ .

Suppose vector is of length N. So we need N parallel threads to launch, in total.

e.g. if  $M_x = 128$  threads per block,  $N/128 = N/M_x$  blocks to get our total of N threads running.

Wrinkle: integer division! e.g. if  $N=127, \frac{\dot{N}}{128}=0$ . Solution: consider  $\frac{N+127}{128}$  blocks. If  $N=l\cdot 128+r, \ l\in\mathbb{N}, \ r=0\dots 127$ .

$$\frac{N+127}{128} = \frac{l \cdot 128 + r + 127}{128} = \frac{(l+1)128 + r - 1}{128} =$$

$$= l+1 + \frac{r-1}{128} = \begin{cases} l & \text{if } r = 0\\ l+1 & \text{if } r = 1 \dots 127 \end{cases}$$

$$\frac{N + (M_x - 1)}{M_x} = \frac{l \cdot M_x + r + M_x - 1}{M_x} = \frac{(l+1)M_x + r - 1}{M_x}$$

$$= l + 1 + \frac{r - 1}{M_x} = \begin{cases} l & \text{if } r = 0\\ l + 1 & \text{if } r = 1 \dots M_x - 1 \end{cases}$$

So  $\frac{N+(M_x-1)}{M_x}$  is the smallest multiple of  $M_x$  greater than or equal to N, so  $\frac{N+(M_x-1)}{M_x}$  blocks are needed or more than needed to run a total of N threads.

Problem: Max. grid dim. in 1-direction is 65535,  $\equiv N_i^{\text{max}}$ .

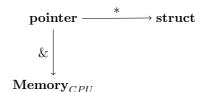
So  $\frac{N+(M_x-1)}{M_x} = N_i^{\max} \Longrightarrow N = N_i^{\max} M_x - (M_x-1) \le N_i^{\max} M_x$ . i.e. number of threads N is limited by  $N_i^{\max} M_x$ .

- number of threads per block in x-direction  $\equiv M_x \Longrightarrow blockDim.x$
- number of blocks in grid  $\equiv N_x \Longrightarrow \mathtt{gridDim.x}$
- $N_x M_x$  total number of threads in x-direction. Increment by  $N_x M_x$ . So next scheduled execution by GPU at the  $k = N_x M_x$  thread.
- 7.2. (CUDA) Constant Memory. cf. Chapter 6 Constant Memory of Sanders and Kandrot (2010) [8] Refer to the ray tracing examples in Sanders and Kandrot (2010) [8], and specifically, here: raytrace.cu, rayconst.cu. Without constant memory, then this had to be done:
  - definition (in the code) Consider struct as a subcategory of Types since struct itself is a category, equipped with objects and functions (i.e. methods, modules, etc.).

So for struct, Objstruct  $\ni$  Sphere.  $\Longrightarrow$ 

• Usage, "instantiation", i.e. creating, or "making" it (the struct):





 $Memoryaddress_{CPU}$ 

$$\Longrightarrow$$

Recalling Eq. 3, for SPHERES ==40 (i.e. for example, 40 spheres) cudaMalloc((void \*\*) &s. sizeof(Sphere)\*SPHERES)

 $\mathbf{Memory}_{\mathrm{GPU}} \xrightarrow{\mathrm{cudaMalloc}} \mathbf{pointers} \xrightarrow{\quad * \quad} \mathbf{pointers} \xrightarrow{\quad * \quad} \mathbf{Types}$ 

$$\begin{array}{c} \text{Memory address}_{\text{GPU}} & \stackrel{\text{cudaMalloc}}{\longmapsto} \&s & \stackrel{*}{\longmapsto} *(\&s) & \stackrel{*}{\longmapsto} & (\text{void} * *)(\&s) \\ \downarrow & & \downarrow & \\ \downarrow & & & * \\ & & & & * \\ \end{array}$$

and syntax-wise.

$$\mathbf{pointers} \times \mathbb{N}^{+} \xrightarrow{\operatorname{cudaMalloc}} \operatorname{cudaError\_r}$$

$$((\text{void} * *)(s), \text{sizeof(Sphere)} * \text{SPHERES}) \xrightarrow{\text{cudaMalloc}} \text{cudaSuccess (for example)}$$

Now consider

$$\verb|cudaMemcpy|(s, temp\_s, sizeof(Sphere)| * SPHERES, cudaMemcpyHostToDevice)|$$

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The lesson then is this, in light of how long ray tracing takes with constant memory and without constant memory cudaMemcpy between host to device, CPU to GPU, is a costly operation. Here, in this case, we're copying from the host memory to memory on the GPU. It copies to a global memory on the GPU.

Now, using constant memory,

we no longer need to do cudaMalloc, allocate memory on the GPU, for s, pointer to a Sphere.

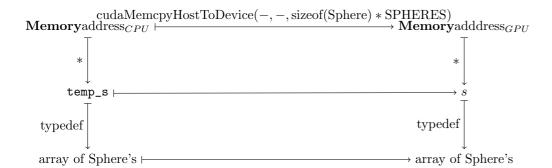
Instead, we have

In this particular case, we want it to have global scope.

Note, it is still on host memory.

Notice that

$$\begin{array}{c} \operatorname{cudaMemcpyHostToDevice}(-,-,\operatorname{sizeof}(\operatorname{Sphere}) * \operatorname{SPHERES}) \\ \operatorname{\mathbf{Memory}}_{CPU} & \longrightarrow \operatorname{\mathbf{Memory}}_{GPU} \end{array}$$



So notice that we have a bijection, and on one level, we can think of the bijection from temp\_s, an array of Sphere's to s, array of Sphere's. So notice that the types and memory size of temp\_s and s must match.

And for this case, that's all there is to constant memory. What's going on involves the so-called warp, a collection of thread "woven together" and get executed in lockstep. NVIDIA hardware broadcasts a single memory read to each half-warp. "every thread in a half-warp requests data from the same address in constant memory, your GPU will generate only a single read request and subsequently broadcast the data to every thread." (cf. Sanders and Kandrot (2010) [8]). Furthermore, "the hardware can aggressively cache the constant data on the GPU."

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