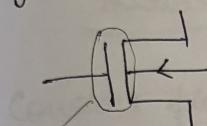
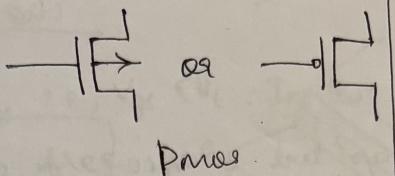


21st / 2 / 24

Mosle's law - for every 18 months, no. of transistors doubles for given area.

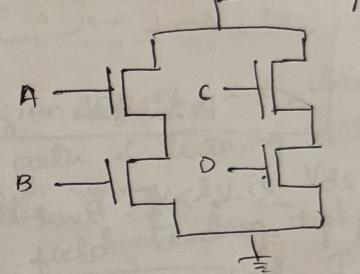
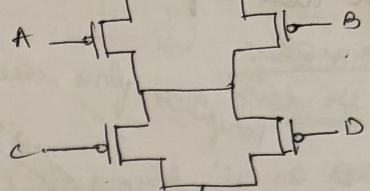


NMOS
gap is width of dielectric

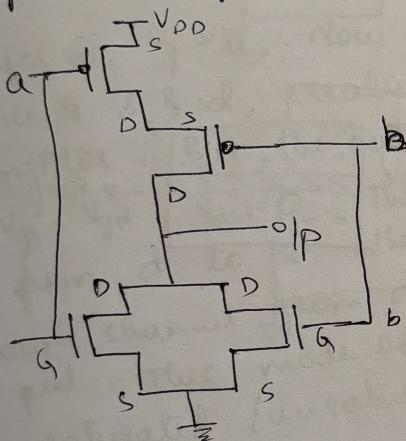


OR

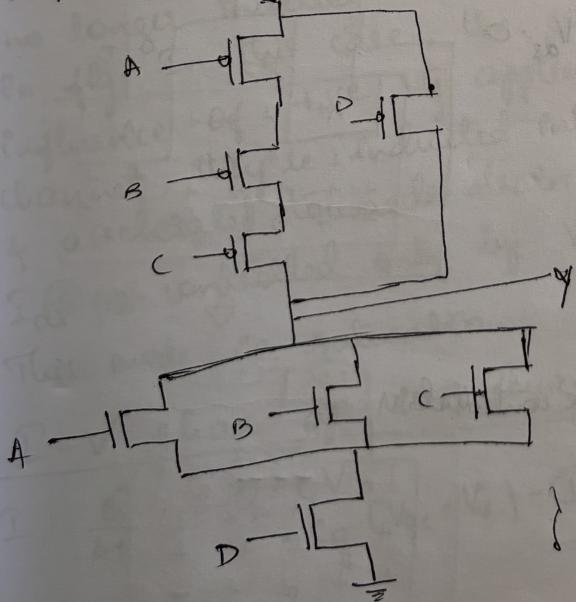
$$1) Y = \overline{AB + CD} \quad V_{DD}$$



2 input NOR gate



$$2) Y = \overline{(A + B + C)} D$$



	pull up (off)	pull up (on)
pull down (off)	Z	1
pull down (on)	0	X

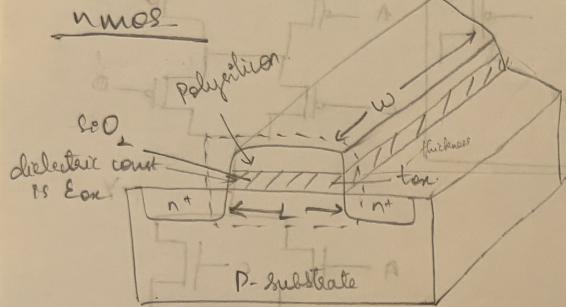
power consumption

$$A + B + C$$

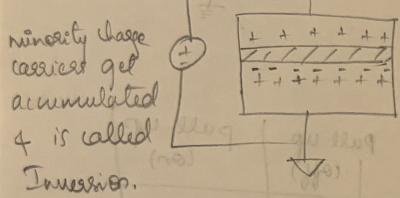
13/24.

MOS Transistor Theory.

nMOS is faster than pMOS as the mobility of e⁻ is faster than that of holes.



↑ the $V_g \rightarrow V_g > V_t$ min V_g required to punch the channel.



How to vary V_t : ↓ ϵ_{ox} , ↓ ϵ_{ox} .

Operation of nMOS device.

1) Cut-off (sub-threshold): $V_{gs} < V_t \rightarrow V_{ds} = 0$ (off region)

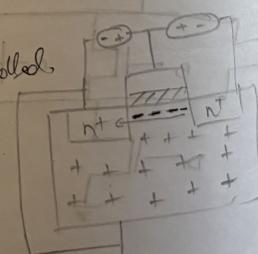
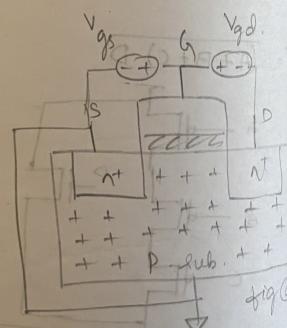
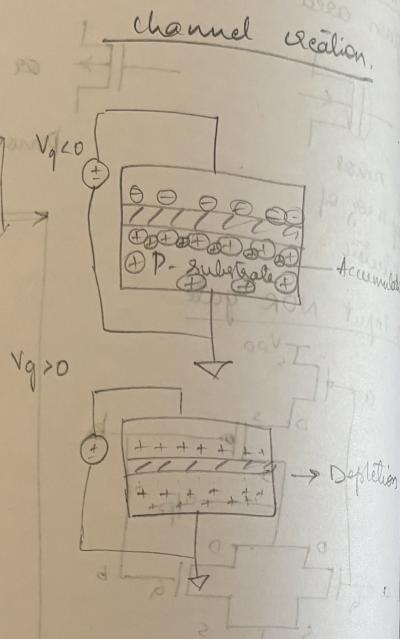
2) Linear region: $V_{gs} = V_{gd}$.

$$V_{gs} > V_t \quad V_{ds} = V_{gs} - V_{gd}$$

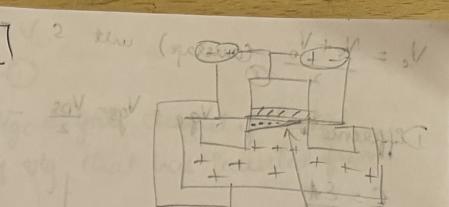
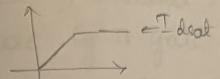
$$V_{ds} = 0$$

$$\star [V_{gs} > V_{ds} > V_{gd}] V_t \text{ or } [V_{ds} < V_{gs} - V_t]$$

Once the electrons start moving, V_g can be controlled.



3) Saturation: $V_{gs} > V_t$ $\boxed{V_{ds} > V_{gs} - V_t}$



Consider fig ③, V_{gs} i.e., $V_g > V_t$. In this case, only S & d are having free holes but no e⁻. The junction b/w body of source are zero biased, so no current flows. $\therefore I_d$ is off. This is cut-off mode.

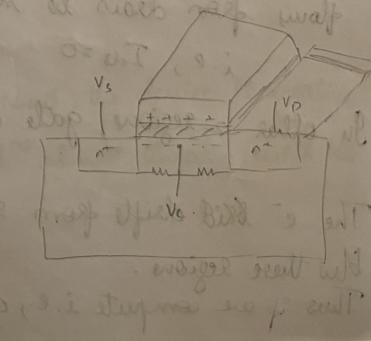
In fig ④, $V_g > V_t$. Now the inversion region of e⁻ i.e., channel connects S & d, creating a conducting path & turning all the transistors on. But the potential diff b/w the d & s is $V_{ds} = V_{gs} - V_{gd}$. $\because V_{gs} = V_{gd}$, $V_{ds} = 0$. There is no electric field tending to push I from d to s, when small amt of V_{ds} is applied, I_{ds} flows through channel from d to s. The I ^{res} when both V_{ds} & V_{gs} are fed. This mode of op. is termed as linear, resistive, triode. non-saturated / unsaturated.

When V_{ds} becomes sufficiently large i.e., $V_{ds} > V_t$, a channel is no longer inverted near drain & becomes pinched off as shown in fig. In this case, the conduction is due to drift of e⁻ under influence of +ve V_g applied at drain. As e⁻s reach end of the channel, they're induced into depletion region near the drain & accelerated towards drain, to stop above this drain V_g , & controlled only by V_g & cease to be influenced by drain. I_{ds} is controlled only by V_g & ceases to be influenced by drain. This mode is saturation.

I-V char of MOS device.

$$I = \frac{Q}{\Delta t} \quad Q = CV \\ = Cg(V_{gc} - V_t) - ①$$

$$V_{gc} = ?$$



$$V_c = \frac{V_s + V_D}{2} \quad (\text{cancellation}) \quad \text{w.r.t } S = V_s + \frac{V_{DS}}{2} \quad \text{--- (3)}$$

$$\text{Difference} \Rightarrow V_{gc} = V_{gs} - \frac{V_{DS}}{2} \quad \text{--- (4)}$$

$$C = \frac{\epsilon A}{d}$$

$$C_g = \frac{\epsilon_0 \epsilon_{ox} L W}{t_{ox}} \quad \text{--- (5)}$$

$$N \propto E$$

$$V = ME \quad \text{--- (7)}$$

$$E = \frac{V_{ds}}{L} \quad \text{--- (8)}$$

$$V = \mu \frac{V_{ds}}{L}$$

$$V_{ds} \equiv V_{gs} - V_t = V_{gat}$$

$$I_{ds} = \beta \left[(V_{gs} - V_t)^2 - \frac{V_{gs} - V_t}{2} \right]$$

$$I_{ds} = \frac{\beta}{2} [(V_{gs} - V_t)^2] \quad \text{- Saturation}$$

MOSFET operates in 3 regions ().

a) Cut-off $\rightarrow V_{gs} < V_t$. There is no channel & almost 0 current flowing from drain to source i.e., $I_{ds} = 0$.

In other 2 regions, gate attracts carrier to form channel.

The e^- drift from source to drain at a rate \propto to E-field (EF) b/w these regions.

Thus if we compute i.e., amount of charge in channel of the

$$\begin{aligned} I_{ds} &= \frac{Q}{\Delta t} \\ \frac{Q}{V} &= \frac{Q}{L} = \frac{QV}{L} \quad \text{--- (6)} \\ &= \frac{QV}{L} = \left(\frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} \right) \frac{W}{L} \left(V_{gs} - \frac{V_{ds}}{2} - V_t \right) \cdot \frac{1}{L} \mu \frac{V_{ds}}{L} \\ I_{ds} &= C_{ox} \frac{W}{L} \mu \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad \text{--- (9)} \\ I_{ds} &= \beta \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \quad \text{--- (10) linear} \end{aligned}$$

rate at which it moves. $Q = CV$.

Then Q channel = $C_g(V_{gc} - V_t)$ --- (1).

where C_g is gate capacitance, V_{gc} = gate channel potential & $V_{gc} - V_t$ is min amount of V_{gc} that has injected from p to n.

$$\text{Avg } V_c = \frac{V_s + V_D}{2} \quad \text{w.r.t } S \Rightarrow V_s + \frac{V_{DS}}{2}$$

\therefore the mean diff b/w gate & channel potential V_{gc} is

$$V_{gc} = V_{gs} + \frac{V_{DS}}{2}$$

To find gate cap C_g :

if gate has length 'l' & width 'w' & oxide thickness t_{ox} , $\epsilon_{ox} = \epsilon_0 \epsilon_{si}$.

$$C = \frac{\epsilon A}{d} \quad C_g = \frac{\epsilon_0 \epsilon_{ox} L W}{t_{ox}} \quad \text{&} \quad C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$$

cap/unit area of gate oxide.

Each carrier in channel is accelerated when avg velocity (drift velocity) \propto lateral EF & const of proportionality M called carrier mobility. $N \times E \Rightarrow V = ME$.

The EF, E is v/g diff b/w drain & source by channel length.

$$E = \frac{V_{ds}}{L}$$

The time required for carrier to cross the channel length by drift velocity, $1/V$ is the current.

$$I_{ds} = \frac{Q_{\text{channel}}}{L} \cdot \frac{1}{V}$$

When $V_{gs} > V_t$ but V_{ds} is relatively small, the device is resistive because $\frac{V_{ds}}{2} \ll (V_{gs} - V_t)$. i.e., I_{ds} \propto almost linearly with V_{ds} .

Just like ideal diode.

In sat. region, $V_{ds} > V_{dsat} \equiv V_{gs} - V_t$. The channel is no longer inverted in vicinity of the drain. We say the channel is pinched off. Beyond this pt, called the drain sat. V_{tg} going V_d has no further effect on I .

$$V_{ds} = V_{gs} - V_t$$

$$I_{ds} = \beta \left[(V_{gs} - V_t)^2 - \frac{(V_{gs} - V_t)^2}{2} \right]$$

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

$$I_{dsat} = \frac{\beta}{2} (V_{DD} - V_t)^2$$

Summary:

$$I_{ds}$$

Cut-off

$$I_{ds} = 0$$

conditions
 $V_{gs} < V_t$

$$I_{ds}(MA)$$

Linear

$$I_{ds} = \beta \left(V_{gs} - V_t \right) \frac{V_{gs} - V_{ds}}{2}$$

$$= \frac{\beta}{2} V_{ds}$$

Saturation

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

$$V_{gs} > V_t$$

$$V_{ds} > V_{dsat}$$

* (10 m) DC characteristics of CMOS Inverter.

Static

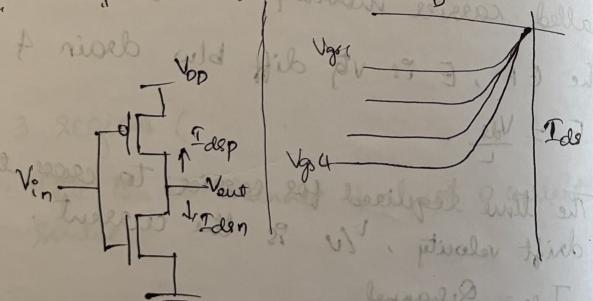
$$\text{Let } \beta_p = \beta_n \quad (\text{on} = \text{off})$$

$$\text{nmos: } V_{gsn} = V_{in} - V_D$$

$$V_{dsn} = V_{out}$$

$$\text{pmos: } V_{gsp} = V_{in} - V_{DD}$$

$$V_{dps} = V_{out} - V_{DD}$$



Cut-off Linear Saturation

$$\text{nmos: } V_{gsn} < V_{tn}$$

$$V_{gsn} > V_{tn}$$

$$V_{in} > V_{tn}$$

$$V_{dsn} < V_{gsn} - V_{tn}$$

$$V_{out} < V_{gsn} - V_{tn}$$

$$V_{gsn} > V_{tn}$$

$$V_{in} > V_{tn}$$

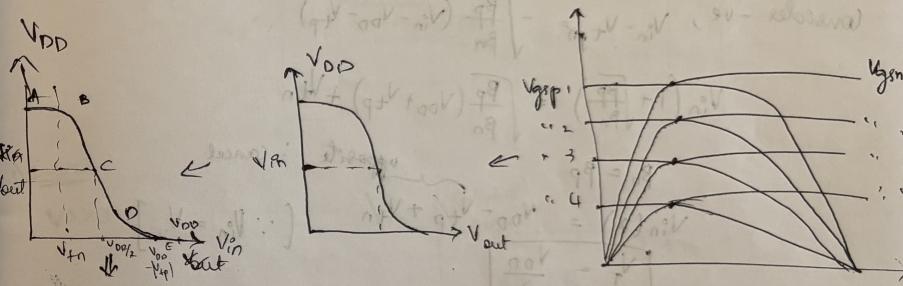
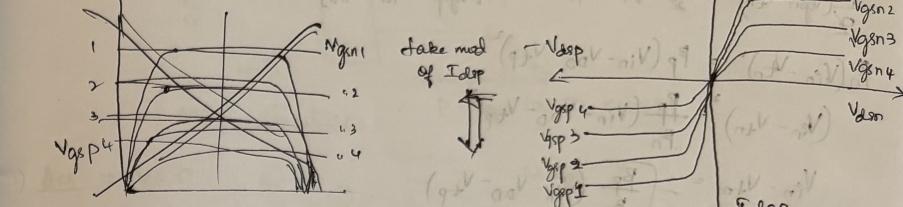
$$V_{dsn} > V_{gsn} - V_{tn}$$

$$V_{out} > V_{gsn} - V_{tn}$$

pmos: $V_{gsp} > V_{tp}$ $V_{gsp} < V_{tp}$
 $V_{in} - V_{DD} > V_{tp}$ $V_{in} - V_{DD} < V_{tp}$

$V_{dps} > V_{gsp} - V_{tp}$ $V_{dps} < V_{gsp} - V_{tp}$
 $V_{out} > V_{gsp} - V_{tp}$ $V_{out} < V_{gsp} - V_{tp}$

$I_{dsn} = I_{dps}$ $I_{dsn} = I_{dps}$
 $V_{gsp1} > V_{gsp2} > V_{gsp3} > V_{gsp4}$ $V_{gsp1} < V_{gsp2} < V_{gsp3} < V_{gsp4}$



Region Condition PMOS NMOS Vout.

A $0 < V_{in} < V_{tqn}$ Linear cut-off V_{DD}

B $V_{tp} < V_{in} < \frac{V_{DD}}{2}$ Linear saturation $V_{out} > \frac{V_{DD}}{2}$

C $V_{in} = \frac{V_{DD}}{2}$ Saturation " $V_{out} = \frac{V_{DD}}{2}$

D $\frac{V_{DD}}{2} < V_{in} < V_{tp}$ " linear $V_{out} < \frac{V_{DD}}{2}$

E $V_{DD} - V_{tp} < V_{in} < V_{DD}$ cut-off " " D

When both transistors are on, I is max.

I_{dsn}, I_{dps} \rightarrow this dissipates the I .
 \rightarrow should be $\boxed{0}$

V_T (switching threshold) (pt c in the diagram)

$$P_n = P_p \quad V_{in} = V_{out} = V_T.$$

$I_{Dn} = I_{Dp}$ (saturation)

$$\frac{P_n(V_{in} - V_{tn})^2}{\beta_n} = \frac{P_p(V_{gp} - V_{tp})^2}{\beta_p} \quad \begin{cases} V_{gp} = V_{in} \\ V_{tp} = V_{in} - V_{DD} \end{cases}$$

$$P_n(V_{in} - V_{tn})^2 = P_p(V_{in} - V_{DD} - V_{tp})^2$$

$$(V_{in} - V_{tn})^2 = \frac{P_p}{P_n} (V_{in} - V_{DD} - V_{tp})^2$$

$$V_{in} - V_{tn} = \pm \sqrt{\frac{P_p}{P_n} (V_{in} - V_{DD} - V_{tp})}$$

$$\text{(consider -ve), } V_{in} - V_{tn} = -\sqrt{\frac{P_p}{P_n} (V_{in} - V_{DD} - V_{tp})}$$

$$V_{in} \left(1 + \sqrt{\frac{P_p}{P_n}}\right) = \sqrt{\frac{P_p}{P_n} (V_{DD} + V_{tp})} + V_{tn}$$

$$P_n = P_p$$

$$V_{in}(2) = V_{DD} - V_{tp} + V_{tn} \quad (\because V_{in} = V_T)$$

$$V_T = \frac{V_{DD}}{2}$$

11/3/24 (Day 1)

Energy band gap.

n type / p type

E_{core} - conduction band

E_f - Fermi level

E_i - intrinsic

E_v - valence band

If E_f is near to E_v - n type.

" " towards E_f - p type.

In equi., E_f is always flat.

PN junction

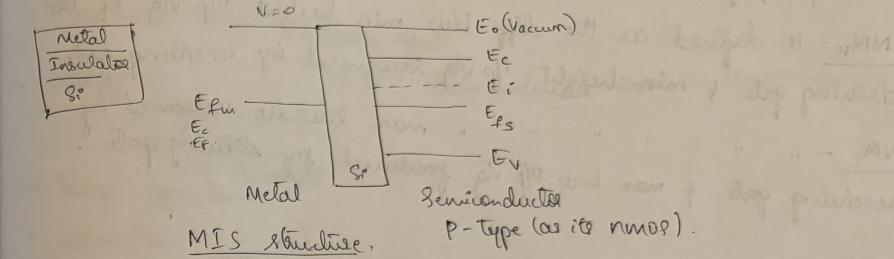


nmos

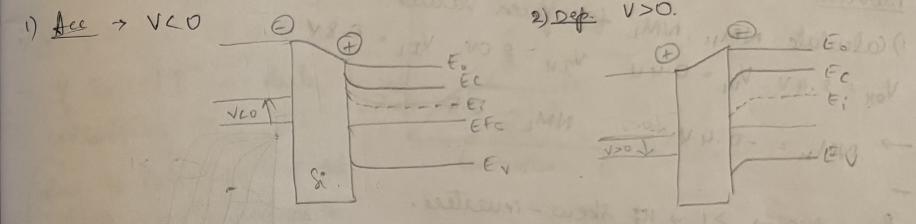
1) Accretion

2) Depletion

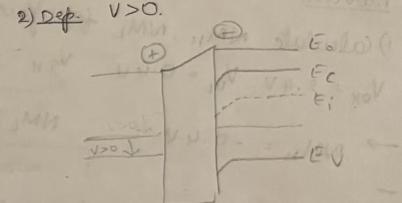
3) Inversion



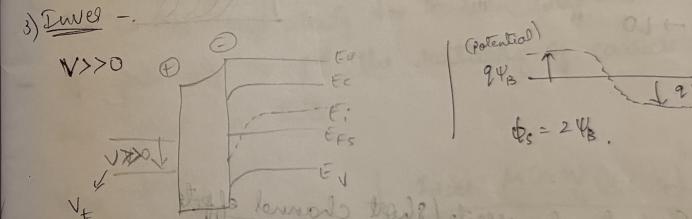
1) Acc $\rightarrow V < 0$



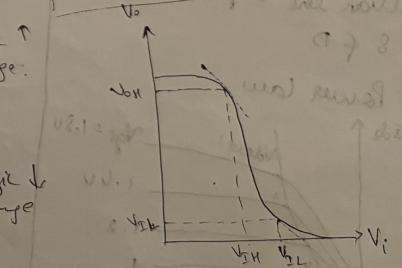
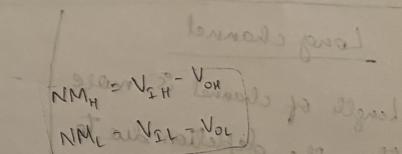
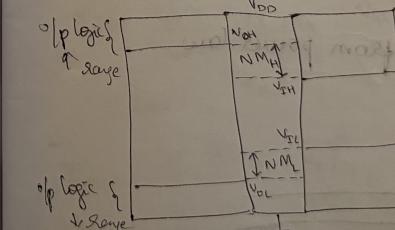
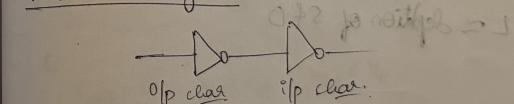
2) Dep $\rightarrow V > 0$



3) Inv



Noise Margin



NM - to determine allowable noise V_{TG} on i/p of gate, so that the o/p of gate is not corrupted.

NN_H - is defined as the diff b/w min height o/p V_{TG} of the driving gate & min height i/p V_{TG} recognised by receiving gate

NM_L - " " " " max low i/p recognised by receiving gate & max low o/p V_{TG} produced by driving gate.

Problem

i) calculate NM_H, NM_L for given values.

$$V_{OH} = 2.4V \quad V_{OL} = 0.4V \quad V_{IH} = 2.0V \quad V_{IL} = 0.8V$$

$$\rightarrow NM_H = -0.4V \quad NM_L = 0.4V$$

β/α ratio $\rightarrow > 1 \rightarrow HE$ skew-inverters.
 $\beta_n < 1 \rightarrow LO$ "

$$B = M \alpha \frac{W}{L}$$

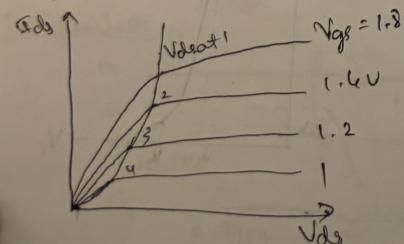
13/3/24

Non-ideal char / Second order effects / short channel effects

Long channel

- Length of channel is more than the depletion due to S & D

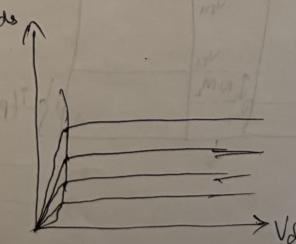
Power law



short channel

- $L \approx$ depletion of S & D

- Deviates from power law



- Velocity Saturation & mobility degradation.

- Channel length modulation (CLM)

- Threshold voltage

Body effect

- Leakage

Gate leakage

Junction threshold

- Temp. dependence

- Geometric " (critical EF)

-

ii) VS & MD $\rightarrow V = ME$

- If $V_{ds}(E) \uparrow^{\text{ex}}$, e starts collecting. \rightarrow in SC.

\downarrow due to this there'll be sat. called velocity saturation.

\downarrow due to this drift velocity \downarrow in turn I_{dsat} does.

- If gate V_{TG} is fed, the scattering of carriers occurs which does the I_{dsat} . \rightarrow MD.

$$V_{sat} = M E_{sat}$$

$$V = M \frac{E_{sat}}{1 + E_{sat}/E_{sat}} \Rightarrow \text{drift velocity.}$$

$$I_{dsat} = M \alpha \frac{W}{L} (V_{gs} - V_t)^2$$

$$* I_{ds} = \alpha \omega W (V_{gs} - V_t) V_{sat}$$

$I_{ds} = 0$ cut off $V_{gs} < V_t$

$I_{dsat} \frac{V_{ds}}{V_{sat}}$ linear $V_{gs} < V_{dsat}$

I_{dsat} sat $V_{gs} > V_{dsat}$

$$I_{dsat} = P_c \frac{\beta}{2} (V_{gs} - V_t)^{\alpha}$$

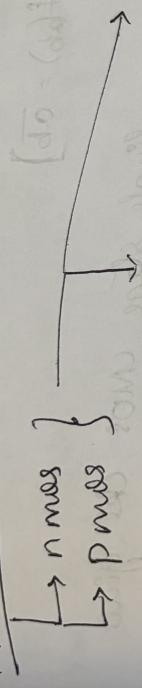
$$V_{dsat} = P_c (V_{gs} - V_t)^{1/2}$$

$\alpha = VS$ index.

Logic families -

- 1) RTL - resistor-transistor logic
- 2) DTL - diode ..
- 3) TTL - Transistor ..
- 4) ECL - emitter coupled ..
- 5) I²L / T²L - integrated injection logic
- 6) MOS - metal oxide semiconductor
- 7) CMOS - complementary ..

MOSFET - metal oxide semiconductor field - effect transistor



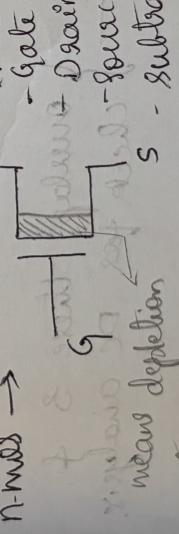
Enhancement type

- Normally off.
- Bias gate V_G is applied to turn on.
- Mostly used.
- Drain - source V_D is applied to conduct.

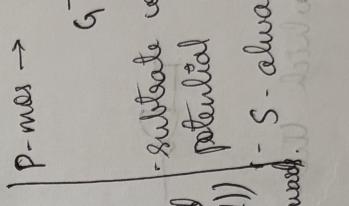
Depletion type

- Channel present
- called normally on V_D which means ready to conduct.
- Bias gate V_G is applied to turn off.

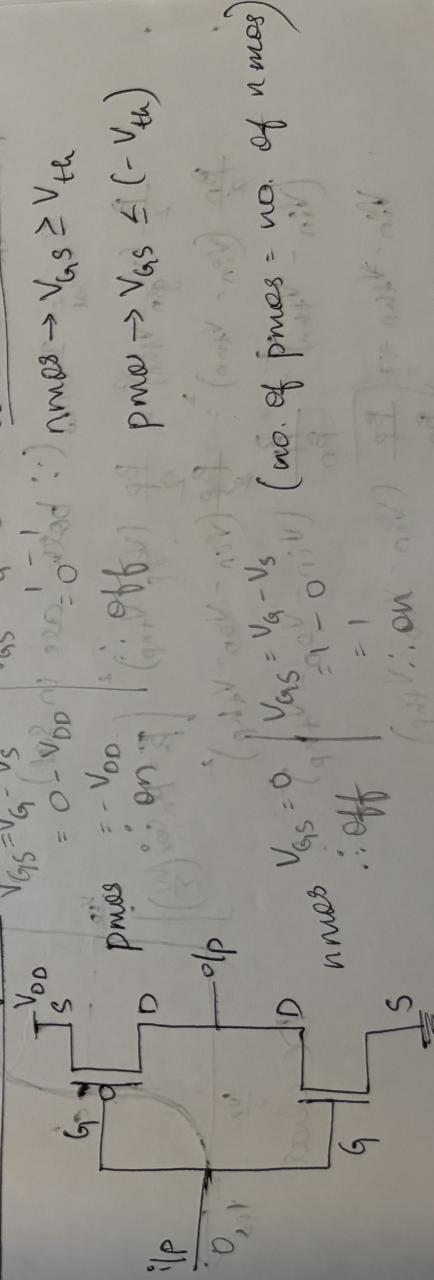
n-mos

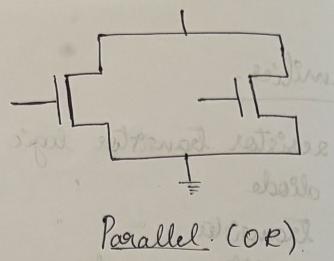
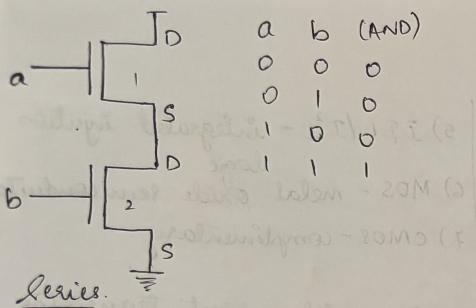


p-mos

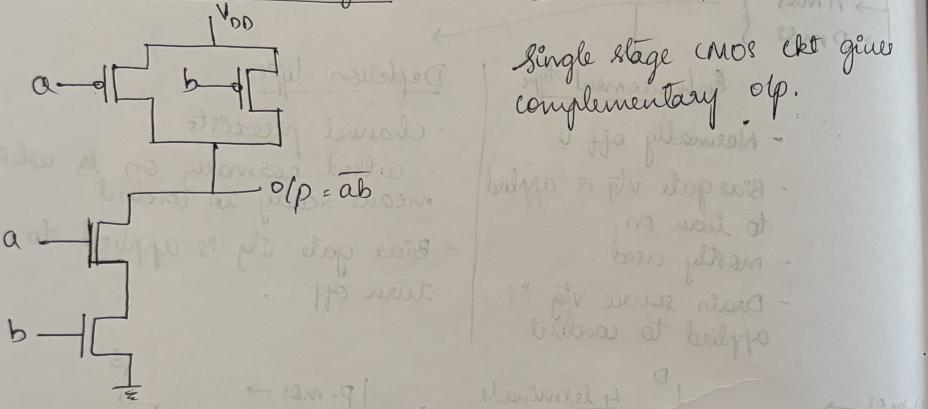


CMOS NOT gate





2 i/p CMOS NAND logic $[f(ab) = \bar{ab}]$



6/3/24.

At V_T , $V_{in} = V_{out} = V_T - 0$.
At V_T , $V_{in} = V_{out} = V_T - 0$.
At V_T , $V_{in} = V_{out} = V_T - 0$.

$I_{Dn_{sat}} = I_{Dp_{sat}}$ (\because both are in sat).

$$\frac{P_n}{2} (V_{gsn} - V_{thn})^2 = \frac{P_p}{2} (V_{gsp} - V_{thp})^2 \quad (P_n = P_p \cos(\frac{\pi}{c}))$$

$$\frac{P_n}{2} (V_{in} - V_{thn})^2 = \frac{P_p}{2} (V_{in} - V_{DD} - V_{thp})^2$$

$$(V_{in} - V_{thn})^2 = \frac{P_p}{P_n} (V_{in} - V_{DD} - V_{thp})^2$$

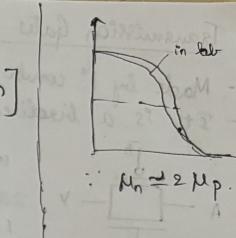
$$V_{in} - V_{thn} = \pm \sqrt{\frac{P_p}{P_n} (V_{in} - V_{DD} - V_{thp})}$$

$$V_{in} (1 + \sqrt{\frac{P_p}{P_n}}) = \sqrt{\frac{P_p}{P_n} (V_{DD} + V_{thp})} + V_{thn}$$

$$V_T = \frac{V_{DD} + V_{thp} + V_{thn}}{2}$$

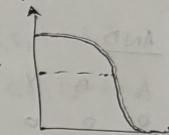
$$V_T = \frac{V_{DD}}{2}$$

$$[V_{thp} = -V_{thn}]$$



In order to make $J_n = J_p$, double the width of pmos.

Length cannot be changed as techs gets changed.
no. of carriers also \uparrow \therefore graph shifts to right.



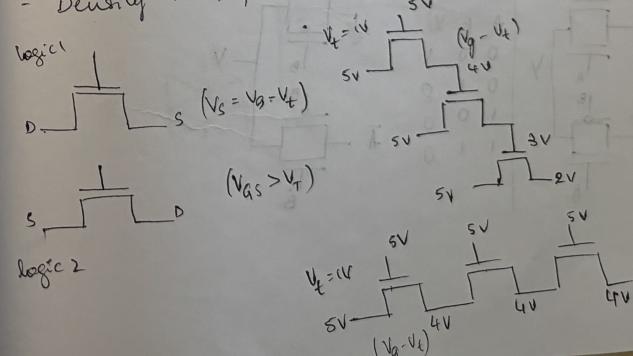
When we get the o/p with 1 i/p Bjt then why do we use diff op-amps?
(noise reduction)

$$\begin{aligned} & \text{in}_1 \xrightarrow{\text{BJT}} \text{O/P} \xrightarrow{\text{in}_1 + \text{in}_2} \text{O/P} \approx A(V_{in_1} \cup V_{in_2}) \\ & = A(V_{in_1} + V_{in_2} - V_{in_2} + V_{in_2}) \\ & = A(V_{in_1} - V_{in_2}) \end{aligned}$$

Diff blw oscillator & multivibrator.
 \downarrow L+ve f/b
only sinusoidal wf
non-sinusoidal wf.

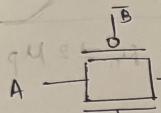
Pairs transistors:

- Either nmos or pmos.
- No. of tr. can be reduced.
- Density \uparrow , power \downarrow .



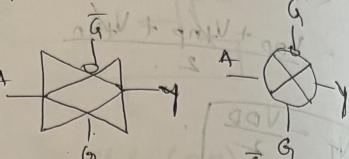
Transmission Gates

- Made by ^{the} combo of nmos & pmos.
- It is a bidirectional switch.



when $C=1 \quad A=B$
 $C=0 \quad A \neq B$

1 → nmos on
 0 → pmos on



when $C=1 \quad A=B$
 $C=0 \quad A \neq B$

AND

A

B

Y

0

0

0

0

1

1

1

A

B

Y

0

0

0

0

1

1

1

XNOR		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

OR

A

B

Y

0

0

1

1

1

A

B

Y

0

0

1

1

1

NAND

A

B

Y

0

0

1

1

0

A

B

Y

0

0

0

0

1

1

0

NOR

A

B

Y

1

1

0

0

0

1

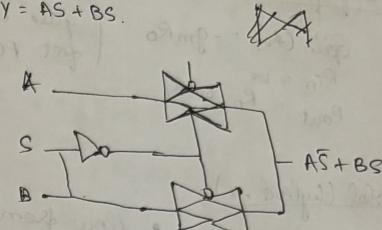
1

0

2:1 MUX

S	A	B	Y
0	1	0	A
0	0	1	B
1	0	1	$\bar{A} + B$

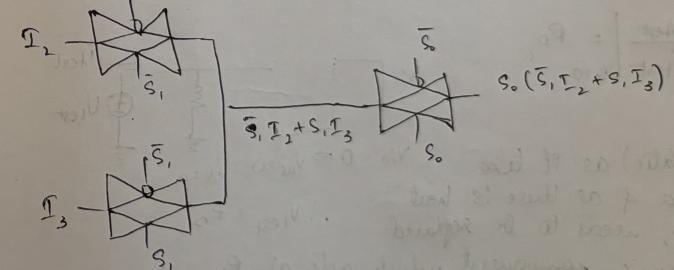
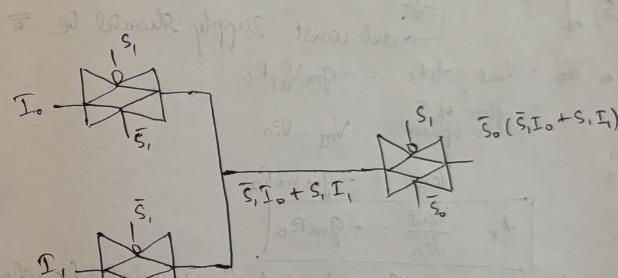
$$Y = \bar{A}\bar{S} + BS$$



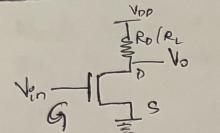
4:1 MUX

I ₀	I ₁	I ₂	I ₃	S ₁	S ₂	S ₃	Y
0	0	I ₀	I ₁	0	0	0	$\bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3$
0	1	I ₁	I ₂	0	1	0	$\bar{I}_0\bar{I}_1\bar{I}_2I_3$
1	0	I ₂	I ₃	1	0	1	$\bar{I}_0\bar{I}_1I_2\bar{I}_3$
1	1	I ₃	I ₀	1	1	1	$\bar{I}_0I_1\bar{I}_2\bar{I}_3$

$$Y = \bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3 + \bar{I}_0\bar{I}_1\bar{I}_2I_3 + I_0(\bar{I}_1\bar{I}_2 + I_2\bar{I}_3)$$



Common Source Amplifier.



$$\text{Gain } (A_v) = -g_m R_D$$

$$R_{in} = \infty$$

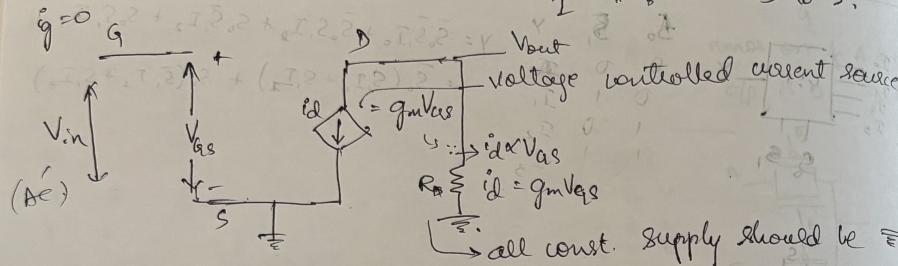
$$R_{out} = R_D \text{ or } R_L$$

gate current is zero
for FETs.

Small signal model (hybrid pi).

i_s flow from S to D.

$I_D = g_m V_{DS}$



$$A_v = \frac{V_{out}}{V_{in}} \quad \& \quad V_{RD} = V_{out} - i_d R_D = -g_m V_{AS} R_D$$

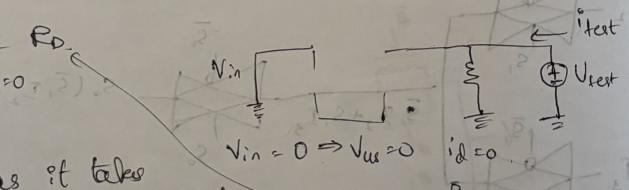
($I_D + i_s$) is upscale. $V_{AS} = V_{in}$

$$R_{in} = \frac{V_{in}}{I_{in}} = \infty$$

$$A_v = \frac{V_{out}}{V_{in}} = -g_m R_D$$

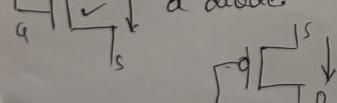
As V_{tg} at source \uparrow , I flow via gate ext. the insulator (oxide layer) resistance the I. $\therefore R_{tg} = 0$. \therefore no I blowing & S.

$$R_{out} = \frac{V_{test}}{i_{test}} \quad | \quad i_{test} (V_{in}=0) = R_D$$



- Resistor (static) as it takes more area & as there is heat dissipation, needs to be replaced by a dynamic component which acts at R_o .

now its 2 terminal op of a diode.



$$A_v = -g_m R_D$$

$$g_m = \frac{2 N_s C_{ox} (W/L) I_D}{q W^2}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$= \frac{2 N_s C_{ox} (W/L) I_D}{2 N_p C_{ox} (W/L) I_D}$$

$$i_{d1} = i_{d2}, \quad N_n \approx 2 N_p$$

$$= - \frac{2 N_p C_{ox} (W/L) I_D}{2 N_p C_{ox} (W/L) I_D}$$

$$A_v = - \sqrt{\frac{2 C_{ox} (W/L)_1}{C_{ox} (W/L)_2}}$$

$$\boxed{\frac{A_v^2}{2} = \frac{(W/L)_1}{(W/L)_2}}$$

$$A_v \approx 0$$

$$\frac{(10)^2}{2} = \frac{(W/L)_1}{(W/L)_2}$$

$$\text{Let } (W/L)_1 = \frac{10}{1}$$

$$(W/L)_2 = 80 = \frac{10}{5} = \frac{1}{5} = \frac{2}{25}$$

$$V_o = -A_v V_{in} \quad (V_{in} = 2 \text{ mV}) \\ = -10 \times -2 \text{ mV} \\ V_o = 20 \text{ mV} \text{ (out of phase)}$$