EC630 08/03/2022

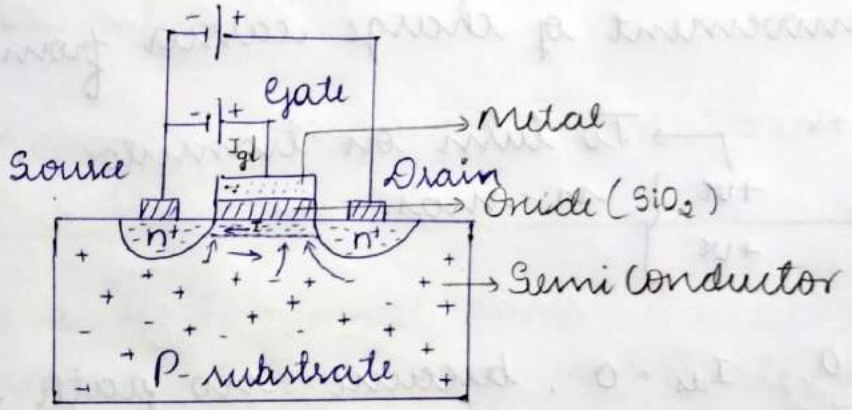
CMOS VLSI CIRCUITS

Logic families :

1. DTL - Diode transistor logic
2. RTL - Resistor transistor logic
3. TTL - Transistor transistor logic
4. ECL - Emitter couple logic
5. IIL / I^2L - Inverse injection logic
6. MOS - Metal oxide semiconductor
7. CMOS - Complementary metal oxide semiconductor.

Advantages of MOS over BJT :

* We can't reduce the size of BJT, but its possible in MOS
* We can consider any of the region in substrate as source or drain. but its n't possible in BJT



Current → D→S
Charge carrier → S→D

Cross-sectional view of MOSFET (N-MOS)

MOSFET
- n-channel mosfet (n-mos)
  - Enhancement type
  - Depletion type
- p-channel mosfet (p-mos)
  - Enhancement type
  - Depletion type

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Enhancement type:

* Establishing the channel by applying gate voltage (V_{gs}) is known as Enhancement
* Normally OFF transistor.

Depletion type

* Channel already exist
* Normally ON transistor

* After applying the gate voltage (V_{gs}) opposite charge carrier will starts to move towards the oxide layer ~~and Transistor switches from OFF to ON.~~
* Channel will be created
* Transistor switches from OFF to ON.

Transistor ON means * Its ready to conduct (No conduction)

* Because no movement of charge carrier from S → D.
* $I_{ds} = 0$

→ To turn on transistor

$V_{gs} = V_g - V_s$ +ve } n-mos
$V_{ds} = V_d - V_s$ +ve

when $V_{ds} = 0$, $I_{ds} = 0$, because no path to travel for charge carrier

$I_{ds} \propto V_{ds}$

and also depends on V_{gs} (Indirectly)

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$V_{gs} \geq V_{th}$, n-mos-ON.

i. If $V_{ds} = 0$, $I_{ds} = 0$

ii If $V_{ds} > 0$ $I_{ds} > 0$

iii $V_{gs} = 0$, $V_{ds} > 0 \Rightarrow I_{ds} = 0$ (because N-mos is OFF. means, no channel created, No movement of charge

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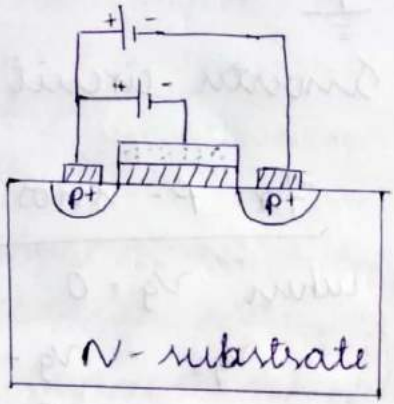
carrier from source to drain).

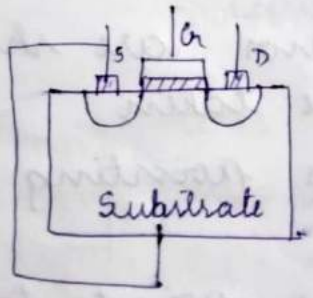
* Even V_{gs} is +ve, gate current (I_g) is always zero because oxide acts as barrier to gate current.
∴ MOS is a "voltage controlled device"

p-channel mosfet (P-MOS)



N-MOS : $V_{gs} \geq \lvert V_{th\,n} \rvert$ (+ve)	→ Transistor is ON
P-MOS : $V_{gs} \leq \lvert V_{th\,p} \rvert$ (-ve)	→ Transistor is ON

* MOS is a 4-terminal device
Gate, source, drain and substrate / Body
* Substrate is always connected to source.



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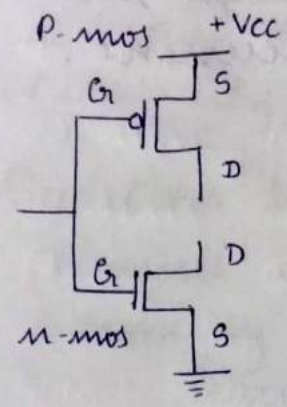
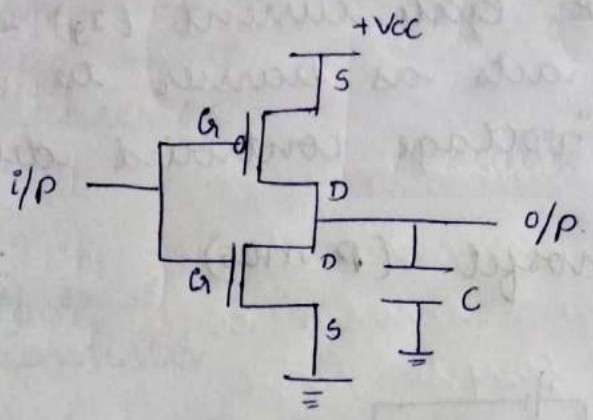
CMOS :





CMOS / Inverter circuit

For n-mos

* when $V_{gs} = +ve$
  ($V_g = 0$)

$V_{gs} = V_g - V_s$
$= 0 - 0$
$= 0$

n-mos is OFF

* when $V_g = +V_{cc}$

$V_{gs} = V_g - V_s$
$= +V_{cc} - 0$

$V_{gs} = +V_{cc}$

n-mos is ON

For p-mos : $V_{gs} = -ve$

* when $V_g = 0$

$V_{gs} = V_g - V_s$
$= 0 - (+V_{cc})$

$V_{gs} = -V_{cc}$

p-mos is ON

* when $V_g = +V_{cc}$

$V_{gs} = V_g - V_s$
$= +V_{cc} - (+V_{cc})$

$V_{gs} = 0$

p-mos is OFF.

Observation from CMOS Circuit :

* Drain of p-mos and n-mos are shorted and across which output will be taken
* Source of p-mos is always pointing to upward and given to $+V_{cc}$
* Source of n-mos is always points to Downward and given to ground.

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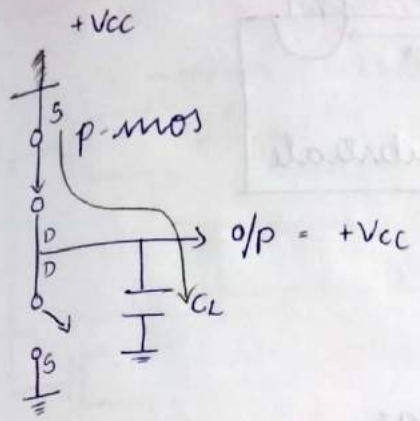
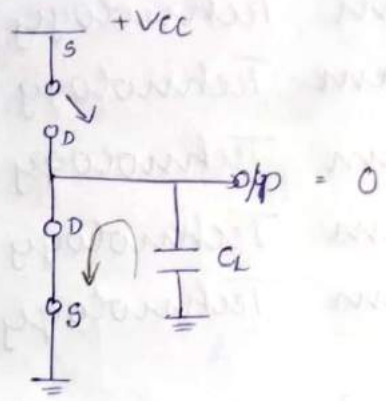
i. for '0' input



* p-mos is ON
* n-mos is OFF
* p-mos voltage (+Vcc) ~~will move~~ across the capacitor
* Charging of Capacitor takes place

ii for '1' input



* P-mos is OFF
* n-mos is ON
* Discharging of capacitor takes place.

TT of single stage CMOS circuit

Vin	Vout
0	1
1	0

$RC = \tau$ (Time constant)

C ~~is~~ constant

as $R \uparrow$, $\tau \uparrow$ $\Rightarrow$ Takes more time to charge or discharge.

* Analyzing of n-mos is completely opposite to p-mos or, o/p of single stage CMOS circuit is compliment. hence the name Complementary metal oxide semiconductor.

* for n-mos $\rightarrow$ e^- moves from $S \rightarrow D$
  current move from $D \rightarrow S$, $I_{ds} = +ve$

* for p-mos $\rightarrow$ holes from $S \rightarrow D$
  Current move from $S \rightarrow D$
  $\therefore$ $I_{sd} = +ve$ or $I_{ds} = -ve$

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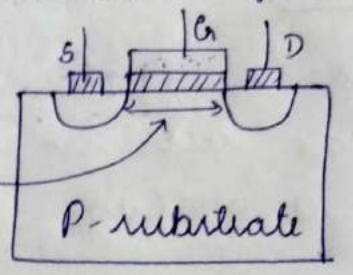
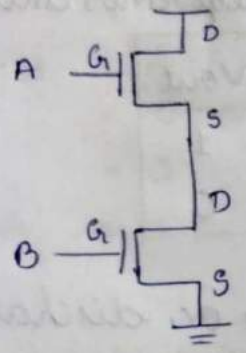
180 nm Technology
90 nm Technology
45 nm Technology
22 nm Technology
14 nm Technology
7 nm Technology

→ Channel length



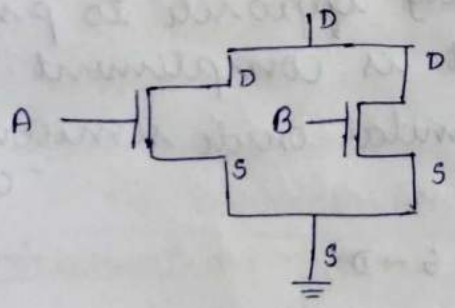
SEM - Scanning electron microscope - 100nm
TEM - Travelling electron microscope - 1nm

* when n-mos are connected in series → AND logic

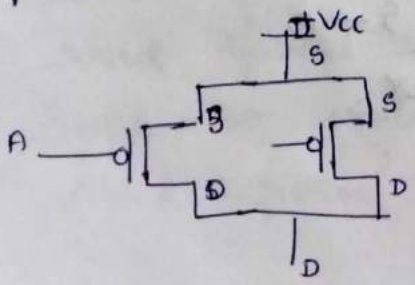


A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

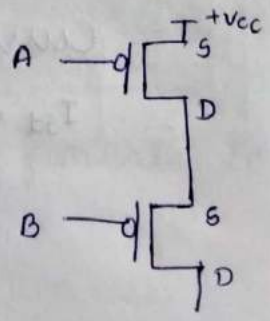
* n-mos connected in parallel - OR logic (A+B)



* P-mos connected in parallel → AND logic



* P-mos connected in series → OR logic



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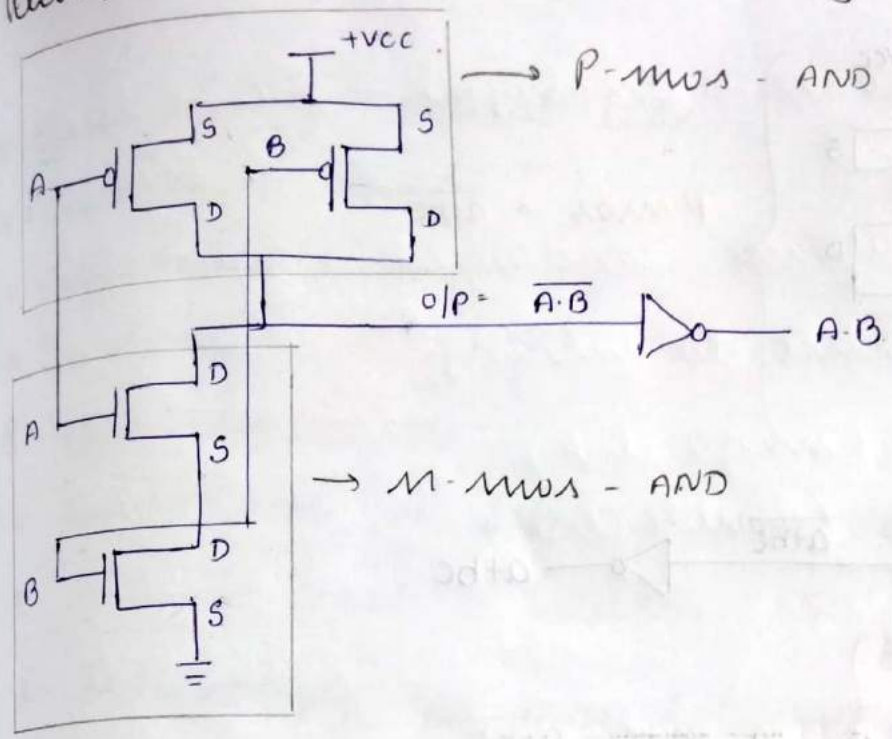
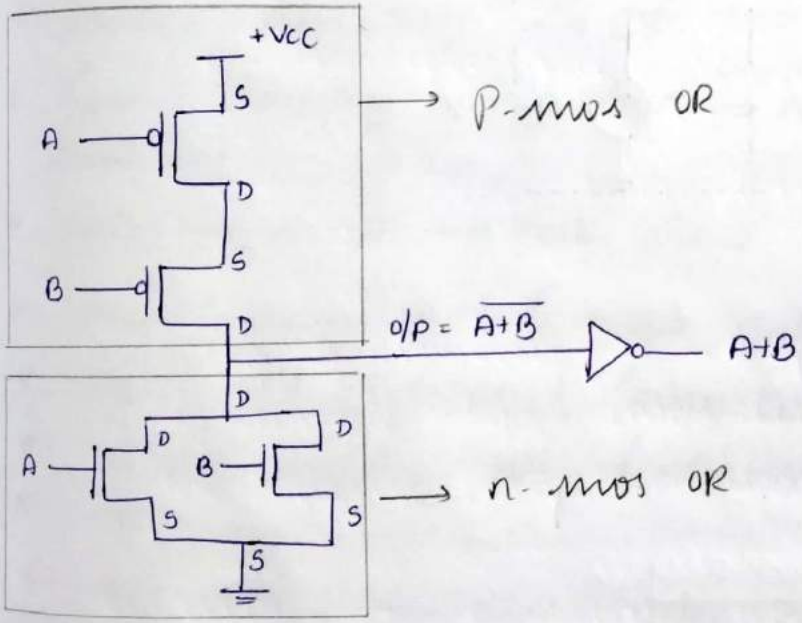
Realization of AND (A*B) using CMOS circuit



Realization of OR (A+B) using CMOS circuit



Disadvantage of CMOS :

* No. of transistor required → more.

Advantage :

* Gives flexibility in analyzing the circuit

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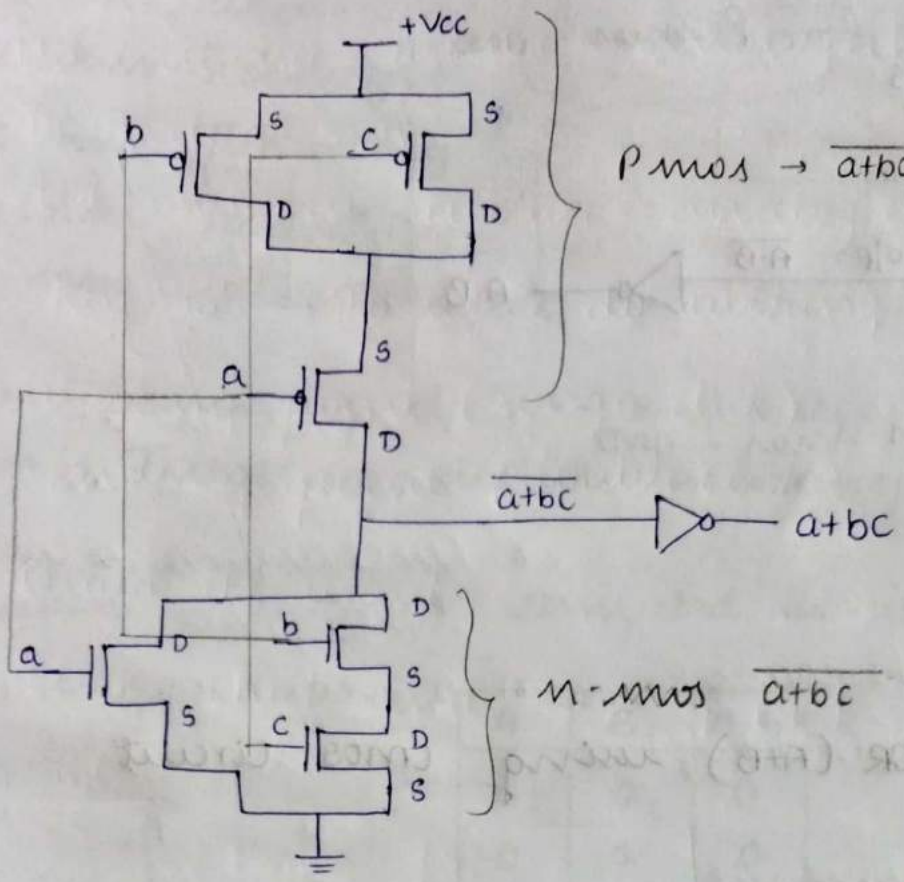
Realize, $f(a, b, c) = a + bc$ using cmos circuit



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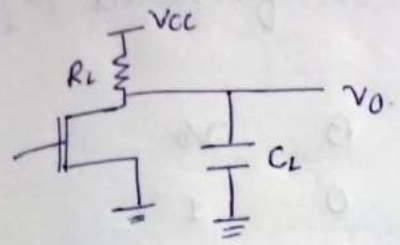
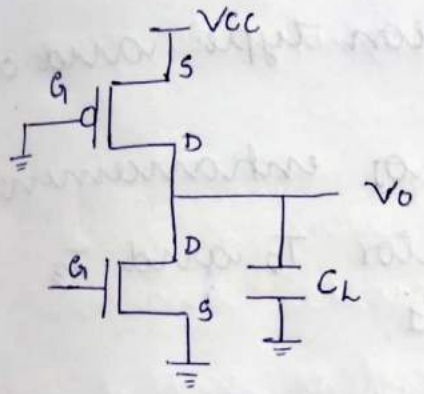
n-mos inverter using active device.



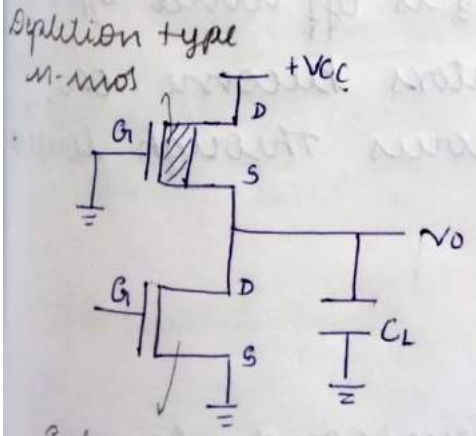
Inverter using passive device:

i. Using p-mos as load



* When $V_{GS} = 0$, p-mos is always on
* It acts as load.
* When i/p = 1, forms closed circuit, and o/p = 0.
* When i/p = 0, forms open ckt and o/p = 1.

ii Using depletion n-mos as load:



* In depletion type n-mos channel already exist (Normally ON Transistor).
* Therefore gate should be grounded.
* It acts as load.

* Depletion type n-mos = enhancement type p mos with gate voltage = 0.

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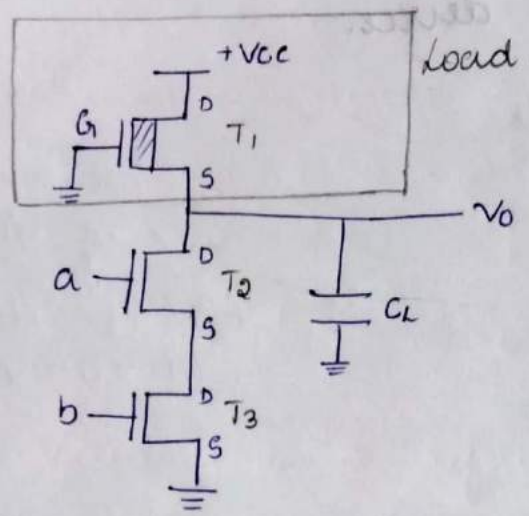
Realization of two input NAND gate using n-mos



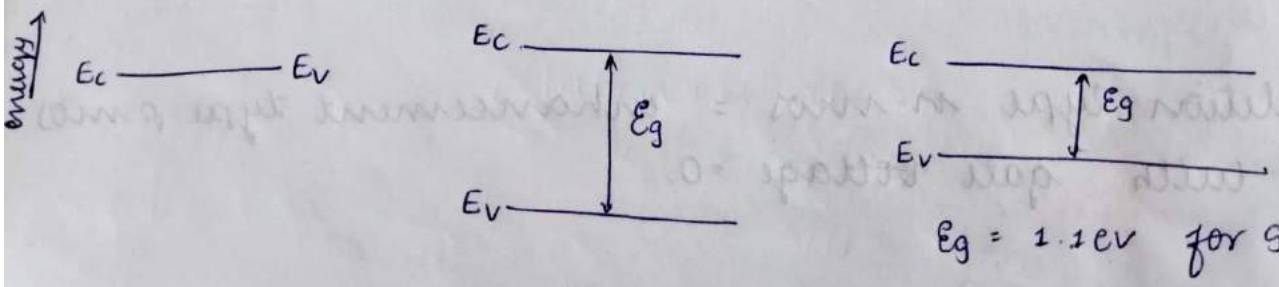
* No. of mos for load = 1.

A	B	V_0
0	0	1
0	1	1
1	0	1
1	1	0

* n-mos transistor T_1 is of deplition type and acts as load.
* n-mos transistor T_2 and T_3 are of enhancement type
* when a = b = 0, both the transistor T_2 and T_3 remains off and output $V_0 = 1$.
* when a = 0, b = 1, Transistor T_2 is off and T_3 is on and output $V_0 = 1$.
* when a = 1, b = 0, T_2 is on and T_3 is off and o/p = 1
* when a = b = 1, Both the Transistors become on, forms a closed circuit, voltage flows through low resistance and output $V_0 = 0$.

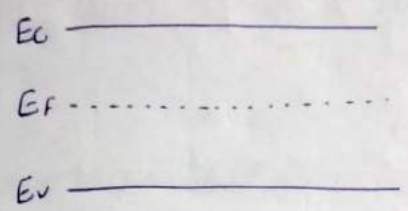
Energy band diagram :

Conductor Insulator Semiconductor

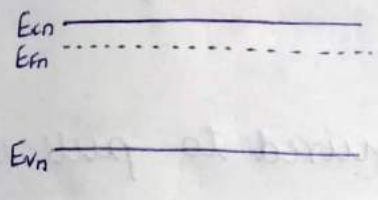


E_g = 1.1 eV for Si.

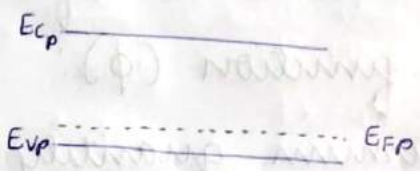
* For pure semiconductor, fermi level lies exactly in the centre between E_c and E_v.

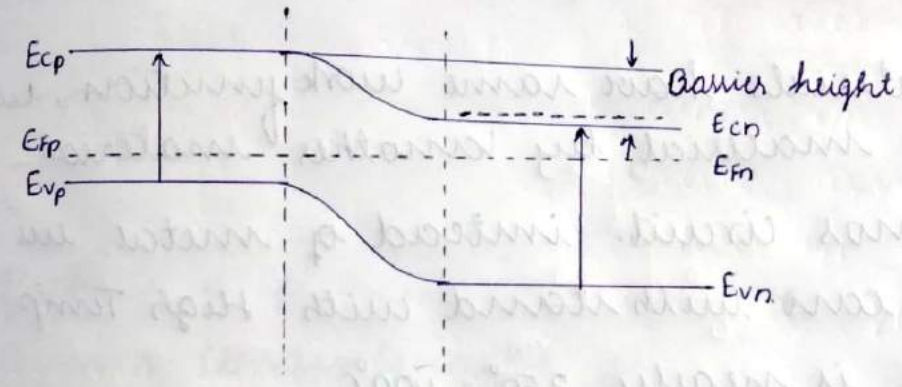


n - type



P- type

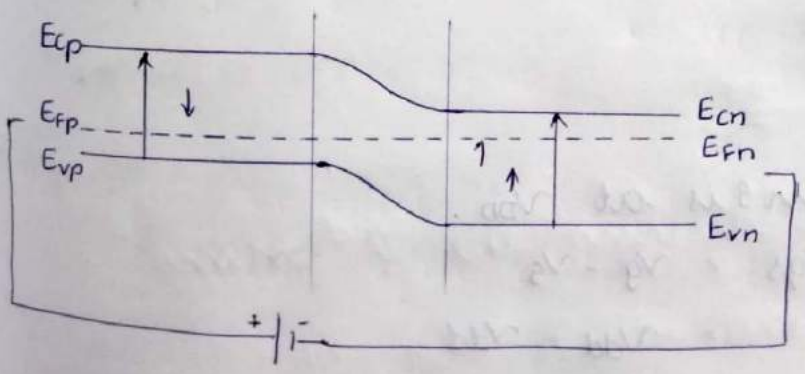




Unbias condition

* In unbias condition, Energy level E_f will be allign and becomes straight.

Forward bias:



* Majority charge carrier in n type goes to p and barrier height will decreases.

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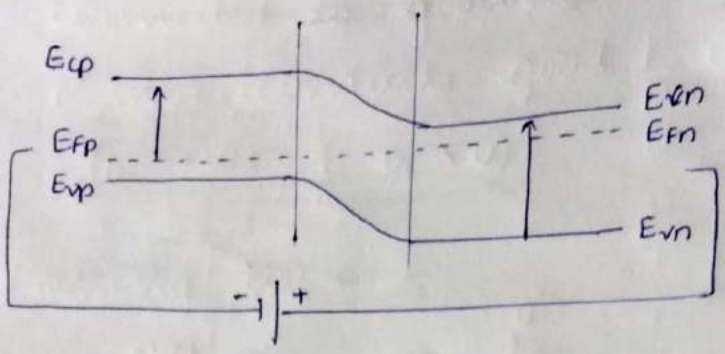
Reverse bias :

* barrier height will



* Vacuum is a reference with zero eV (0eV)

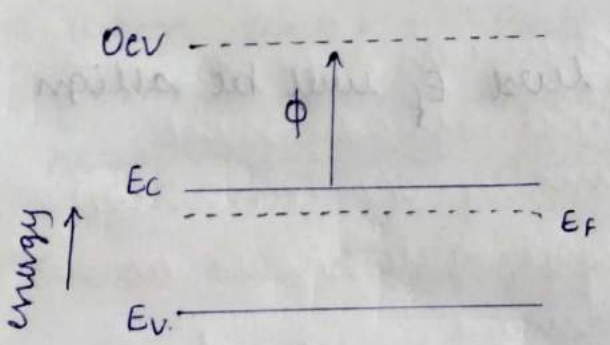
Work function (ϕ):

* Minimum quantity of energy required to pull the e^- from surface of the metal.

* when two materials have same work function, we can replace one material by another material.

* Therefore, in mos circuit instead of metal, we use polysilicon (It can withstand with High Temp.)

* M.P. of metal is nearly 350° - 400°C.



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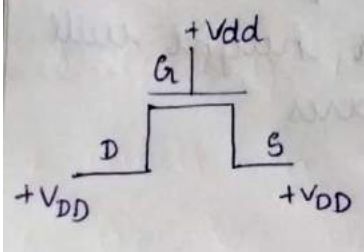


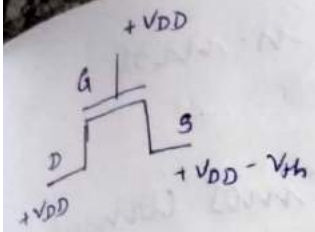
i. when S is at V_{DD}.

$V_{gs} = V_g - V_s$

$= V_{dd} - V_{dd}$

$= 0$.

n-mos is off.

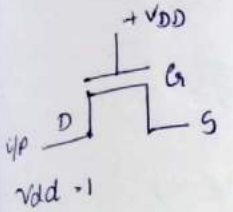


ii When S is at $V_{DD} - V_{th}$

$$V_{gs} = V_g - V_s$$
$$= V_{DD} - V_{DD} + V_{th}$$
$$= V_{th}$$

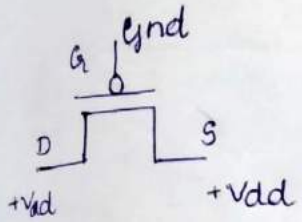
n-mos is ON.

Pass-transistor:



o/p $V_{DD} - V_{th}$ < 1.

* when i/p = 1, we will get o/p < 1.
* ∴ n-mos conducts bad 1.



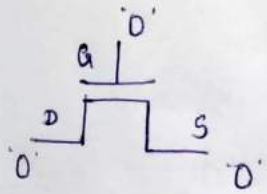
$V_{gs} = -ve$ for p-mos.

$$V_{gs} = V_g - V_s$$
$$= 0 - V_{dd}$$
$$V_{gs} = -V_{dd}$$

P-mos is ON.

if gate of p-mos connected to ground
* P-mos conducts good 1.

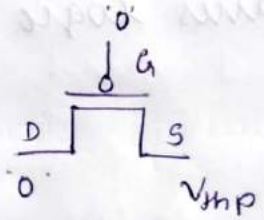
i.



$$V_{gs} = V_g - V_s$$
$$= 0 - 0$$
$$= 0.$$

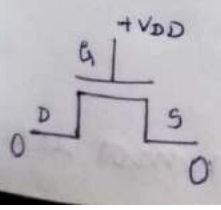
P-mos is OFF

ii.



$$V_{gs} = V_g - V_s$$
$$= 0 - V_{thp}$$
$$V_{gs} = -V_{thp}$$

* if i/p = 0V, ⟶ o/p is some +ve value.
∴ P-mos conducts bad zero.



$$V_{gs} = V_g - V_s$$
$$= V_{DD} - 0$$
$$= +V_{DD}$$

n-mos is ON
n-mos conducts good '0'

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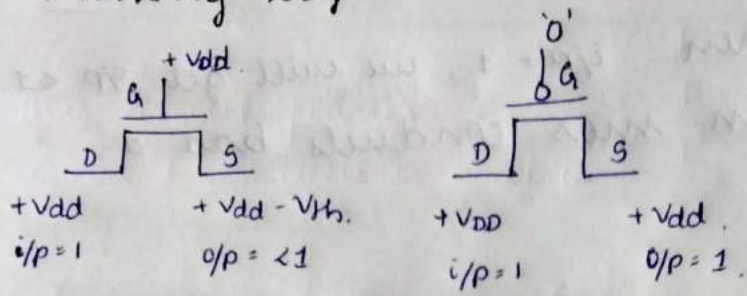
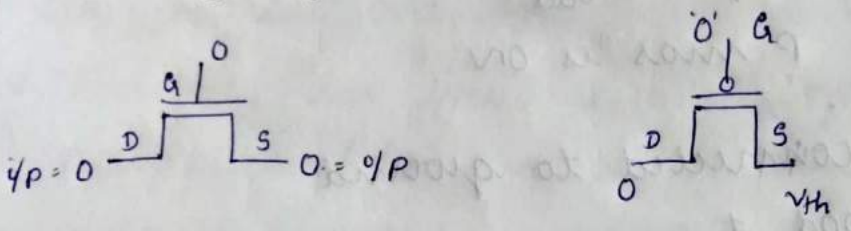
* n-mos conducts good 0, when S of n-mos connected to ground. (G → +V_{DD})
* p-mos conducts good 1, when S of p-mos connect. to +Vdd (G → 0)

Passing logic 1 :



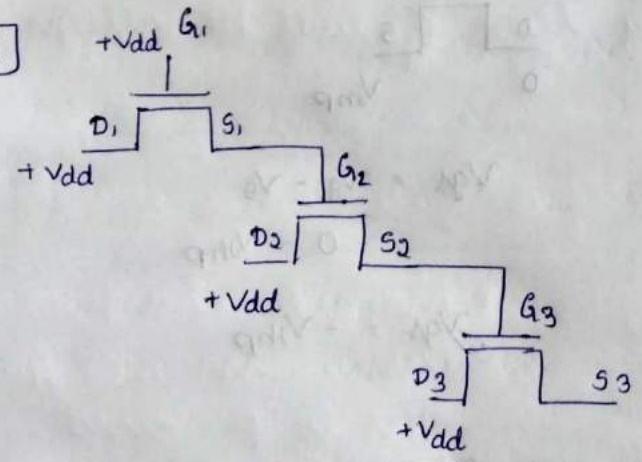
* p-mos passes logic 1 in proper way.

Passing logic 0 :



* n-mos passes logic 0 in proper way.

i]



* Gate of 1st n-mos is driving the 2nd n-mos.
* when G_1 = +Vdd, D_1 = +Vdd ⇒ S_1 = $V_{dd} - V_{th}$.
* G_2 = $V_{dd} - V_{th}$, D_2 = V_{dd},

Assume, S_2 = Vdd, V_{gs} = $V_{dd} - V_{th} - V_{dd} = -V_{th}$, n mos is OFF

$V_{gs} = V_g - V_S$

* $= V_{dd} - V_{th} - V_{dd} + 2V_{th}$

$V_{gs} = V_{th}$ (n-mos is ON)

$\boxed{S_2 = V_{dd} - 2V_{th}}$

* assume, $S_2 = V_{dd} - V_{th}$

$V_{gs} = V_g - V_S$

$= V_{dd} - V_{th} - V_{dd} + V_{th}$

$V_{gs} = 0$.

n-mos is OFF.

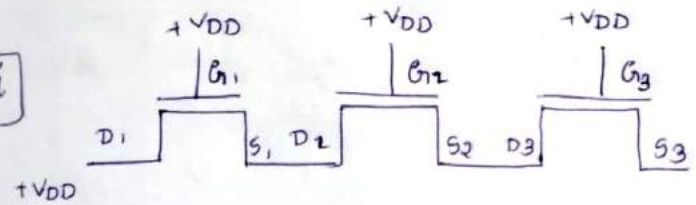
$V_{gs} = V_g - V_S$

* $= V_{dd} - 2V_{th} - V_{dd} + 3V_{th}$

$V_{gs} = V_{th}$

$\boxed{S_3 = V_{dd} - 3V_{th}}$.

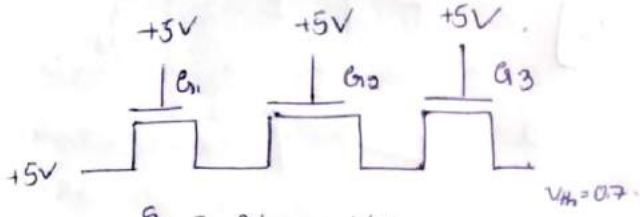
ii]



$S_1 = V_{DD} - V_{th}$.

$S_2 = V_{DD} - V_{th}$.

$S_3 = V_{DD} - V_{th}$.

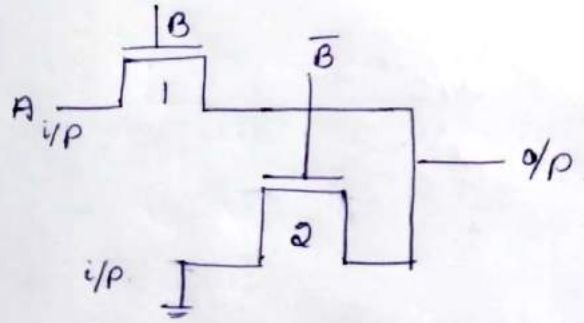


$S_1 = V_{DD} - V_{th}$

$= 5 - 0.7$.

$S_1 = S_2 = S_3 = 4.3V$

Realization of AND logic using pass-transistor:



A	B	o/p
0	0	0
0	1	0
1	0	0
1	1	1

* when $A = B = 0$, T_1 is OFF and T_2 is ON, but the i/p is grounded, $\Rightarrow$ o/p = 0
* when $A = 0$, $B = 1$, T_1 is ON and T_2 is OFF, but the i/p = 0 $\Rightarrow$ o/p = 0.
* when $A = 1$, $B = 0$, T_1 is OFF, and T_2 is ON, i/p = 0 $\Rightarrow$ o/p = 0
* when $A = B = 1$, T_1 is ON and T_2 is OFF, i/p = 1 $\Rightarrow$ o/p = 1 (n-mos conducts good 1)

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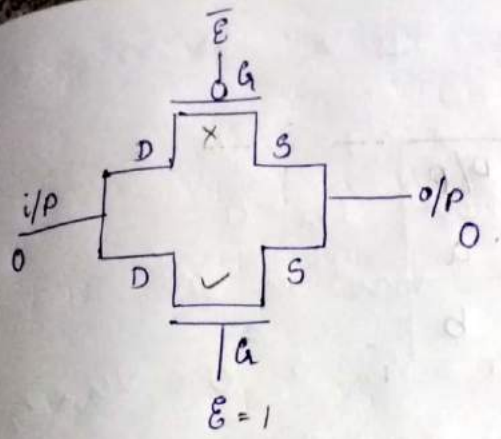
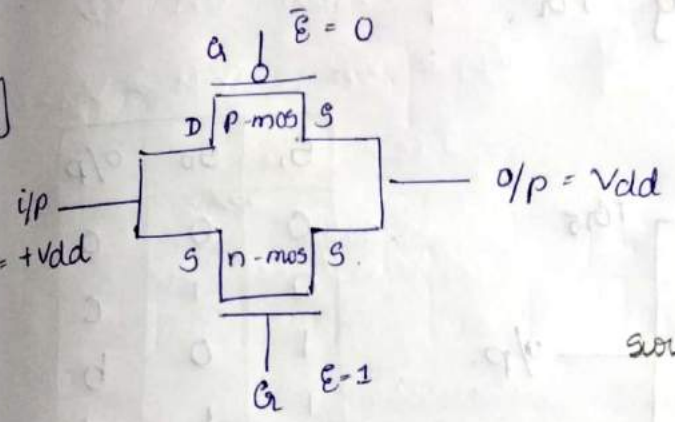
i]



This circuit passes good 1 as well as good 0.

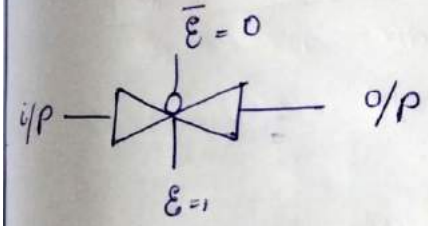
when the circuit is enabled.

ii]



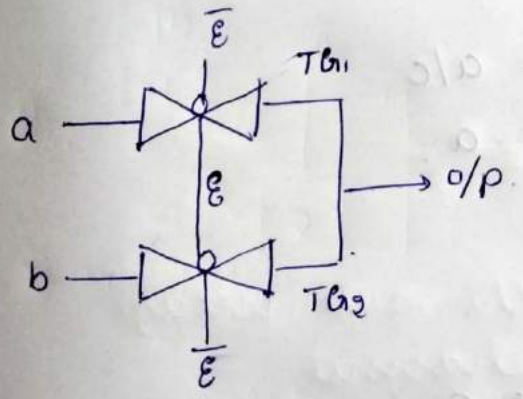
n-mos → off
p-mos → ON

* Source of n-mos becomes Vdd due to the source force of p-mos.



* 1 is transmitted by p-mos.
0 is transmitted by n-mos.

∴ This circuit passes good 1 and as well as good 0.



a	b	ε	TG_1	TG_2	o/p
0	0	0	×	✓	b = 0
0	0	1	✓	×	a = 0
0	1	0	×	✓	b = 1
0	1	1	✓	×	a = 0
1	0	0	×	✓	b = 0
1	0	1	✓	×	a = 1
1	1	0	×	✓	b = 1
1	1	1	✓	×	a = 1

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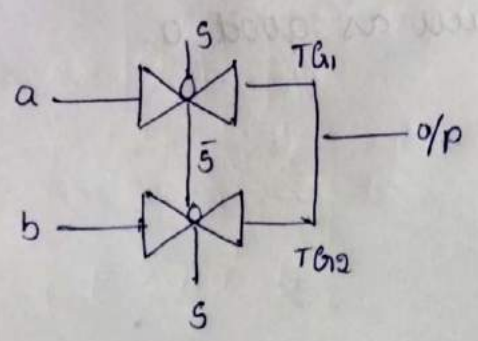
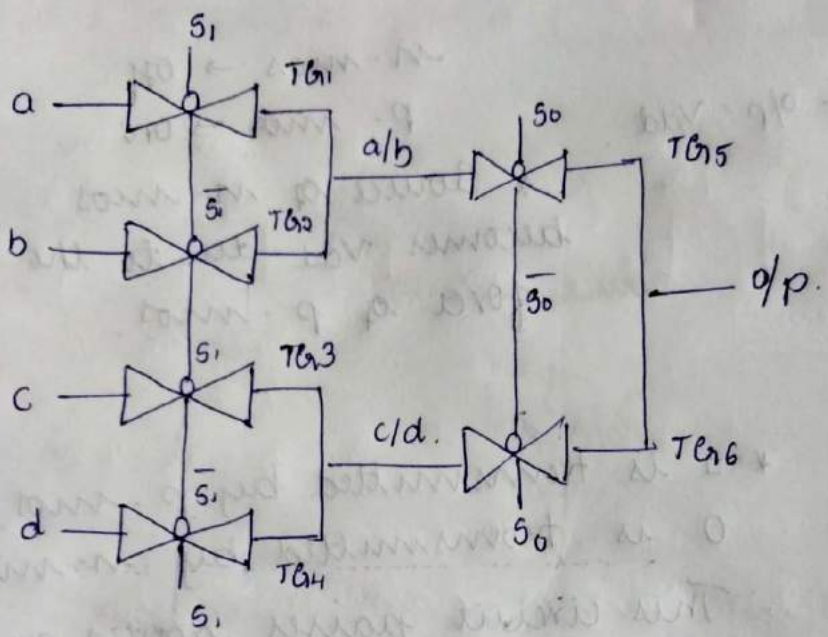
Construct 2:1 mux using TG.



S	o/p
0	a
1	b

Construct 4:1 mux using TG.



S_1	S_0	o/p
0	0	a
0	1	c
1	0	b
1	1	d

* when $S_1 = 0$ and $S_0 = 0$,

$S_1 = 0 \Rightarrow$ TG1 and TG3 are ON, $o/p_1 = a/c$.

$S_0 = 0 \rightarrow$ TG5 is ON $\Rightarrow$ $o/p = a$.

* when $S_1 = 0$ and $S_0 = 1$.

$S_1 = 0 \Rightarrow o/p_1 = a/c$.

$S_0 = 1 \Rightarrow$ TG6 is ON $\Rightarrow o/p = c$.

* when $S_1 = 1$ and $S_0 = 0$.

$S_1 = 1 \Rightarrow$ TG2 and TG4 becomes ON $\Rightarrow o/p_1 = b/d$

$S_0 = 0 \Rightarrow$ TG5 is ON $\Rightarrow o/p = b$.

* when $S_1 = 1 = S_0$

$S_1 = 1 \Rightarrow o/p_1 = b/d$

$S_0 = 1 \Rightarrow$ TG6 is ON $\Rightarrow o/p = d$

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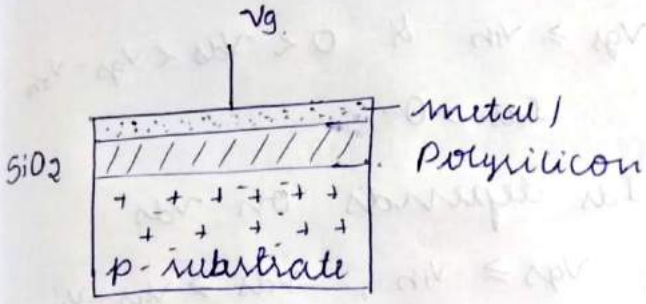
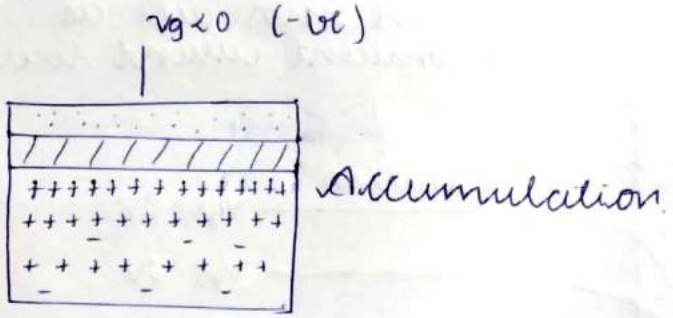
* If S_1 and S_2 are interchanged, o/p = a, b, c, d.

16/03/2022

n-mos :

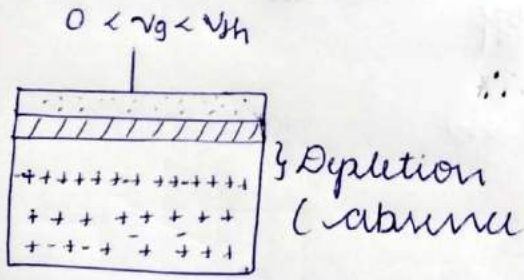


i. if $V_g < 0$



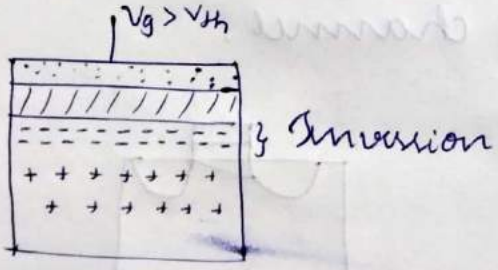
* Accumulation of +ve charge carrier (holes) near the oxide layer.

ii. $0 < V_g < V_{th}$



* Due to small +ve gate volt. (V_{th}) holes are starts to movedown & some of the e^- starts to move up.
∴ Space is created near the oxide layer called as depletion region

iii $V_g > V_{th}$



* Holes are completely replaced by e^-s
* Channel is created (enhancement)

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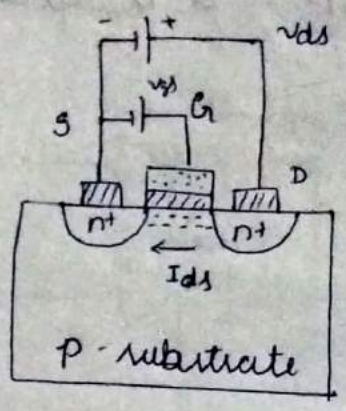


i. $v_{gs} = 0$, $I_{ds} = 0$, n-mos is off

ii If $v_{gs} \geq v_{th}$, $v_{ds} = 0$

then, $I_{ds} = 0$

n-mos is on

iii. If $v_{gs} \geq v_{th}$ & $0 < v_{ds} < v_{gs} - v_{th}$

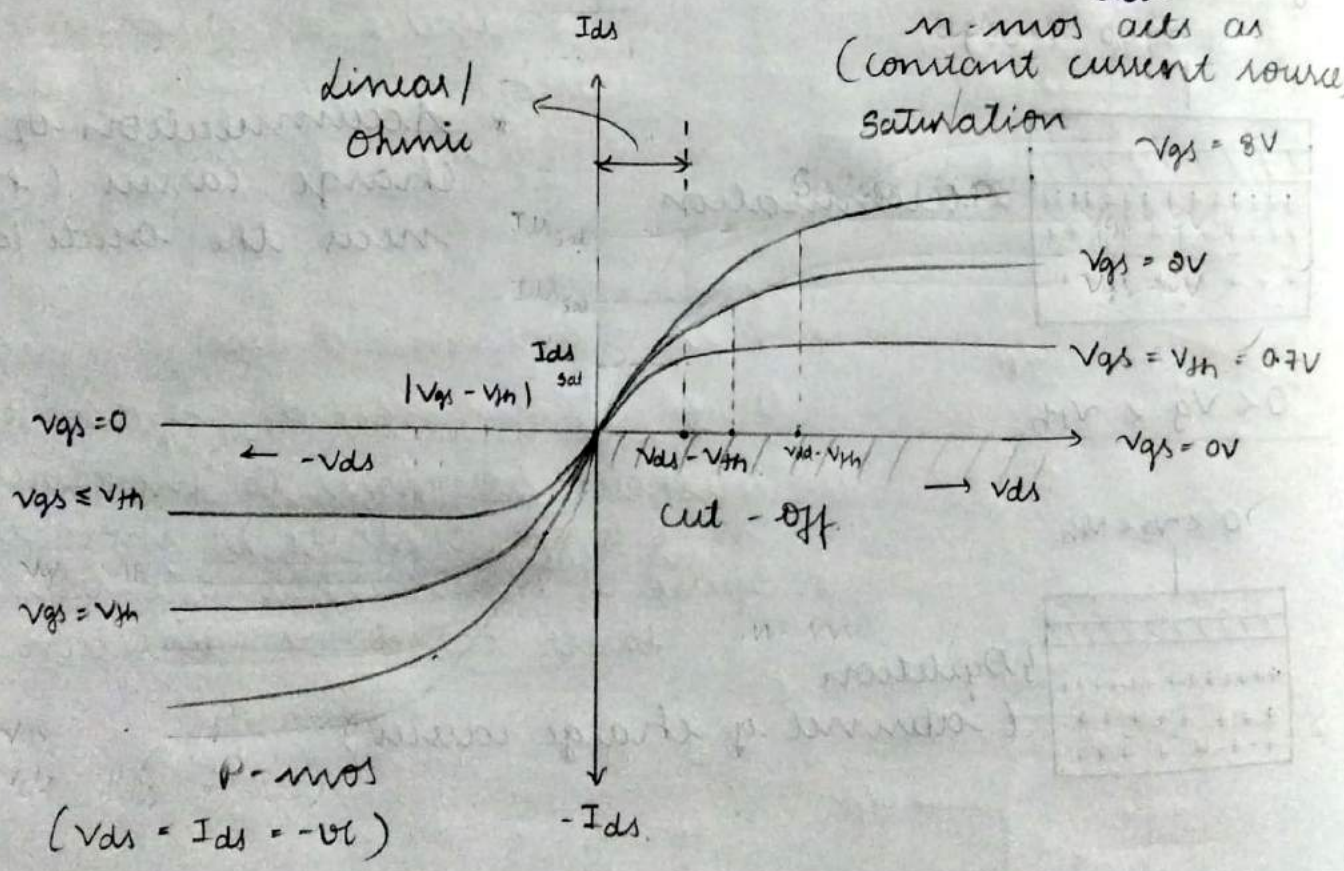
$I_{ds} > 0$.

I_{ds} depends on v_{ds}

iv. If $v_{gs} \geq v_{th}$, $v_{ds} \geq v_{gs} - v_{th}$

$I_{ds} = I_{ds\,sat.}$

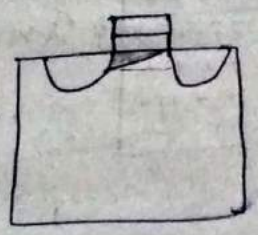
n-mos acts as (constant current source)



* when drain voltage exceeds the gate voltage, drain takes the control on channel.

* Gate looses the control on channel near the drain

i. $v_{ds} = v_{gs} - v_{th}$



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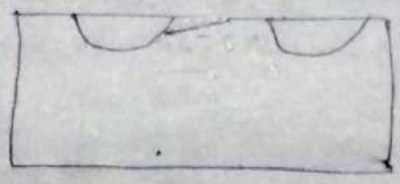
* ii. $V_{ds} > V_{gs} - V_{th}$
channel will demolish before reaching the drain



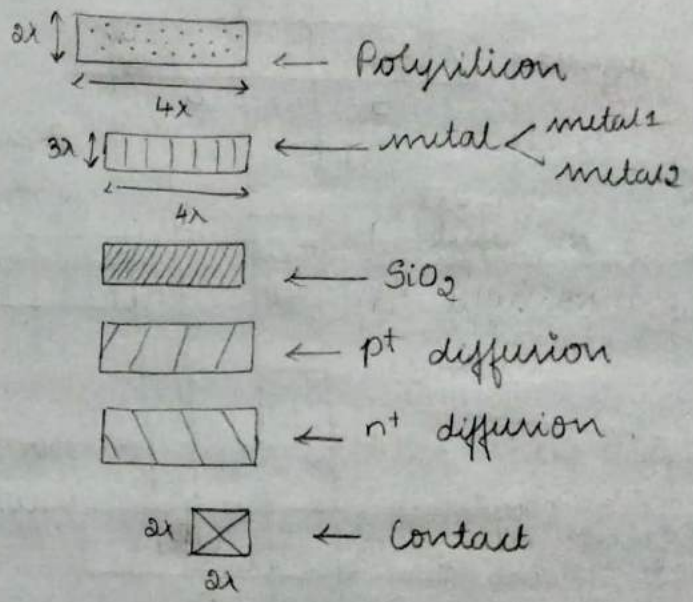
* Effective channel length, $L_1 = L - \Delta L$

* Even though channel become zero at drain, current will n't zero because V_{ds} has greater energy to pull the e from near the source.
* But the current will be at saturation.

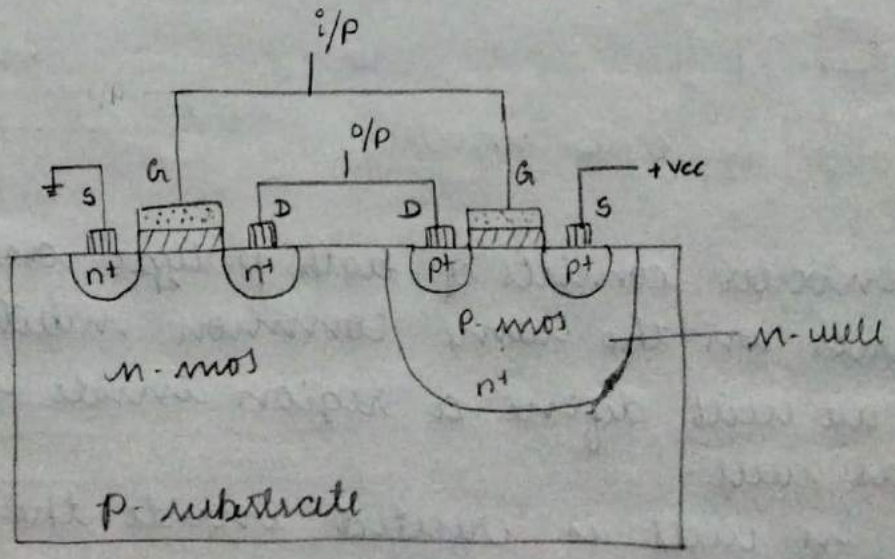
21/03/2022

Layout:

λ based rules:

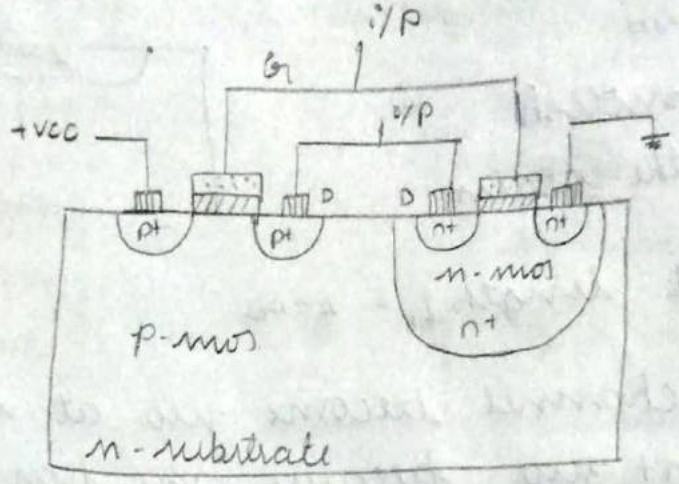


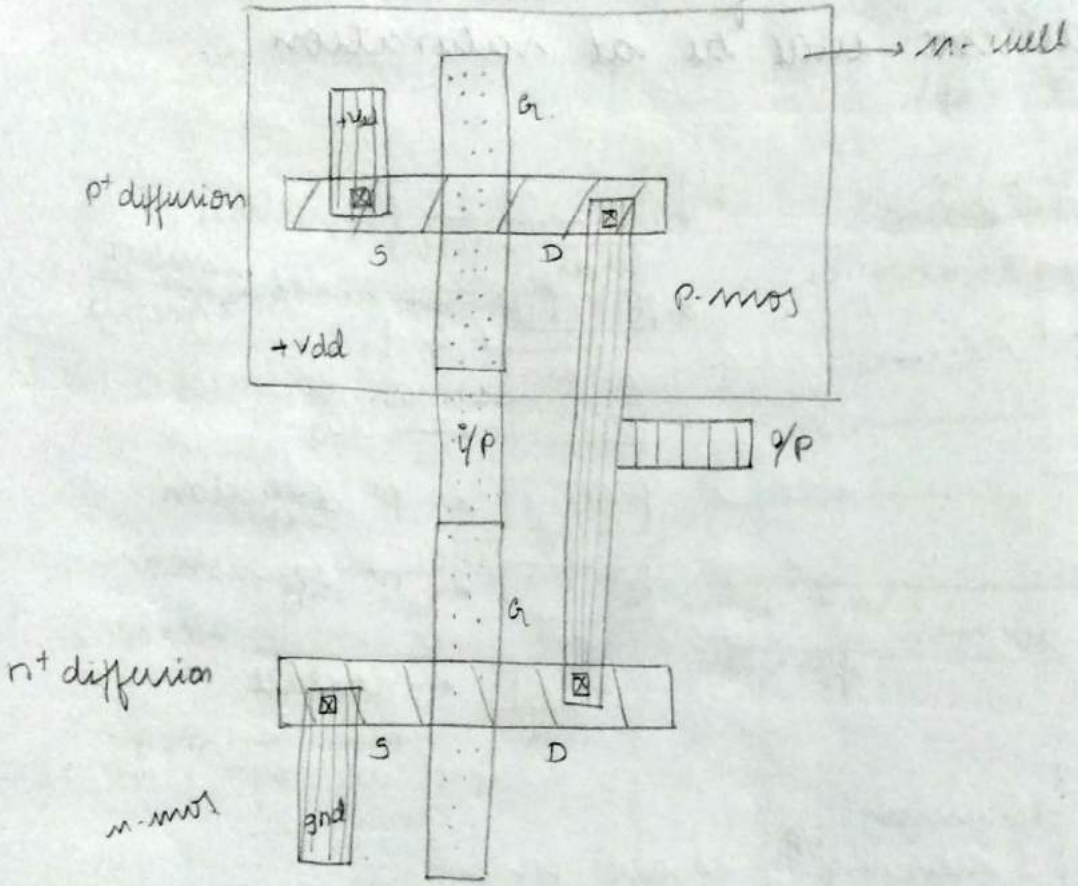
CMOS inverter:



Well → Defining a region inside the substrate

Scanned with CamScanner





Layout of CMOS inverter

* A CMOS inverter consists of both p-type and n-type MOS devices on the same common substrate
* Therefore we will define a region inside a substrate called as well.
* Usually n-well is created inside the p-substrate
* whenever polysilicon crosses n^+ diffusion we will get n-mos, similarly, whenever polysilicon crosses p^+ diffusion we will get p-mos.

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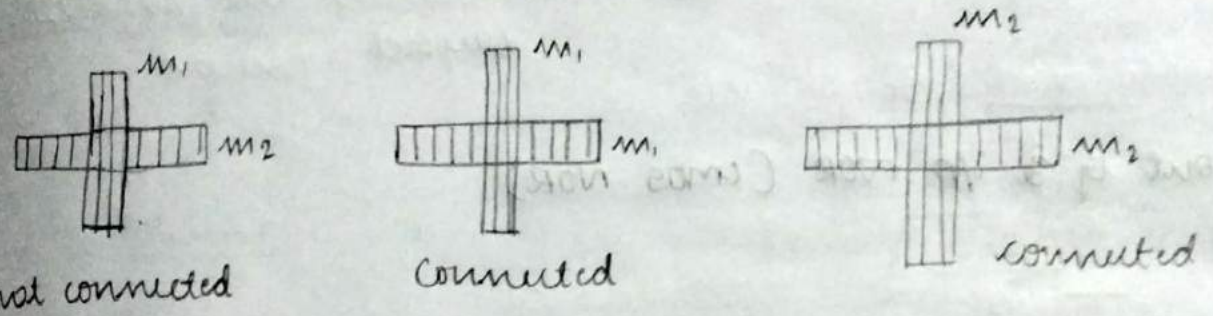
* Identify the all the terminals of n-mos & p-mos
* Gate of n-mos & p-mos are shorted because they are of same type.
* p^+ and n^+ diffusions are connected via metal with contact because they are of different types. (drain)
* Connect source of n-mos to ground via metal with ~~me~~ contact and connect source of p-mos to $+V_{dd}$
* well should connected to either higher potential or lower potential depending upon type of mos used.
* Here well is connected to $+V_{dd}$, because we are creating p-mos using n-well.



* If the two metals are of same type, then they are connected otherwise not connected (overlap)

Schematic to Layout (SL):

1. Full custom layout design:
   Building the layout from the scratch.
2. Semi custom layout design:
   * Transistors are already exist/present, we need to do only connection (just like drag and drop).

RC extraction:

Extraction of R and C from the layout.

Capacitance: In a layout Inbetween the two metals, there will be some gap, so that dielectric comes into picture ⇒ Parallel plate capacitor.

R- Any active device posses some internal resistance.

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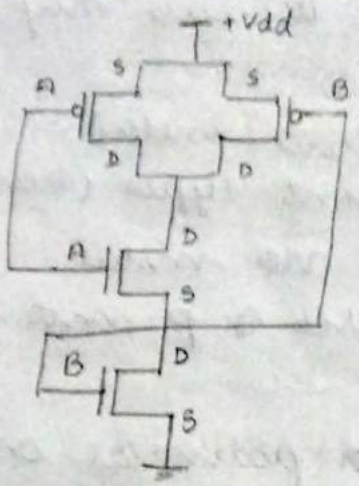
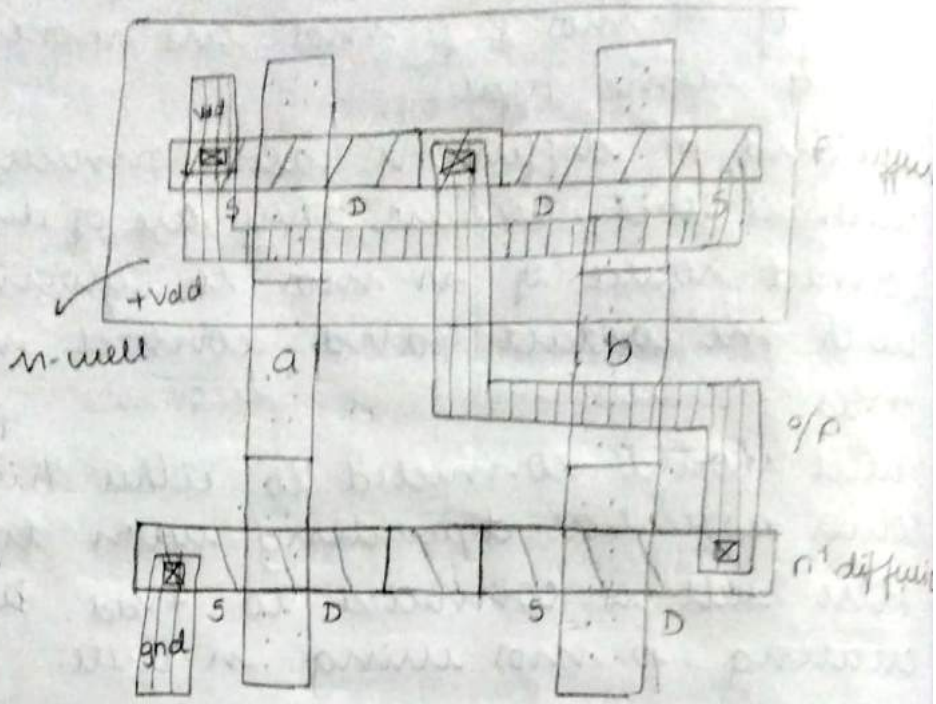
Layout of 2 i/p CMOS NAND

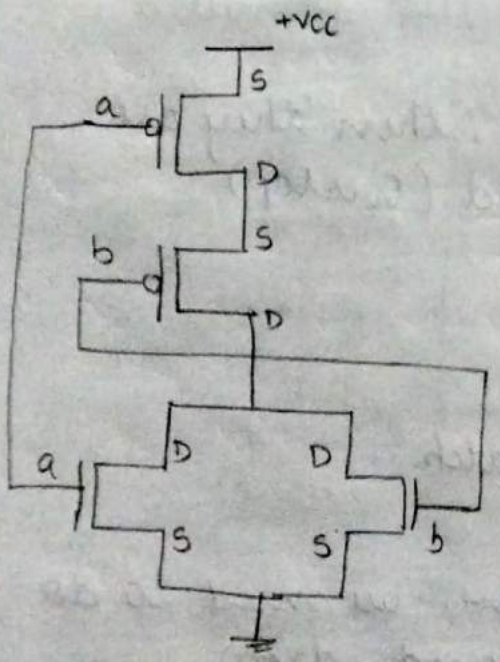


Schematic

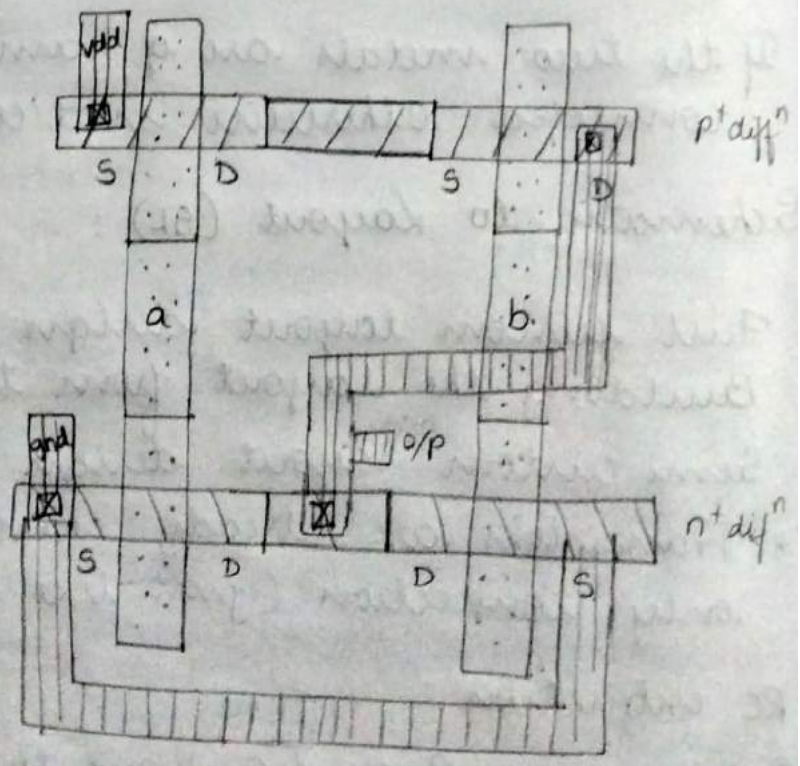


Layout

Layout of 2 i/p NOR (CMOS NOR)



Schematic



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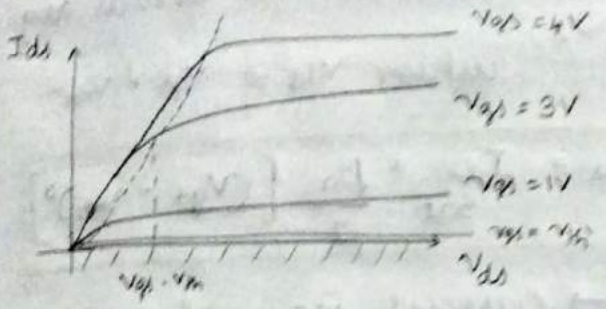
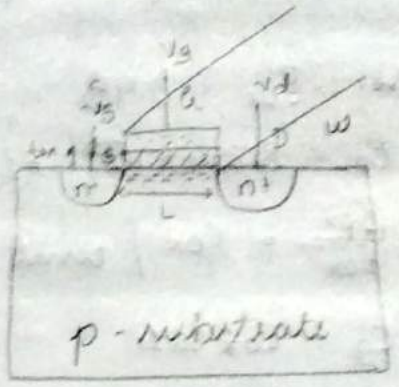
23/03/2022

Regions of operations :

1. cutoff region or Subthreshold region ($v_{gs} < v_{th}$) , $I_{ds} = 0$
2. linear region
3. Saturation

} $v_{gs} \geq v_{th}$

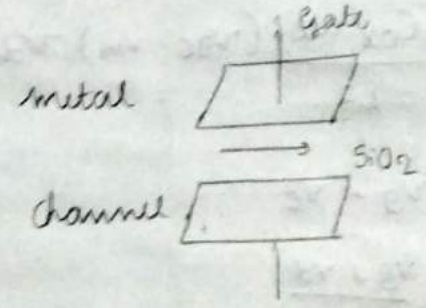




ii when $v_{gs} \geq v_{th}$.

$$I_{DS} = \frac{Q}{\Delta t}$$

$$I_{DS} = \frac{Q_{channel}}{\Delta t}$$



For parallel plate capacitor.

$$\boxed{Q = CV}$$

$$Q_{channel} = C_{gc}(v_{gc} - v_{th})$$

$$\therefore I_{ds} = \frac{C_{gc}(v_{gc} - v_{th})}{\Delta t}$$

$$\Delta t = \frac{L}{v} = \frac{\text{Distance}}{\text{velocity}}$$

$$I_{ds} = \frac{C_{gc}(v_{gc} - v_{th})\, v}{L}$$

$v \propto E$, $v = \mu_n E$ where μ_n = mobility

$$I_{ds} = \frac{C_{gc}(v_{gc} - v_{th})\, \mu_n E}{L}$$

* Gate region will be considered as parallel plate capacitor. because metal and channel are of conducting type and oxide layer acts as dielectric

$$E = \frac{V_{ds}}{L}$$

$$I_{ds} = \frac{\mu_n C_{gc}(V_{gs} - V_{th}) V_{ds}}{L^2}$$

$$* \; C_{gc} = C_g = \frac{\varepsilon A}{d} = \frac{\varepsilon_{ox} W L}{t_{ox}}$$

where $\varepsilon_{ox} = 3.9\varepsilon_0$, $\varepsilon_r = 3.9$ for SiO_2

$\varepsilon_0 = 8.854 \times 10^{-12}$ F/cm.

$\frac{\varepsilon_{ox}}{t_{ox}} = C_{ox}$ / unit area

$C_g = C_{ox} W.L.$

$$I_{ds} = \frac{\mu_n C_{ox} W L}{L^2} (V_{gc} - V_{th}) V_{ds}$$

$$* \; V_{gc} = V_g - V_c$$

$$V_c = \frac{V_s + V_d}{2}$$

$$V_c = \frac{V_s}{2} + \frac{V_d}{2} + \frac{V_s}{2} - \frac{V_s}{2}$$

$$V_c = V_s + \frac{1}{2}(V_d - V_s)$$

$$V_c = V_s + \frac{V_{ds}}{2}$$

$$V_{gc} = V_g - V_s - \frac{V_{ds}}{2}$$

$$\boxed{V_{gc} = V_{gs} - \frac{V_{ds}}{2}}$$

$$I_{ds} = \frac{\mu_n C_{ox} W L}{L^2} \left(V_{gs} - \frac{V_{ds}}{2} - V_{th}\right) V_{ds}$$

$$I_{ds} = \frac{\mu_n C_{ox} W}{L} \left(V_{gs} - \frac{V_{ds}}{2} - V_{th}\right) V_{ds}$$

$$I_{ds} = \frac{\mu_n C_{ox} W}{L} \left((V_{gs} - V_{th}) V_{th} - \frac{V_{ds}^2}{2}\right)$$

where $\mu_n C_{ox} \frac{W}{L} = \beta_n$.

$$\therefore \boxed{I_{ds} = \beta_n \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]}$$

↳ current in linear region

when $V_{ds} \geq V_{gs} - V_{th}$

$$\boxed{I_{ds} = I_{ds\,sat} = \frac{\beta_n}{2} \left[(V_{gs} - V_{th})^2 \right]}$$

↳ current in saturation region

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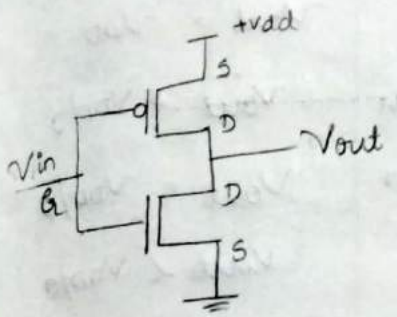
24/03/2022

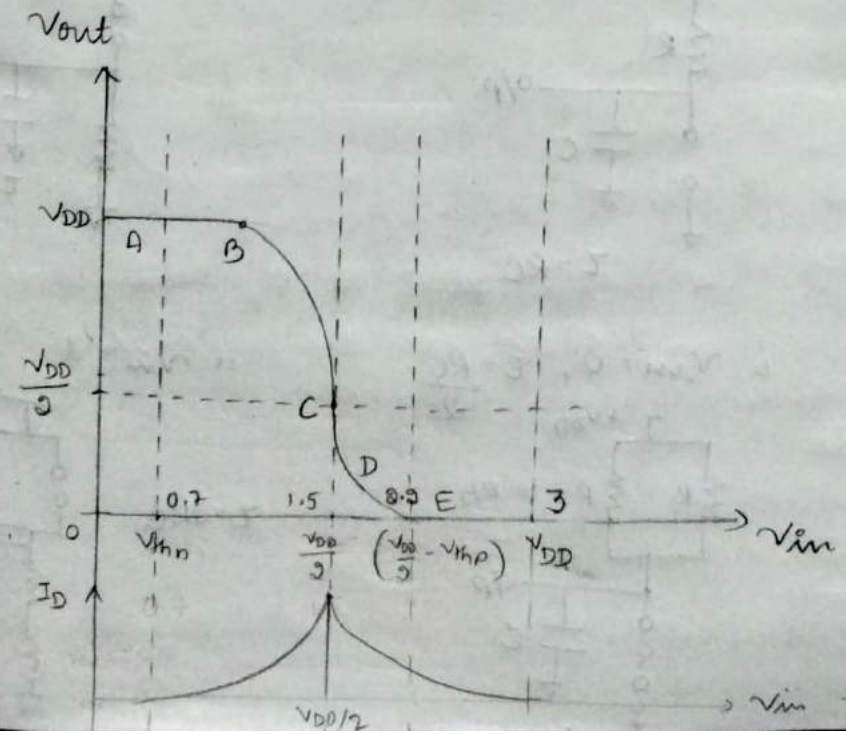
DC Characteristics of CMOS Inverter



NOTE : $V_{thn} \rightarrow +ve$

$V_{thp} \rightarrow -ve$

	Cut off region	Linear region	Saturation region
1. n-mos $V_{gs} = V_{in}$	$V_{gs} < V_{thn}$ $V_{in} < V_{thn}$	$V_{gs} \geq V_{thn}$ $V_{in} \geq V_{thn}$ $V_{ds} < V_{gs} - V_{thn}$ $V_{out} < V_{gs} - V_{thn}$	$V_{gs} \geq V_{thn}$ $V_{in} \geq V_{thn}$ $V_{ds} > V_{gs} - V_{thn}$ $V_{out} > V_{gs} - V_{thn}$
2. p-mos	$V_{gs} > V_{thp}$ $V_{in} > V_{thp} + V_{dd}$	$V_{gs} \leq V_{thp}$ $V_{in} \leq V_{thp} + V_{dd}$ $V_{ds} > V_{gs} - V_{thp}$ $V_{out} > V_{gs} - V_{thp} + V_{dd}$ $= V_{out} > V_{in} - V_{thp}$	$V_{gs} \leq V_{thp}$ $V_{in} \leq V_{thp} + V_{dd}$ $V_{ds} < V_{ds} - V_{thp}$ $V_{out} < V_{gs} - V_{thp} + V_{DD}$ $V_{out} < V_{in} - V_{thp}$



i. $V_{in} = 0.6$, $V_{out} = V_{DD}$

ii. $V_{in} = 1V$

$V_{out} > \frac{V_{DD}}{2} \Rightarrow V_{out} = 2V$

iii $V_{in} = \frac{V_{DD}}{2} = 1.5 = V_{out}$

iv. $V_{in} = 1.8V$

$V_{out} < \frac{V_{DD}}{2} = 0.6V$

v. $V_{in} = V_{out} = 0V$

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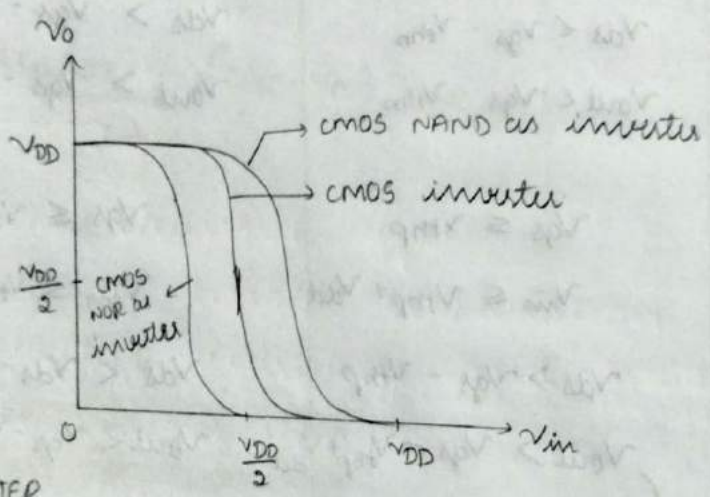
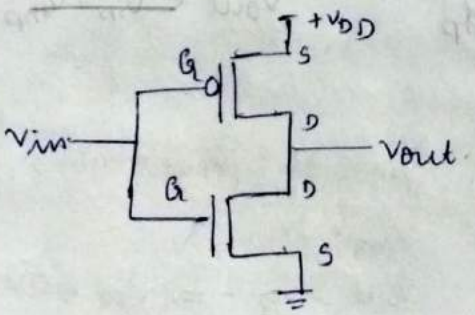
Region	Condition	p-mos	nmos	Output
A	$0 \le V_{in} < V_{thn}$	Linear	Cut-off	$V_{out} = V_{DD}$
B	$V_{thn} < V_{in} < V_{DD}/2$	Linear	Saturation	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	Saturation	Saturation	$V_{out} = V_{DD}/2$
D	$V_{DD}/2 < V_{in} < \frac{V_{DD}}{2} - V_{thp}$	Saturation	Linear	$V_{out} < V_{DD}/2$
E	$\frac{V_{DD}}{2} - V_{thp} < V_{in} \le V_{DD}$	Cut-off	Linear	$V_{out} = 0$

28/03/2022

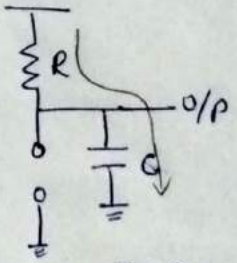
DC Characteristics :



INVERTER

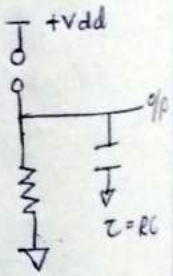


i. $V_{in} = 0$

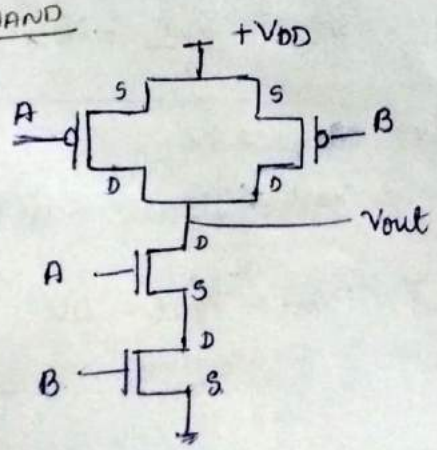


$\tau = RC$

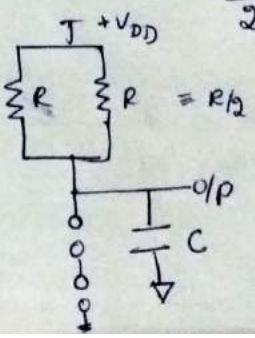
ii $V_{in} = 1$.



NAND

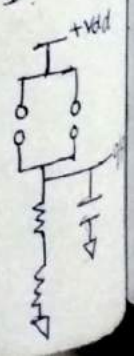


i $V_{in} = 0$, $\tau = \frac{RC}{2}$



ii $V_{in} = 1$.

$\tau = 2RC$



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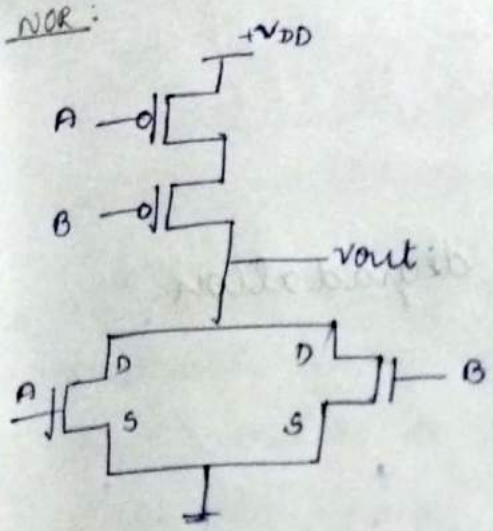
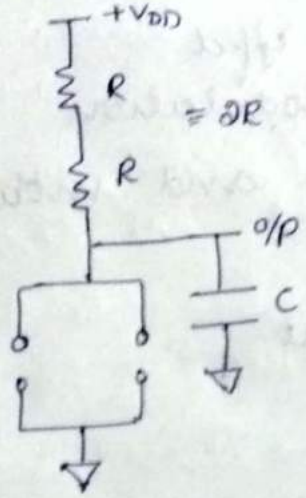
NOR:

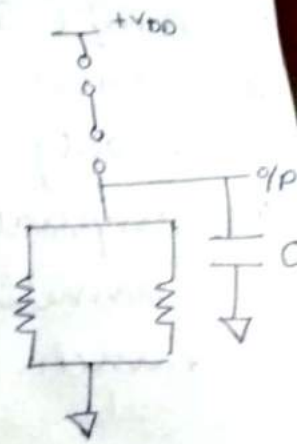


i. $V_{in} = 0$



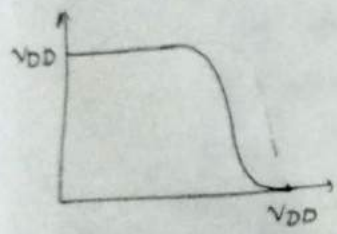
$\tau = 2RC$

ii. $V_{in} = 1$



$\tau = \frac{RC}{2}$

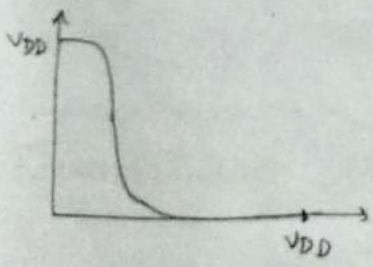
NAND:



* Discharging time is more
  Charging time - less.
* High to low transition - slow.
* Low to high transition - Fast.

∴ Q point will shift to right side.

NOR:



* Discharging time - less.
  Charging time - more.
  (or)
* Requires less time for high to low transition and more time for low to high transition.

∴ Q point will shift to left side.

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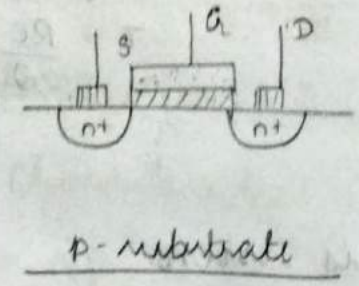
Secondary effects :

1. Body (Substrate) effect :
2. Channel length modulation.
3. velocity saturation and mobility degradation
4. Temperature
5. Tunneling current.
6. Punch through.



30/03/2023

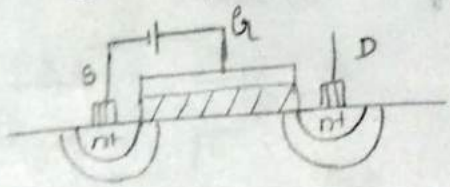
1. Short channel effects :

* Channel length modulation.
* velocity saturation and mobility degradation
* Tunneling current.
* Punch through.

Secondary effects.

* Body effects.
* Temperature

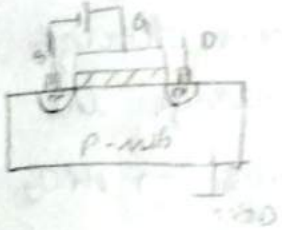
* Body effects :



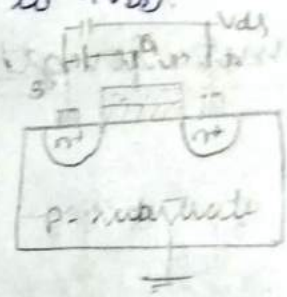
p-substrate

* There will be a depletion region in an unbiased transistor

* After applying V_{gs}, its a kind of forward bias at source - ~~substrate~~ region. Therefore no depletion region near the oxide layer.



* If we connect body to $+V_{DD}$, forward bias condition, there will be a flow of current from body to source. but we don't want this current. Therefore body should not connected to $+V_{DD}$.



* If we connect body to ground.

$$V_{SB} = V_S - V_B$$
$$= 0 - 0$$
$$= 0 \Rightarrow \text{Unbiased condition}$$
(At source & body)

(After applying V_{ds})
Reverse bias condition → Drain & body region (no current

* ∴ No flow of current from body to source.

If $V_{SB} = 0$, no body effect.

~~why~~ $V_{SB} = 0$ → But case reverse bias → worst case

Tunneling current:

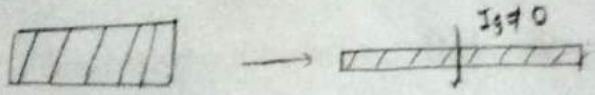
$$I_{ds} = \frac{\mu_n C_{ox} W}{L}\left((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right)$$

$$C = \frac{\epsilon_{ox} A}{t_{ox}} = \frac{\epsilon_{ox} WL}{t_{ox}} \rightarrow \text{constant}$$

$$C \propto \frac{1}{t_{ox}}$$

If we reduce oxide thickness to 0.5nm, (C ↑)

$I_d = 0$ normal



* If we keep on reducing the tox, there will be a gate current. ($I_g \uparrow$), then we have to stop reducing the ~~Ox~~ ox_t ~~tox~~.

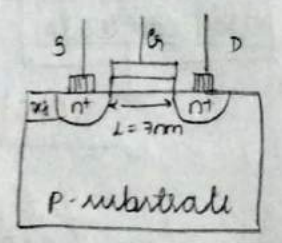
even though I_g is $\uparrow$, still we want $\downarrow$ the ox_t change the material, so that $\varepsilon_0 \varepsilon_r$

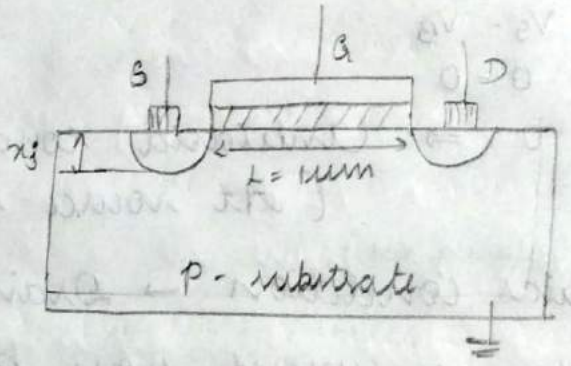
$SiO_2 \longrightarrow HfO_2$, $SiO_2 \rightarrow \varepsilon_r = 3.9$

$HfO_2 \rightarrow \varepsilon_r = 1.1$

Gate current $\longrightarrow$ Tunneling current.

Channel length modulation.





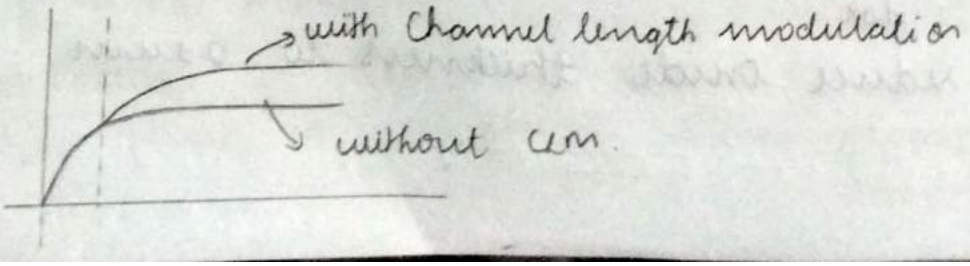
Short channel: $\Rightarrow$ If the channel length is comparable with junction depth, which is almost same, then it's called short channel.

$$L \cong x_j$$

$V_{gs} > V_{th}$, $V_{ds} < V_{gs} - V_{th}$

Saturation $\begin{cases} V_{ds} = V_{gs} - V_{th} \\ V_{ds} > V_{gs} - V_{th} \end{cases}$

* Channel length modulation happens only in saturation region.



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$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2$$

$$L_{eff} = L - \Delta L = L\left[1 - \frac{\Delta L}{L}\right]$$

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L\left(1 - \frac{\Delta L}{L}\right)} (V_{gs} - V_{th})^2$$

$$I_{DS}' = \frac{\mu C_{ox}}{2L} W (V_{gs} - V_{th})^2 \left(1 - \frac{\Delta L}{L}\right)^{-1}$$

$$\left(1 - \frac{\Delta L}{L}\right)^{-1} = (1 - x)^{-1} = 1 - x + x^2 \quad \text{if } x < 1$$

$$\left(1 - \frac{\Delta L}{L}\right)^{-1} = 1 + \frac{\Delta L}{L}$$

$$I_{DS}' = \frac{\mu C_{ox}}{2L} W (V_{gs} - V_{th})^2 \left(1 + \frac{\Delta L}{L}\right)$$

$\Delta L \propto V_{ds}$

$$\frac{\Delta L}{L} = \frac{\lambda' V_{ds}}{L}$$

$$\lambda = \frac{\lambda'}{L}$$

$$\frac{\Delta L}{L} = \lambda V_{ds}$$

$$I_{DS}' = \frac{\mu C_{ox} W}{2L} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds})$$ where λ = slope.

$$\boxed{I_{DS}' = I_{DS} (1 + \lambda V_{ds})}$$ with CLM.

when $\lambda = 0$, $I_{DS}' = I_{DS} \Rightarrow$ no channel length modu^n

$I_{DS}' \propto V_{ds}$.

* In long channel transistor, ΔL is small.

$$L_{eff} = L - \Delta L$$

$$\boxed{L_{eff} \approx L}$$

$\therefore$ CLM has less impact on long channel and more impact on short channel.

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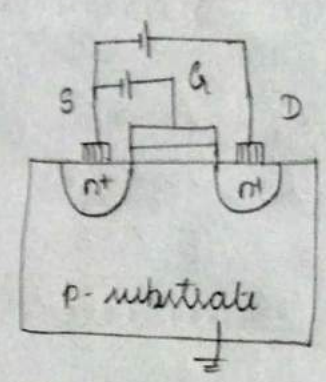
31/09/2021

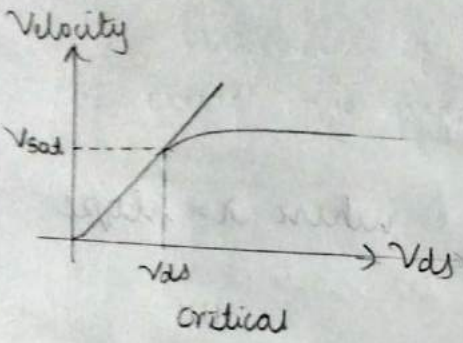
Short Channel effect:

velocity saturation and mobility degradation:



* Lateral electric field → V_{gs}
  (Field created by V_{ds})
* V_{gs} creates the vertical field.
* $E_{Lateral}$: Field created by V_{ds}
  $E_{vertical}$: field created by V_{gs}

* ~~Lateral~~ of



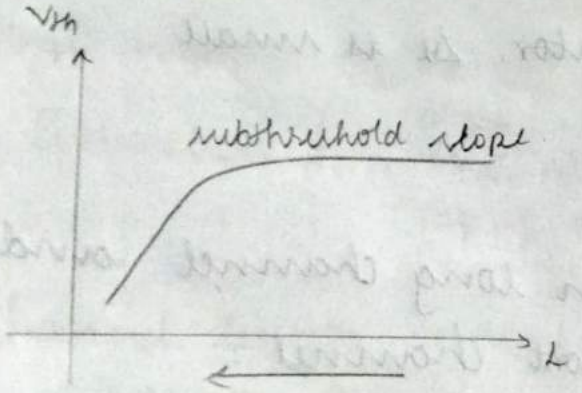
$V \propto E_{lateral}$

$V = \mu E_{lat}$

where μ = mobility

* For low values of V_{ds}, velocity varies linearly.

* If we increase the V_{ds}, there will be a collision of charge carrier therefore mobility will decrease.
* vertical field of gate is also ampels the mobility



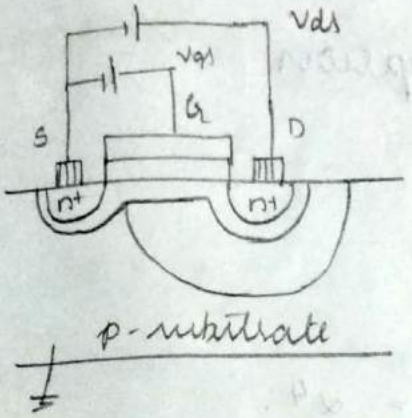
* As we move from long channel to short channel,
  If ↓ in the channel length V_{th} is also ↓

Effect of short channel:

* Gate looses its control on channel.

so that, there is no difference b/w enhancement mode and depletion mode.

Punch through:



As the Vds ~~increases~~, depletion

* After applying Vgs, Source-substrate region in FB
* After applying Vds, Drain-substrate region is in RB.

* As the Vds ↑, Depletion region of Drain is also ↑, and it will overlap with depletion region of Source.
* Charge carrier moves through depletion region.

4/4/22

Scaling: constant E-field scaling Theory:

In 1974, David Dennard, tried to scale all the linear dimensions (W, L, t_{ox}, x_j) by a factor → ($1/\alpha$) where $\alpha > 1$.

* The doping concentration is scaled by α
* Supply voltage → $1/\alpha$.

Derive: * I_D ↓ by a factor ($1/\alpha$)

* $C = \frac{\epsilon_0 A}{d} = \frac{\epsilon W L}{t_{ox}} = \frac{\epsilon \times 1/\alpha \times 1/\alpha}{1/\alpha}$

⇒ capacitance is ↓ by ($1/\alpha$).

* τ = delay = $RC = \frac{VC}{I} = \frac{CV}{I} = \frac{1/\alpha \times 1/\alpha}{1/\alpha}$

⇒ τ is ~~increased~~ scaled by a factor ($1/\alpha$).

Circuit: Power $= VI = \frac{1}{\alpha} \cdot \frac{1}{\alpha} = \frac{1}{\alpha^2}$

Power is reduced by the factor $\frac{1}{\alpha^2}$

Circuit becomes faster with less power consumption

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* Energy = Power × delay $= \frac{1}{\alpha^2} \times \frac{1}{\alpha} = \frac{1}{\alpha^3}$.

Reduction in the energy consumption
$\Rightarrow$ Heat production is more.

* Circuit density $\propto \frac{1}{A^2}$

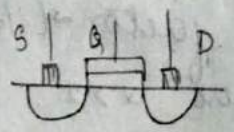
$$= \frac{1}{(\omega L)^3} = \frac{1}{\frac{1}{\alpha^2} \cdot \frac{1}{\alpha^2}} = \alpha^4.$$

Circuit density $\uparrow$s

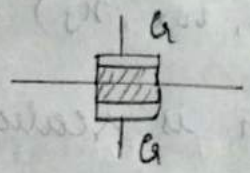
Moore's law:

The number of transistor on a chip/ circuit doubles for every one and half years to two years.

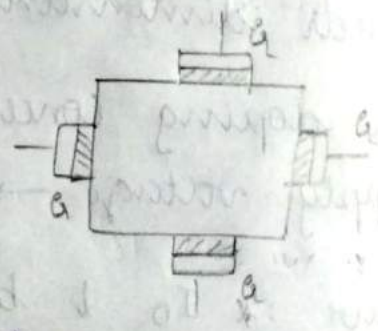
Single gate



Double gate



All gate



FINFET $\rightarrow$ Gate all around.
SET $\rightarrow$ Single electrode transistor

Pipelining:

Inst 1 $\rightarrow$	Fetch	decode	Execute	write back	
Inst 2 $\rightarrow$		Fetch	decode	Execute	write back
Inst 3 $\rightarrow$			Fetch	decode	Execute
					write back

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06/04/22

Temperature dependence:

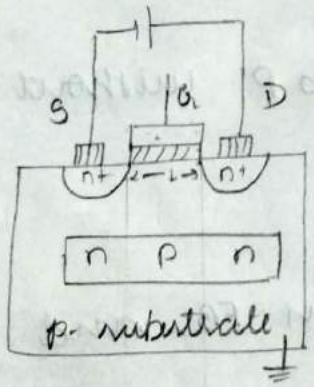
$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-3/2}$$ where T_0 = room Temperature

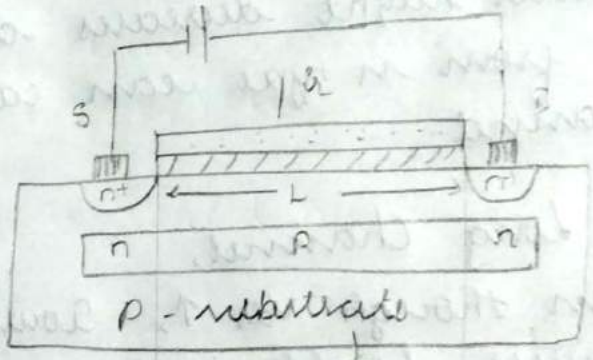
as $T \uparrow$, $\mu \downarrow$

mobility is due to scattering of atoms (carrier).

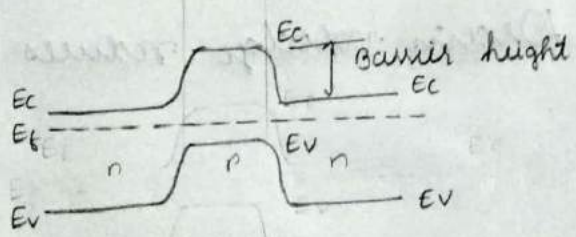
* If T changes from 27°C to 130°C, then mobility will be 1.6.
* As the $T \uparrow$, Energy of carriers $\uparrow$, and threshold voltage $\downarrow$ses.

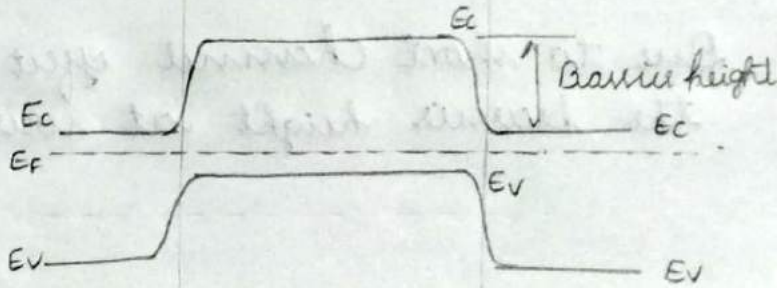
DIBL: Drain reduced barrier lowering.





Unbiased condition.





* Near the junction n-type looses e^-, means its becomes more +ve, ∴ f p-type looses holes & becomes more -ve at the junction. ∴ f (Tramition)

After applying V_{ds}, P-substrate - Drain → RB → Barrier height ↑

* Source - body → FB → Barrier height remains same.

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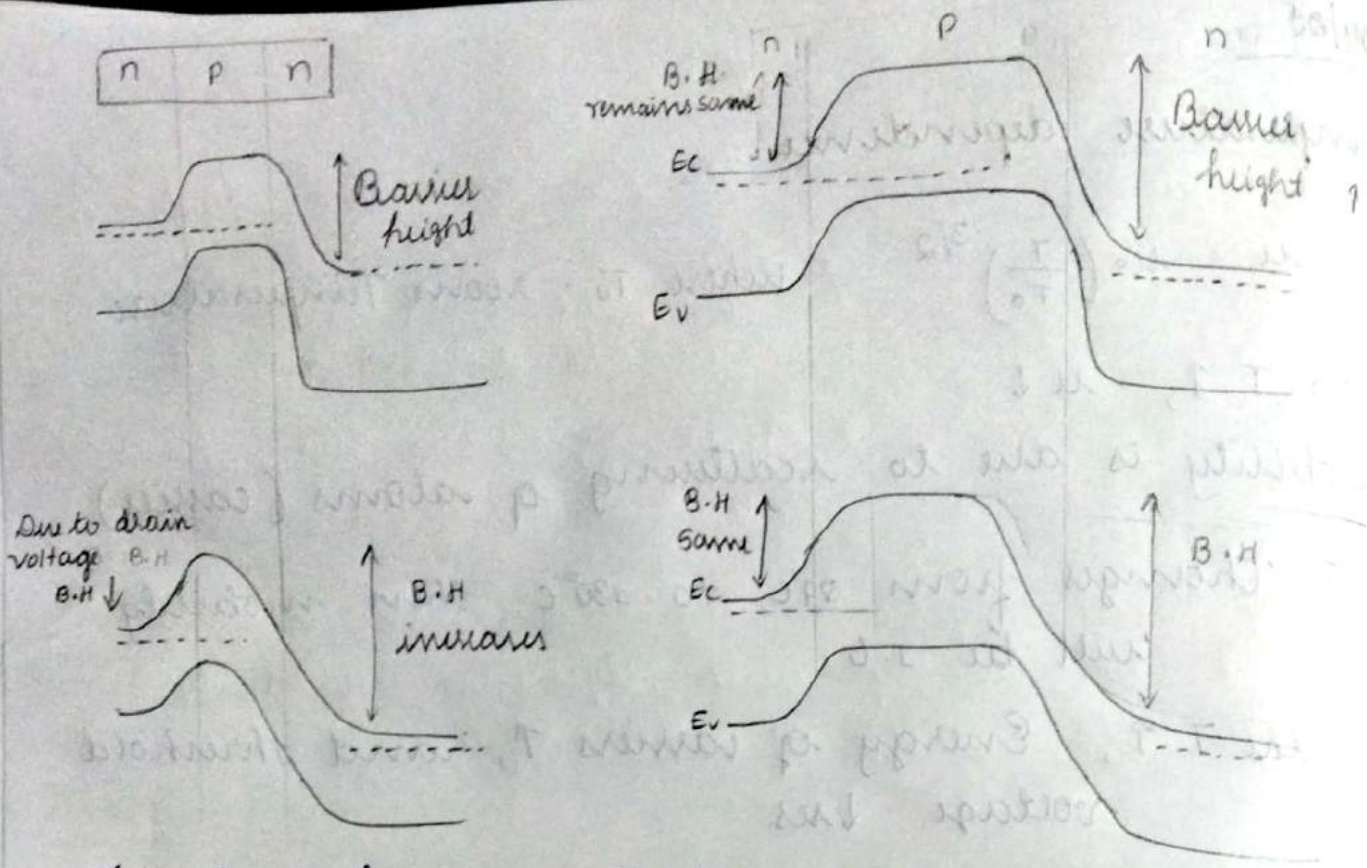

In short channel, As the V_{ds} ↑

* Conduction band of P (E_{cp}) becomes close to E_{cn}.
* Barrier height decreases at source.
* e^- from n type can easily move to P without channel.

In Long channel,

* Even though V_{ds} ↑, Source - Body is in FB, and barrier height remains same.
* no movement of e^- from n to P

Due to short channel effect, Drain voltage reduces the barrier height at source.

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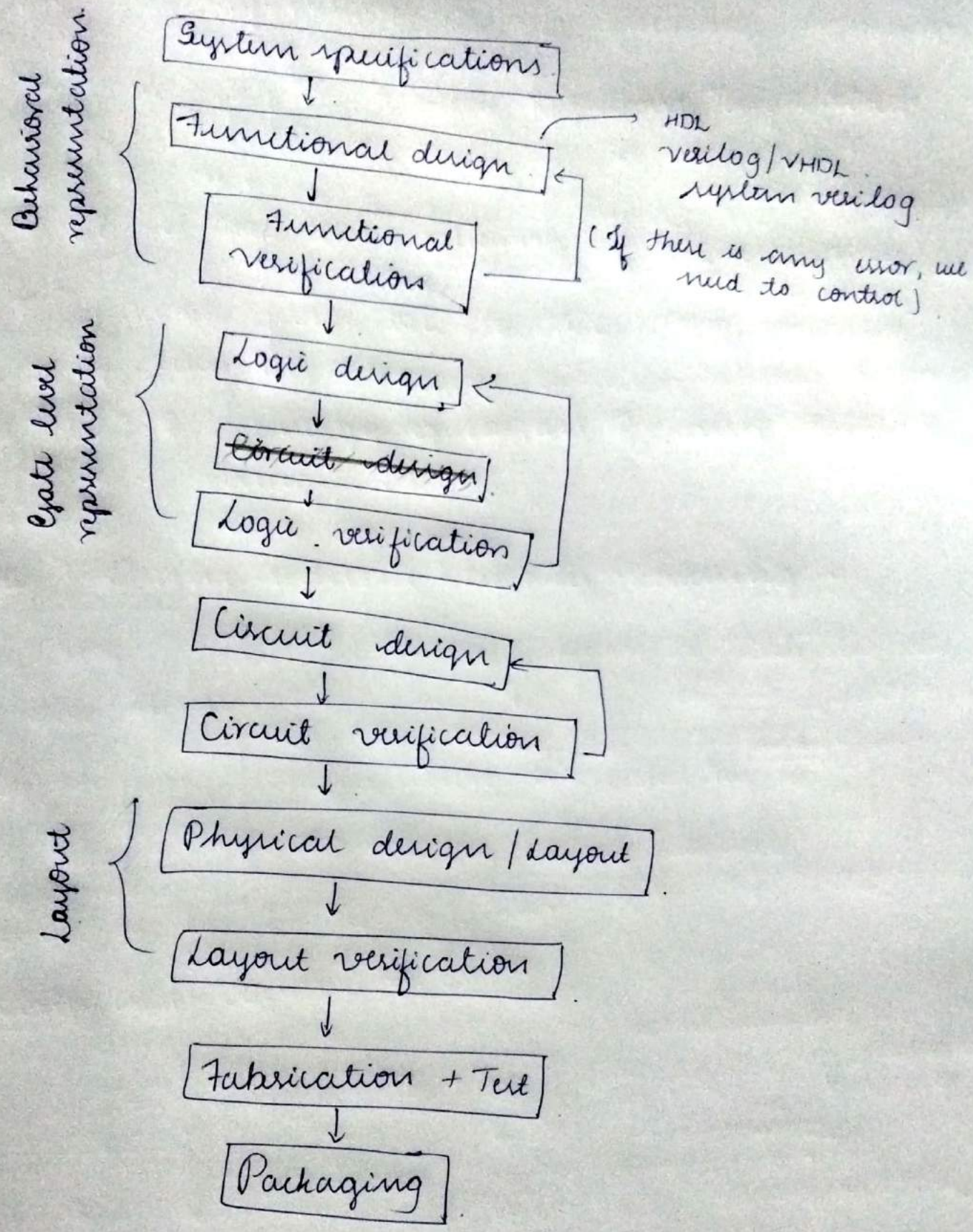
VLSI Design flow:



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18/04/2022

Fabrication :

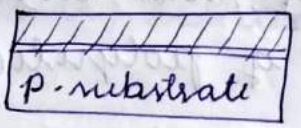
Steps involved in fabrication :

* Oxidation
* Lithography < UV - photolithography / E - beam lithography
* Annealing
* Etching
* Deposition → Sputtering
* Diffusion / Ion implantation

N-mos fabrication process:

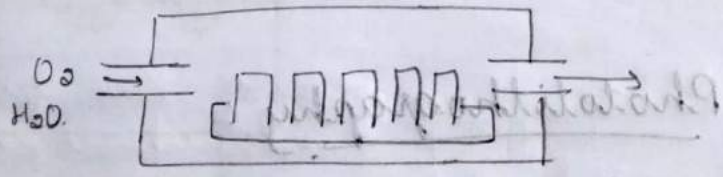
1. (P-type) Top-view

i. SiO_2



SiO_2 acts as insulator as well as gate oxide

After cleaning oxidation is done



* Oxidation of silicon is achieved by heating silicon waters in an oxidizing atmosphere.

i* Wet oxidation : ~~In~~ when 2:1 mixture of Hydrogen and oxygen is used at a Temp. of 900°C & 1000°C, wet oxidation is also called as pyrogenic oxydation.

$$2H_2O + Si \longrightarrow SiO_2 + 2H_2 \uparrow$$

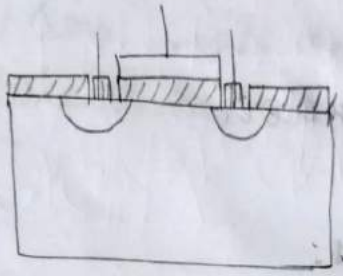
* Oxidizing atmosphere contains water vapours

ii <u>Dry Oxidation:</u>

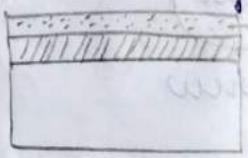
* Oxidizing atmosphere contains pure Oxygen
* Temperature → 1200°C.
* dry Oxidation gives better SiO_2

$$O_2 + Si \longrightarrow SiO_2$$

we need to cooldown the High T. SiO_2 before next oxidation to avoid breakage.



After the oxidation, we can define either region or deposition of polysilicon.



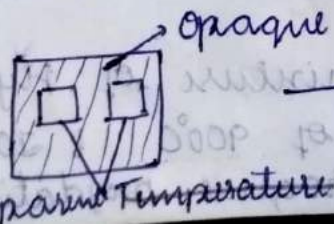
ii Deposition of polysilicon

iii Etching → To remove the unwanted polysilicon

ii] Defining source and drain region followed by etching.

<u>Lithography:</u> i <u>Photolithography:</u>

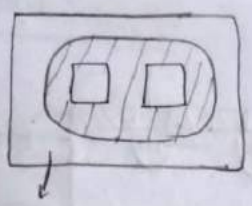
* using photolithography, implantation can occur or dielectric or metal can be etched away in the areas where the mask is absent.



→ Place this on the top of p-type

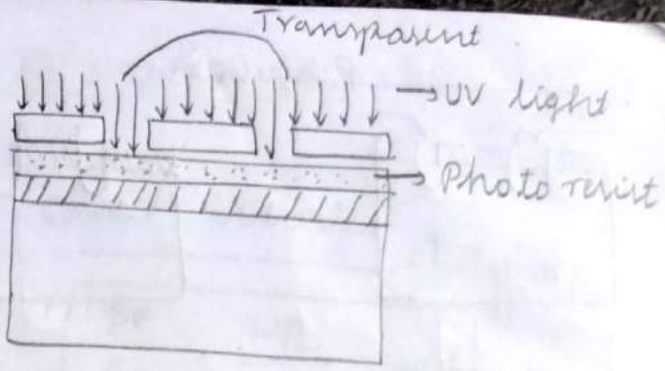
Temperature

i.



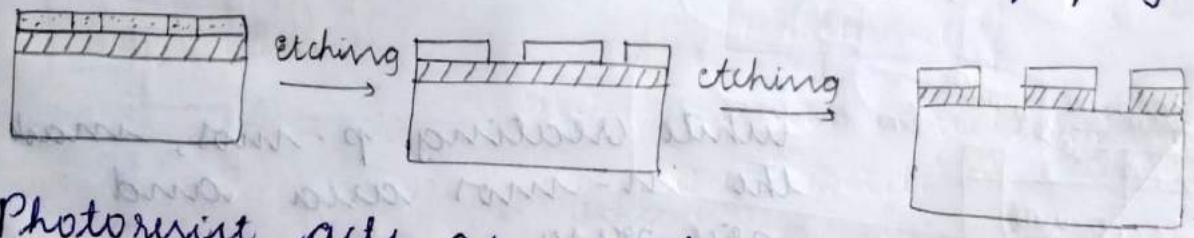
(glass material)

ii



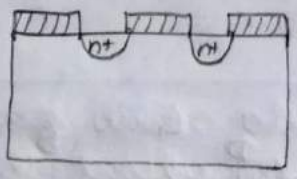
* Pass the light on the top of hard mask,
* Only in the region of Transparent, light will pass (UV rays) and that region will become soften
* Photoresist is sensitive to UV light, wherever UV rays falls on the hardmask, that region will become soften and remaining portion will be still hard.

when we need λ, less than the λ of UV (380nm)
→ we can't define region
Then we go with E-beam lithography.

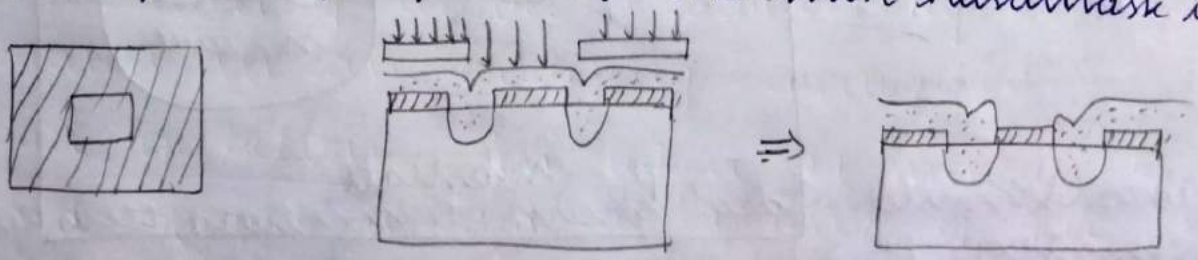


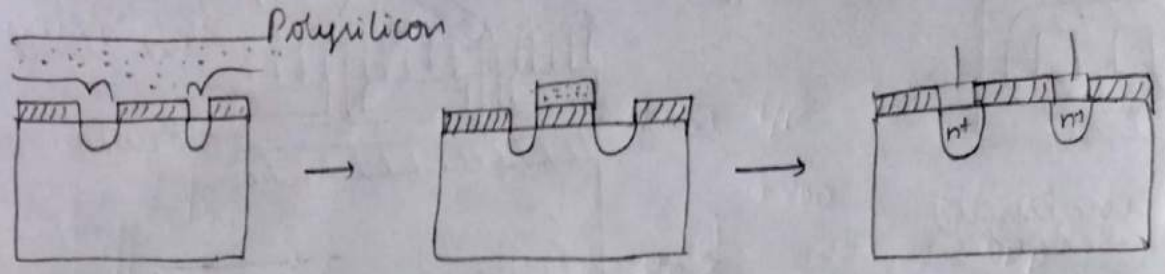
Photoresist acts as mask during lithography.

iii



To deposit polysilicon, one more hardmask is required

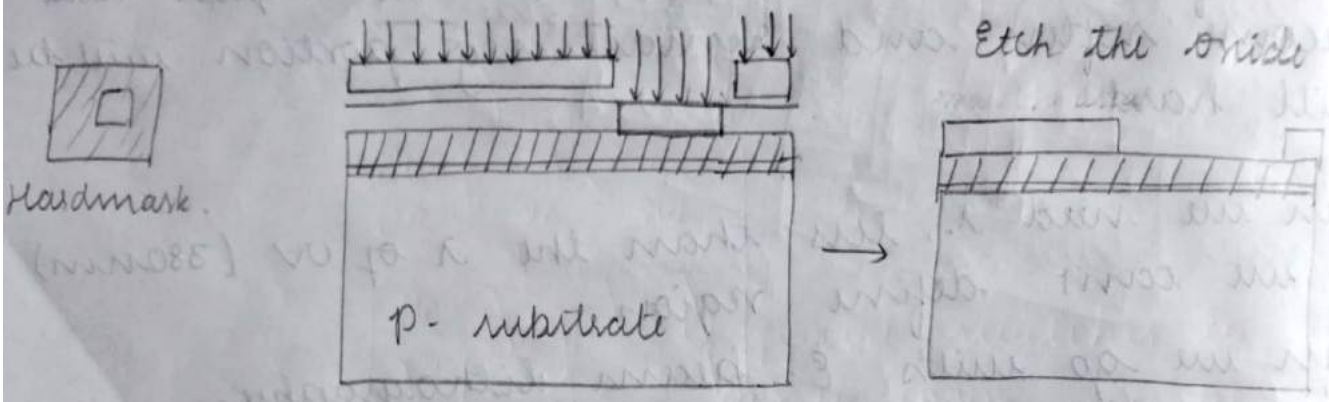


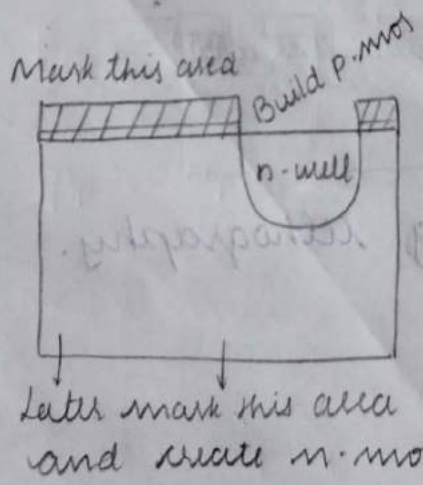


Deposition is always followed by lithography.

Fabrication of CMOS inverter:

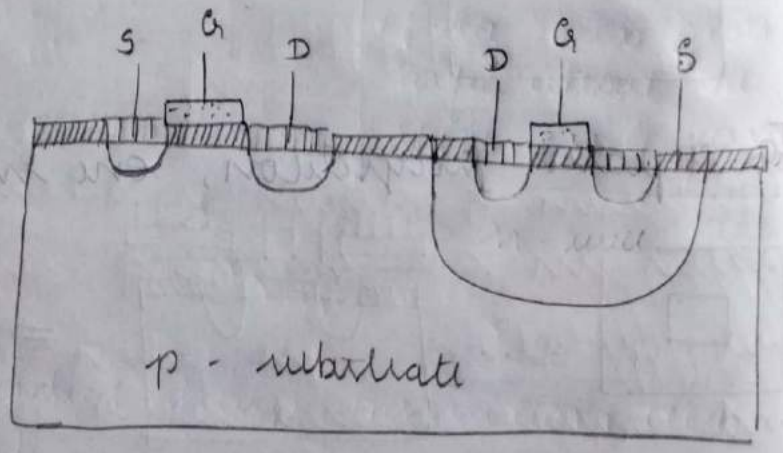
1. Oxidation
2. Create n-well using photolithography.





While creating p-mos, mask the n-mos area and vice versa.

At last:



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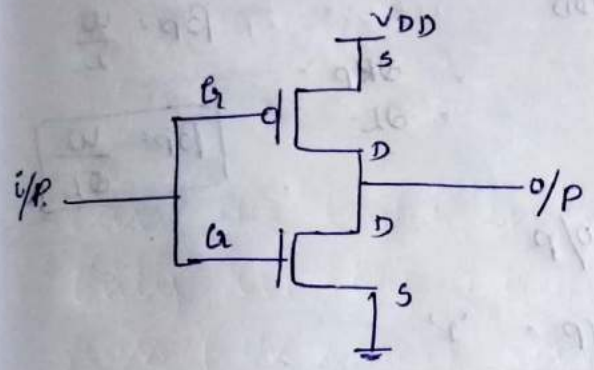
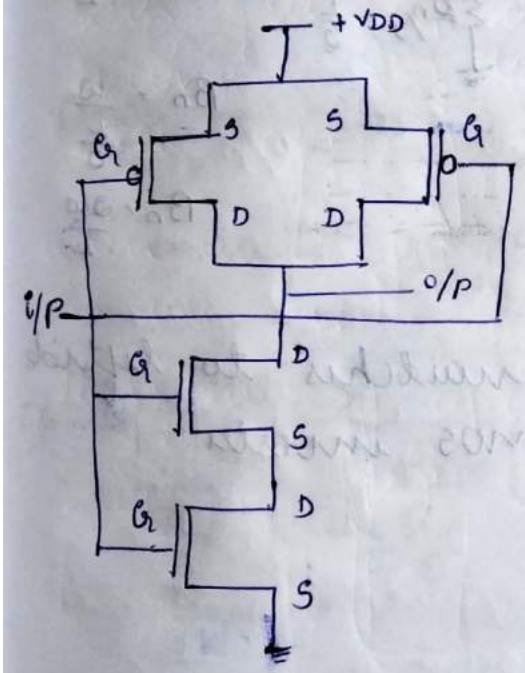
Beta ratio :



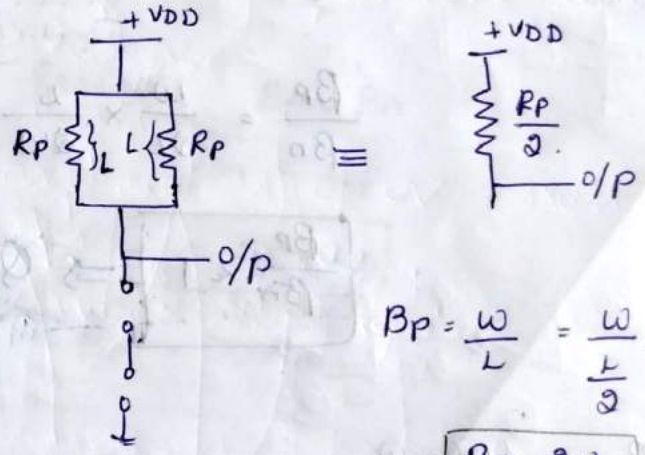
CMOS - inverter

$$\boxed{\frac{\beta_P}{\beta_n} = \frac{W/L}{W/L} = 1}$$

CMOS NAND as inverter :



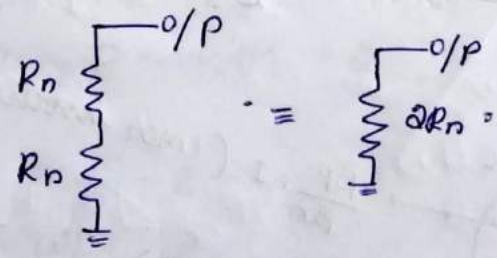
i when i/p = logic '0'



$$\beta_P = \frac{W}{L} = \frac{W}{\frac{L}{2}} = \frac{2W}{L}$$

$$\boxed{\beta_P = \frac{2W}{L}}$$

ii when i/p = logic '1'



$$\beta_n = \frac{W}{L}$$

$$\beta_n = \frac{W}{2L}$$

$$\boxed{\beta_n = \frac{W}{2} \times \frac{1}{L}}$$

$$\frac{\beta_P}{\beta_n} = \frac{\frac{2W}{L}}{\frac{W}{2L}} = 4$$

$$\boxed{\frac{\beta_P}{\beta_n} > 1}$$ (∴ Q point switches to right side w.r to CMOS inverter)

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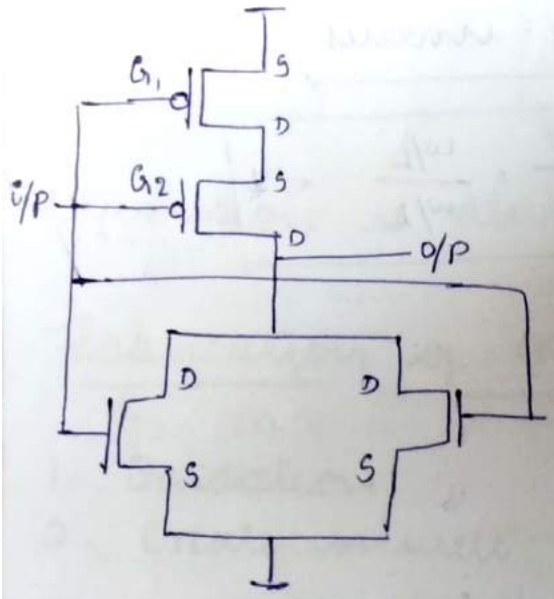
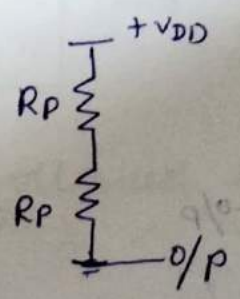
CMOS NOR as inverter:



when i/p = '0'



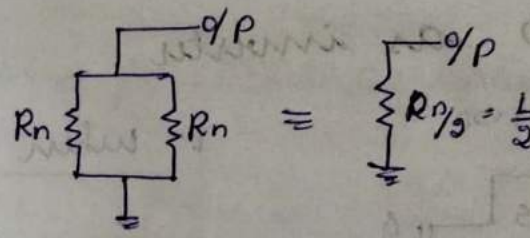
$= 2R_p$

$= 2L$

$\beta_p = \frac{W}{L}$

$\boxed{\beta_p = \frac{W}{2L}}$

when i/p = '1'



$\beta_n = \frac{W}{L}$

$\beta_n = \frac{W}{\frac{L}{2}}$

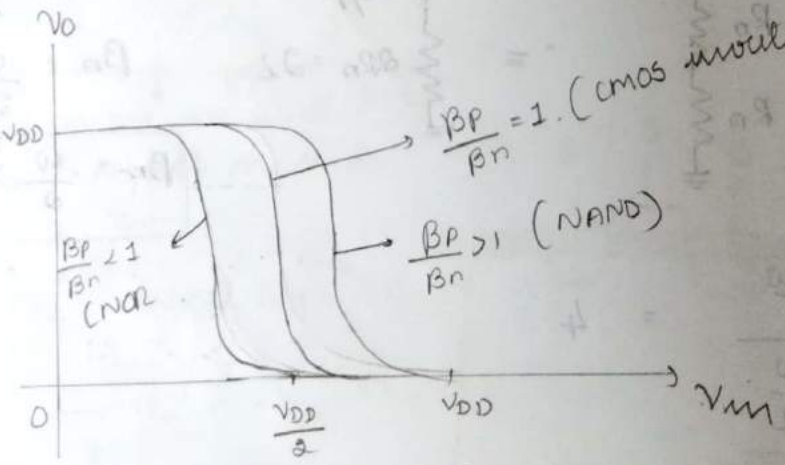
$\beta_n = \frac{2W}{L}$

$$\frac{\beta_p}{\beta_n} = \frac{W}{2L} \times \frac{L}{2W} = \frac{1}{4}.$$

$\boxed{\frac{\beta_p}{\beta_n} < 1}$ ⇒ Q point switches to leftside w.r.to. CMOS inverter.

$\beta_n = \frac{\mu_n C_{ox} W}{L}$ $\qquad \beta_n \propto \frac{W}{L}$

$\beta_p = \mu_p C_{ox} \frac{W}{L}$ $\qquad \beta_p \propto \frac{W}{L}$.



* Beta ratio gives info about the shift in Q-point

* For CMOS inverter, Ideal sharp transition occurs at $\frac{V_{DD}}{2}$ means $\frac{\beta_p}{\beta_n} = 1$.

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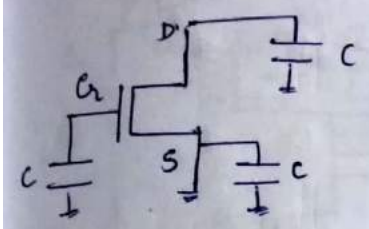
Switch level RC delay:

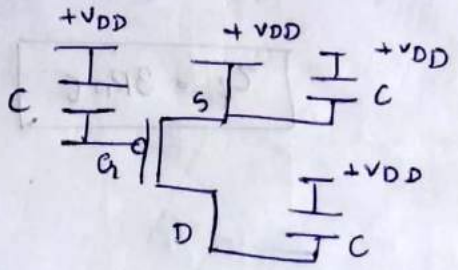
→ Transistor

$C \propto W$
$R \propto \frac{1}{W}$
$R \propto L$

n-mos:



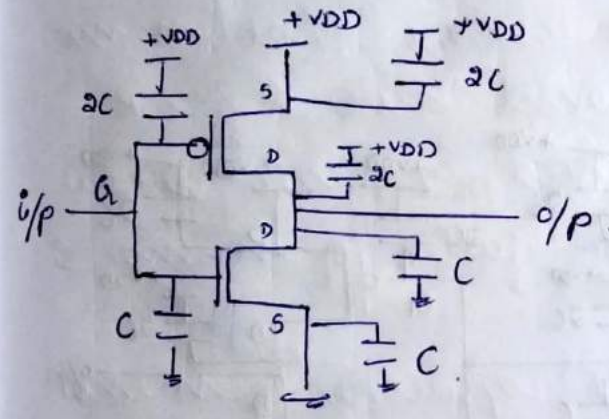
p-mos:



(p-mos)
$\tau_R = RC$
(raising)
$\tau_f = RC$
(n-mos)
(falling)
$\tau_R = \tau_f$
→ To ensure Beta ratio = 1.

* capacitor (because terminals are metals
* Resistor (when transistor is conducting)

CMOS inverter:



Ensure $\beta_p = \beta_n$

$I_{Dn} = I_{Dp}$

$\boxed{\mu_n \approx 2\mu_p}$

$\beta_n = \mu_n C_{ox} \frac{W}{L}$

$\beta_p = \mu_p C_{ox} \frac{2W}{L}$

* Scaling factor for n-mos = 1. (no change)
  for p-mos = 2.

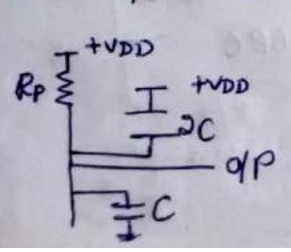
$C = \frac{\epsilon_0 A}{d}$, $C \propto A$, ϵ

$C \propto WL$

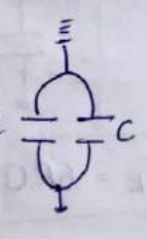
$\boxed{C \propto W}$

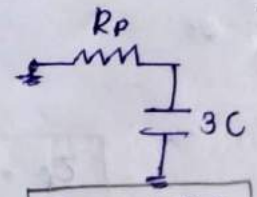
i) when i/p = 0

when i/p = 0, n-mos is off, but D of n-mos is still connected to D of p-mos, ∴ we have to consider capacitor of Dn



⇒





$\boxed{\tau_R = 3R_pC.}$

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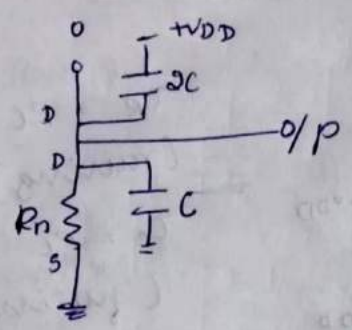
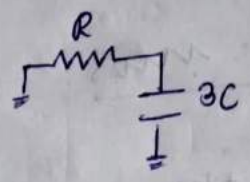
ii) when i/p = 1

$\tau_R = \tau_f = 3RC$

when $R_p = R_{n=p}$



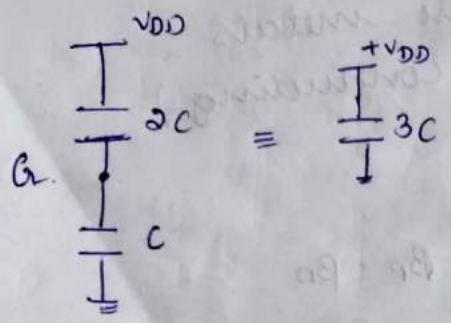


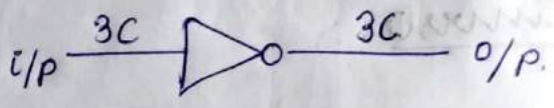
$\boxed{\tau_f = 3R_nC}$

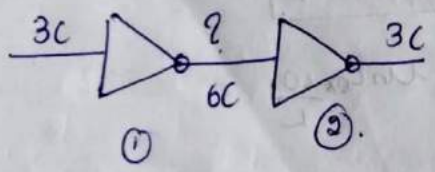
i/p capacitance:

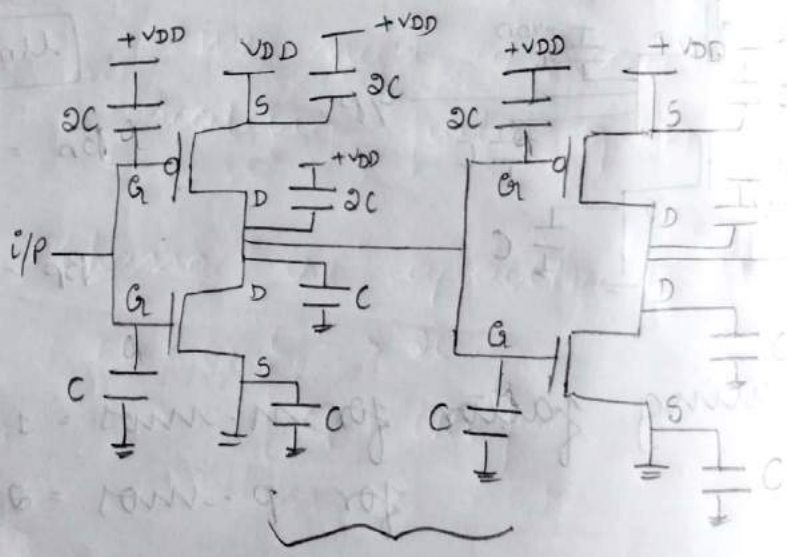
i/p capacitance = 3C

o/p capacitance = 3C

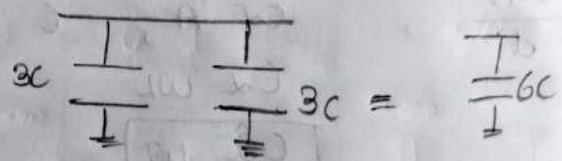


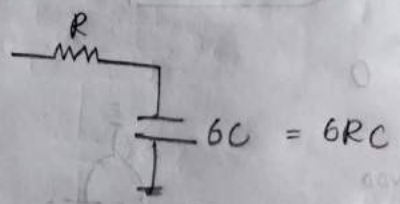






* CMOS inverter is basis for all other circuits.





$\boxed{\tau_f = \tau_R = 6RC}$

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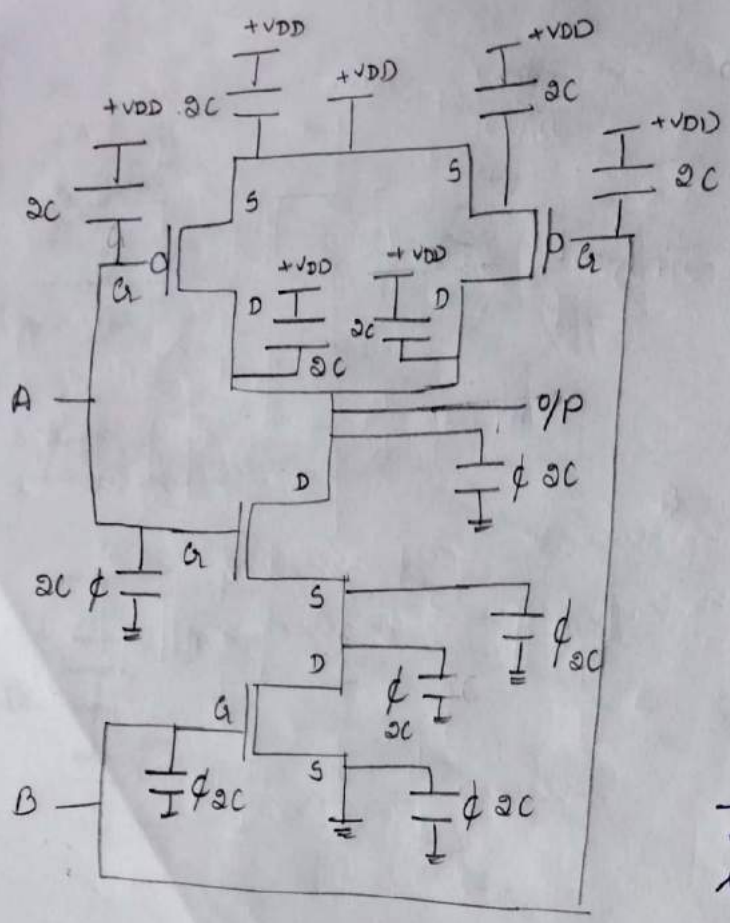
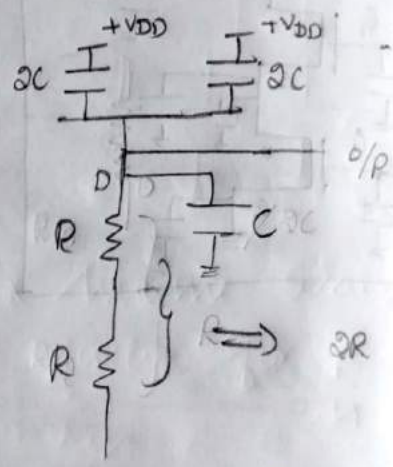
CMOS NAND:



* Assume scaling factor for
  p-mos = 2
  n-mos = 1

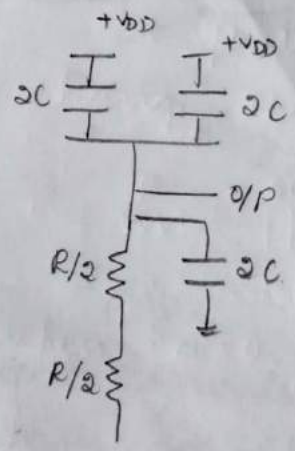
when A = B = 1



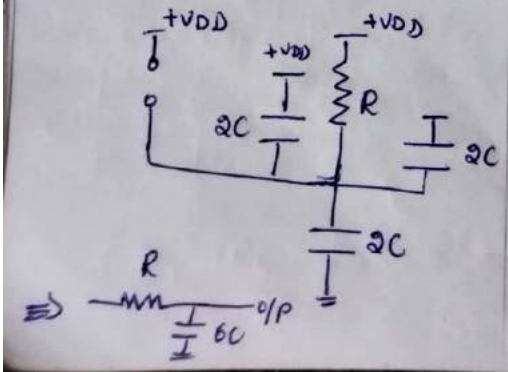
To ensure that n-mos should give $R_{eff} = R$
we need to scale $W = 2W$
∴ Scaling factor of n-mos = 2

Change the capacitor value of n-mos
$C \rightarrow 2C$.

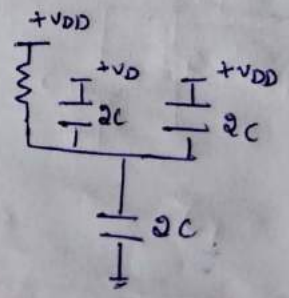
$\boxed{\tau_f = 6RC}$



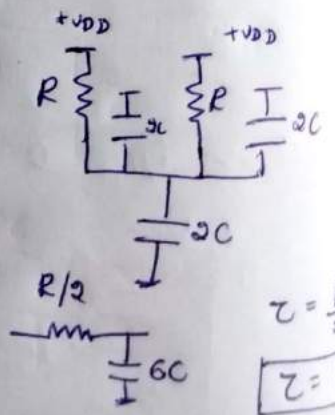
when i/p = 10



i/p = 01



i/p = 00



$\tau = \frac{RC}{2}$

$\boxed{\tau = 3RC}$

when i/p = 00, $R_{eff} = \frac{R}{2}$

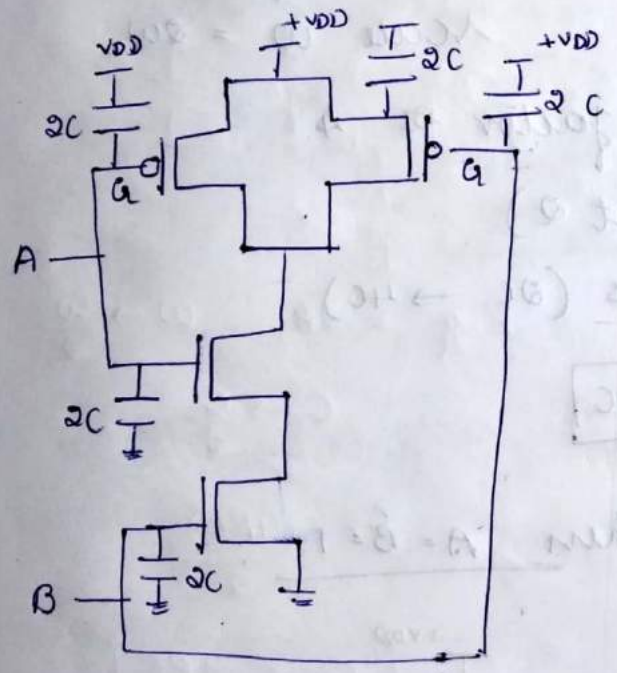
here p-mos is not scaled, because it will change the other combination (10, 11, 01) effective resistance.

Inverter	NAND
* P-mos - scaled	* P-mos - not scaled
* n-mos - not scaled.	* n-mos - scaled.

25/04/22

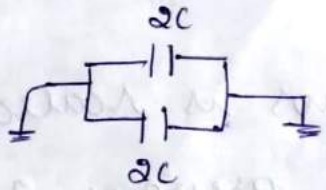
RC delay:

2 i/p NAND:



when A=1, B=0

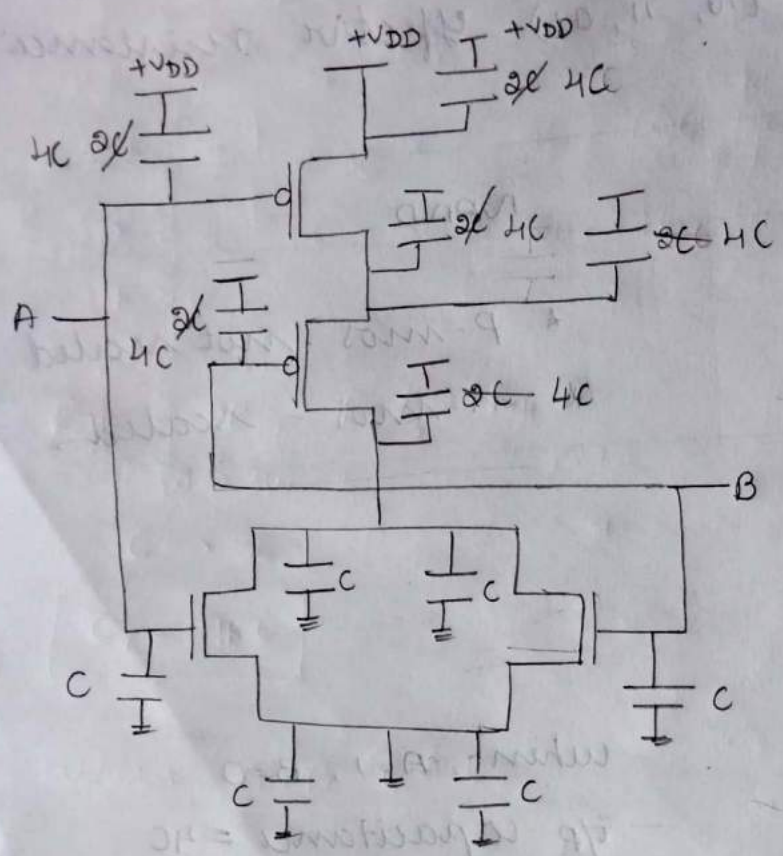
i/p capacitance = 4C

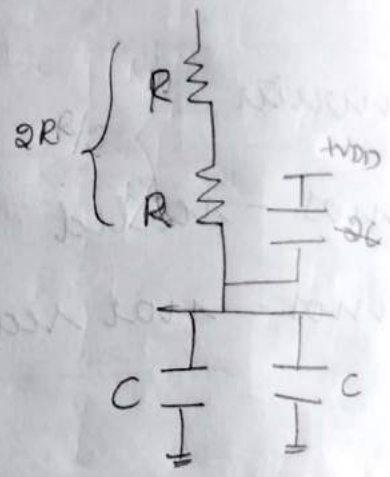


o/p capacitance = 6C

Find τ_f, τ_r for NOR gate:

i. when A = B = 0.



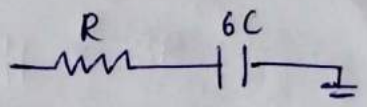


* Assume Scaling factor for p-mos = 2
n-mos = 1

* Make $R_{eff} = R$
scale $\omega = 2\omega$

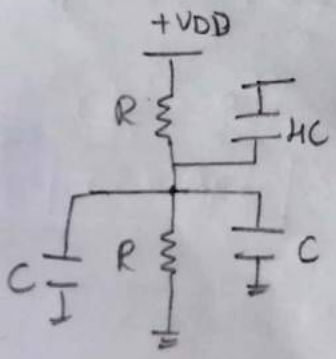
∴ p-mos is scaled by a factor of 4.
(previous 2 + present 2)

* Change the capacitor value (2C → 4C)



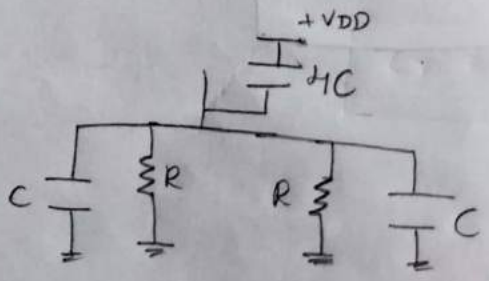
$\boxed{\tau_r = 6RC}$

ii) when A = 0, B = 1:



$\boxed{\tau_r = 6RC}$

when A = B = 1:



$R_{eff} = \frac{R}{2}$

$\tau_r = \frac{6RC}{2}$

$\boxed{\tau_f = 3RC}$

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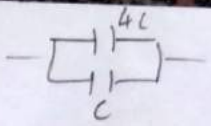
i/p capacitance = 5C

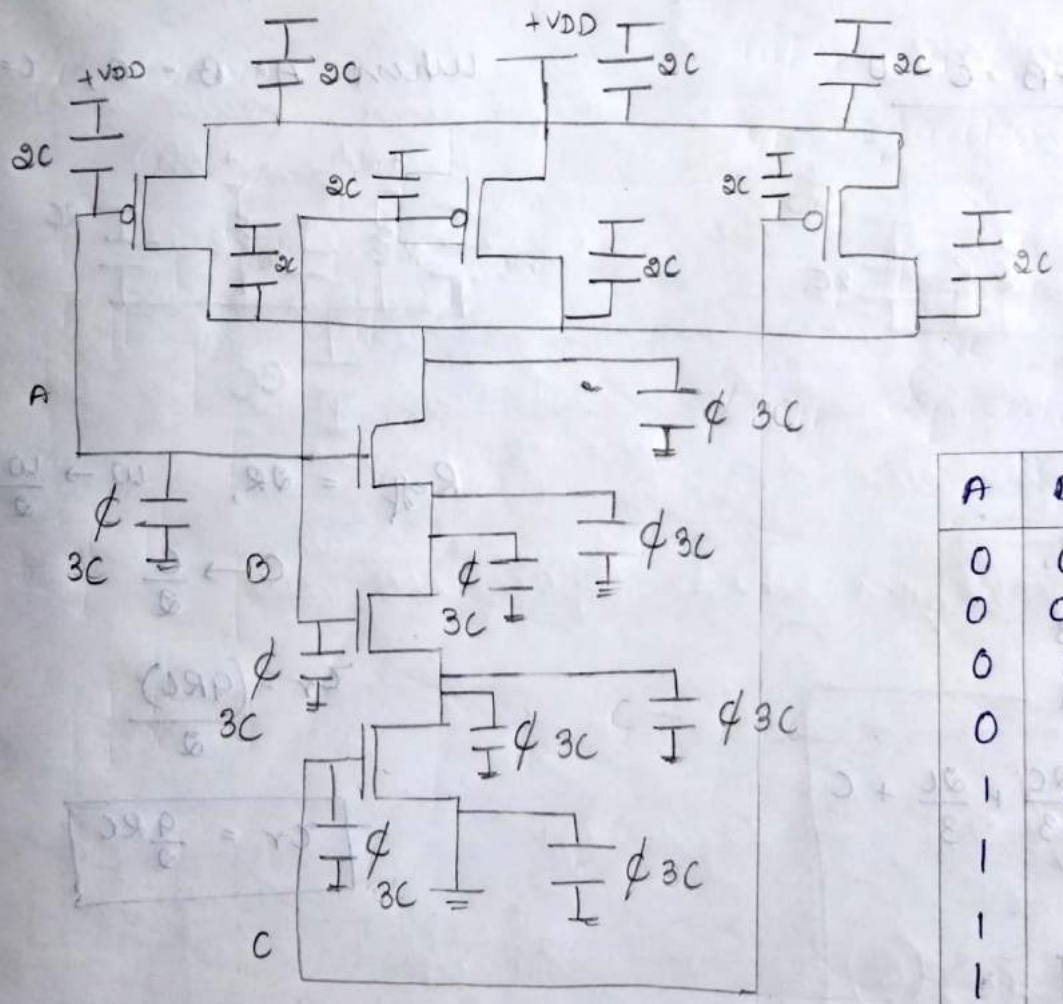
o/p capacitance = 6C



Inference:

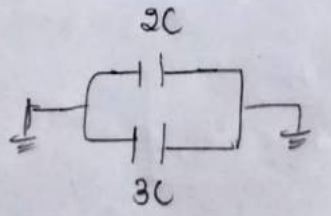
* Scaling is done only for series connection because if any one of the Transistor is off, then current will be zero (open circuit)
* For parallel connection - no scaling because, even if one transistor is ON, it will contribute equivalent resistance and current

3 i/p NAND:



A	B	C	
0	0	0	9RC
0	0	1	9/2 RC
0	1	0	9/2 RC
0	1	1	9RC
1	0	0	9RC
1	0	1	9/2 RC
1	1	0	9/2 RC
1	1	1	9RC

i/p capacitance :



= 5C

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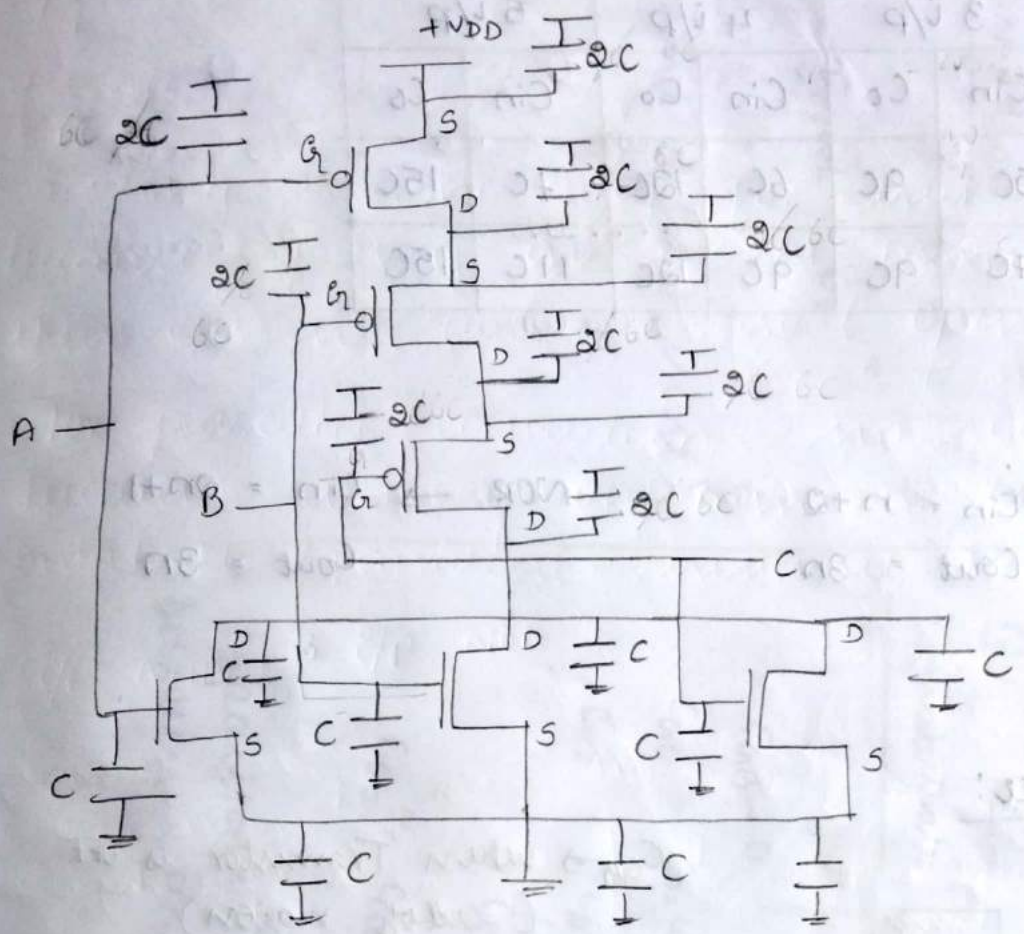
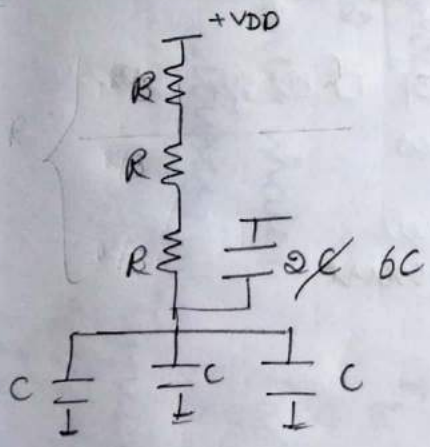
3 i/p NOR :



A	B	C	
0	0	0	9RC
0	0	1	9RC
0	1	0	9RC
0	1	1	9/2 RC
1	0	0	9RC
1	0	1	9/2 RC
1	1	0	9/2 RC
1	1	1	3RC

when $A = B = C = 0$



$R_{eff} = 3R$, $R = \frac{R}{3}$, $R_{eff} = R$.

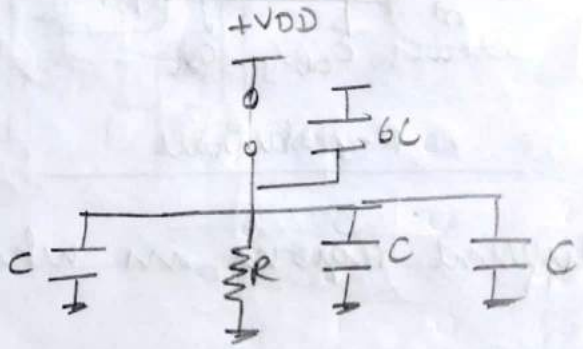
$\omega \rightarrow \cancel{\omega/3}\ 3\omega$

$C \rightarrow \cancel{\omega/3}\ 3\omega$

$2C \rightarrow 6C$

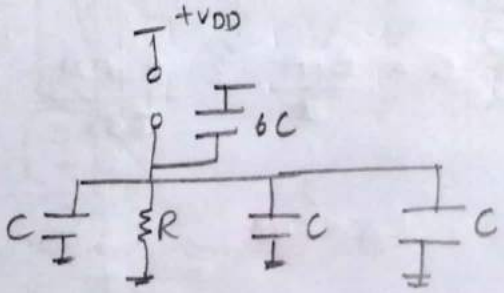
$\boxed{\tau = 9RC}$

when $A = B = 0$, $C = 1$



$\boxed{\tau = 9RC}$.

when $A = C = 0$, $B = 1$



$\boxed{\tau = 9RC}$.

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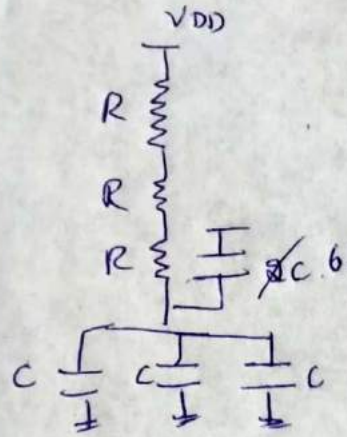
3 I/P NOR

* A = B = C = 0. (000)



$R_{eff} = 3R$

if $R = \frac{R}{3} \Rightarrow R_{eff} = R$.

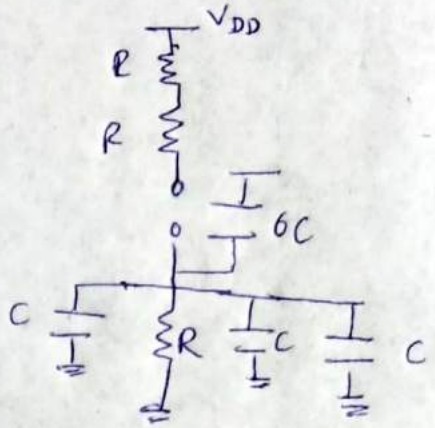
$W \rightarrow 3W$

$C \longrightarrow 3C$

$2C \longrightarrow 6C$

$\therefore \boxed{\tau = 9RC}$

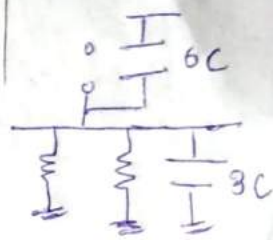
* A = B = 0, C = 1 (001)



$R_{eff} = R$.

$\boxed{\tau = 9RC}$

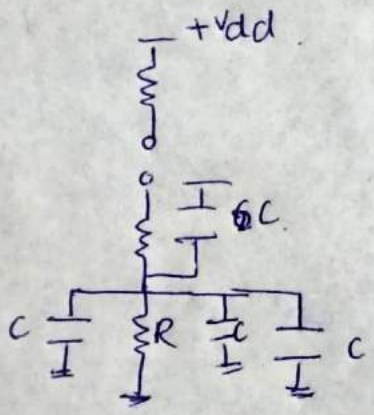
* 1010
* 011
and 110



$R_{eff} = R/2$
no. scaling

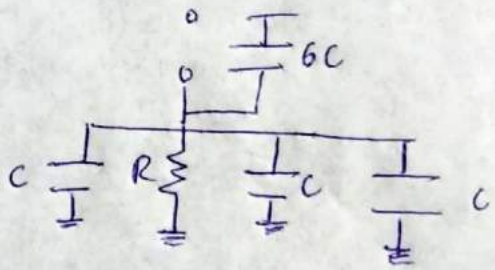
$\boxed{\tau = \frac{9}{2}RC}$

* A = C = 0, B = 1 (010)



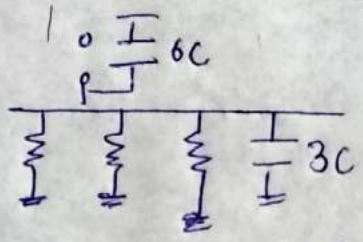
$\boxed{\tau = 9RC}$

* 100



$\boxed{\tau = 9RC}$

* ~~110~~ A = B = C = 1



$R_{eff} = R/3$ (no scaling)

$\tau = \frac{9}{3}RC \Rightarrow \boxed{\tau = 3RC}$

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Inference :

	2 i/p		3 i/p		4 i/p		5 i/p	
~~NAND~~	Cin	Co	Cin	Co	Cin	Co	Cin	Co
~~NOR~~ NAND	4C	6C	5C	9C	6C	12C	7C	15C
~~NAND~~ NOR	5C	6C	7C	9C	9C	12C	11C	15C

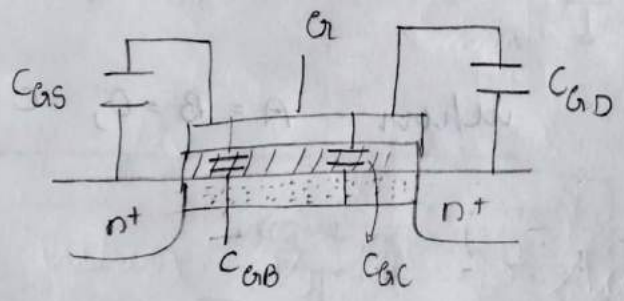
In general.

NAND $\longrightarrow$ $C_{in} = n+2$, $C_{out} = 3n$

NOR $\longrightarrow$ $C_{in} = 2n+1$, $C_{out} = 3n$

27/04/22

Gate Capacitance:



P- substrate

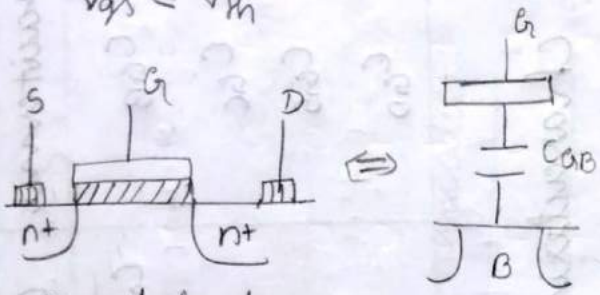
$C_{GB} \Rightarrow$ when Transistor is (cutoff region)

$C_{GC} \rightarrow$ Transistor ON (Linear region

Different regions in which capacitance exist

Cut - off region

$V_{GS} < V_{th}$



$C_{GB} = C_{ox} W L = C_0$

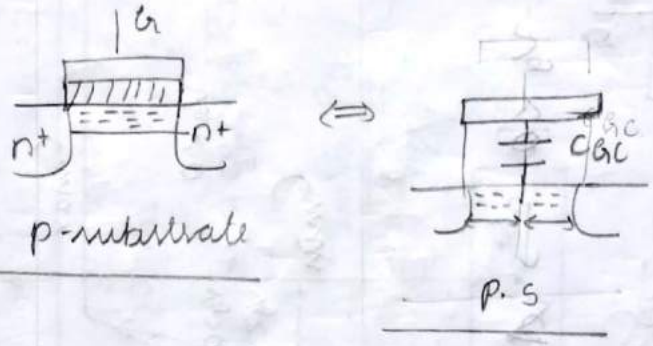
$C_{GC} = 0$

(channel doesn't exist)

Linear

$V_{GS} \geq V_{th}$

$V_{ds} < V_{GS} - V_{th}$



$C_{GB} = 0$

$C_{GC} = C_{ox} W L = C_0$

$C_{GC} = C_{GS} + C_{GD}$

$= C_{ox} W L = C_0$

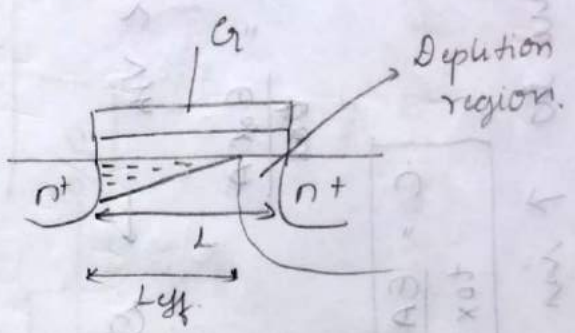
$C_{GS} = C_{GD} = \frac{C_{ox} W L}{2}$

* capacitance is evenly shared between drain & source

Saturation

$V_{GS} \geq V_{th}$

$V_{ds} > V_{GS} - V_{th}$



Depletion region → Drain & Body are in Reverse bias

no charge carrier present ($\frac{1}{3}^{rd}$ of channel)

$C_{GB} = 0$

$C_{GC} = C_{GS} + \cancel{C_{GD}}^{\,0}$ (absence of channel)

∴ no capacitance

$C_{GC} = C_{GS} = \frac{2}{3} C_{ox} W L$

$(1 - \frac{1}{3}) = \frac{2}{3}$

Typically channel exist only in $2/3^{rd}$ of Total channel region.

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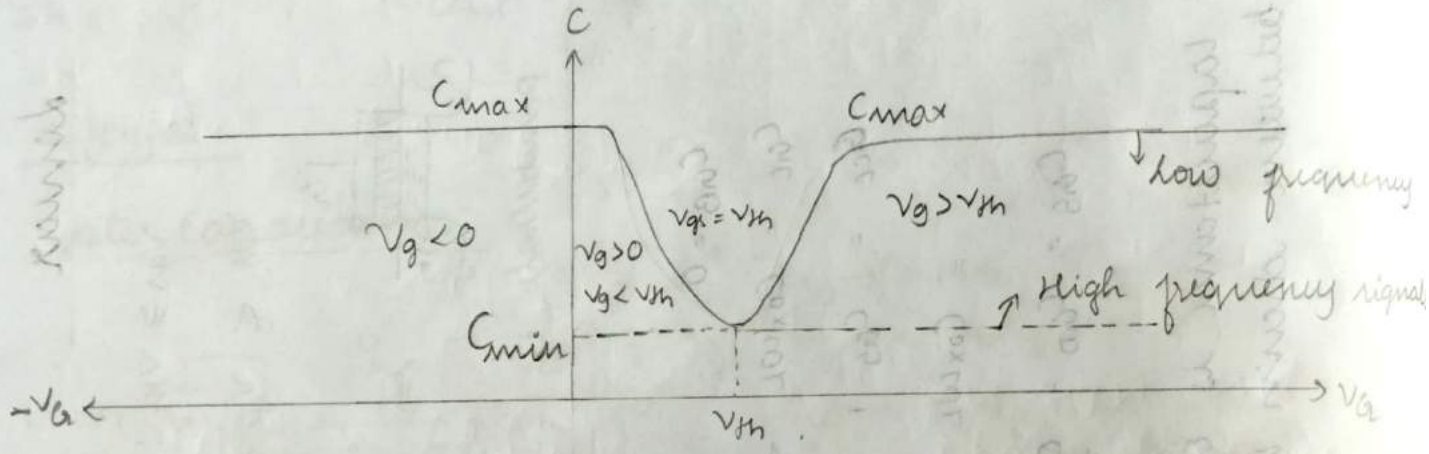
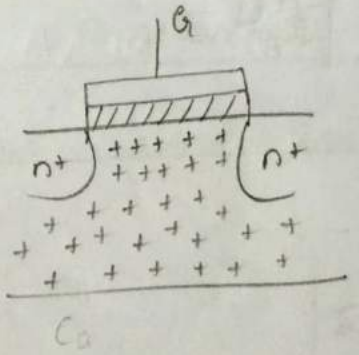
Capacitance	Cut - off	Linear	Saturation
C_{GB}	$C_{ox}WL = C_0$	0	0
C_{GC}	0	$C_{ox}WL = C_0$	$2/3\ C_{ox}WL$
C_{GS}	0	$1/2\ C_{ox}WL$	$2/3\ C_{ox}WL$
C_{GD}	0	$1/2\ C_{ox}WL$	0

C-V Characteristics (MOSFET → MOSCAP)



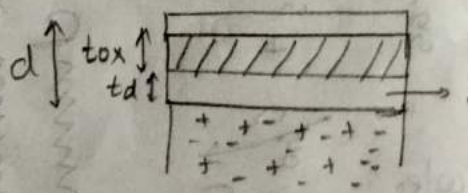
i] when $V_g < 0$ → Accumulation of charge carrier w.r.to. holes.



$C_{max} = C_{ox}WL$.

ii] $0 < V_g < V_{th}$ → Deplition

$$C = \frac{\epsilon_0 A}{d} = \frac{\epsilon_{ox} A}{t_{ox}}$$



~~$C_G = C_{ox}$~~

$$\boxed{C = \frac{\epsilon A}{t_{ox} + t_d}}$$

$\therefore d = t_{ox} + t_d$

C_G ↓ due to ↑ in distance.

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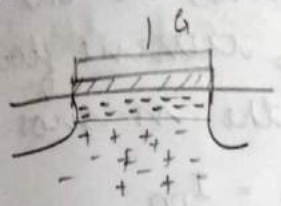
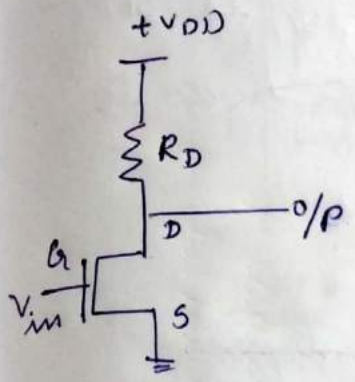
iii] $V_g > V_{th}$ → Inversion

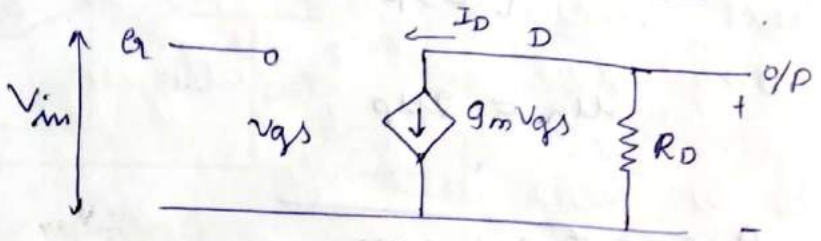


$$C = C_{ox} W L = C_{max}$$

Common - Source amplifier :



Small signal model :



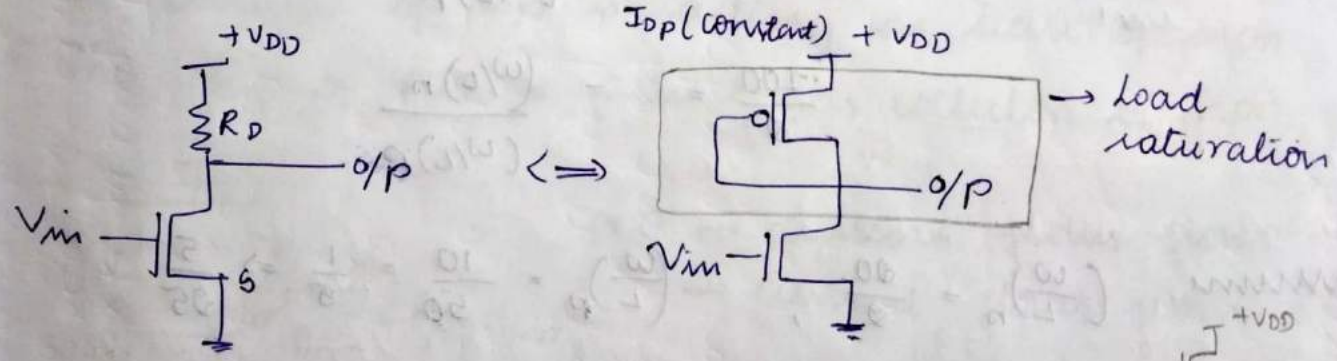
$$V_{in} = v_{gs}$$

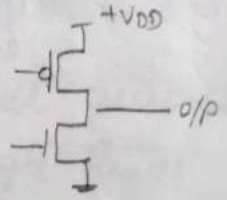
$$V_{out} = -g_m v_{gs} R_D$$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-g_m V_{gs} R_D}{V_{gs}}$$

$$\boxed{A_V = -g_m R_D}$$

Design of C.S. amplifier for a given gain





W.K.T, $A_V = -g_m R_D$

Replace R_D by Transconductance of p-mos

$$A_V = \frac{-g_{mn}}{g_{mp}}$$

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$$A_V = -\frac{\sqrt{\cancel{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \cancel{I_{Dn}}}}{\sqrt{\cancel{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \cancel{I_{Dp}}}}$$

when p-mos is on same I_{Dp} current flows through the n-mos

$\therefore I_{Dn} = I_{Dp}$

$$A_V = -\frac{\sqrt{\mu_n\left(\frac{W}{L}\right)_n}}{\sqrt{\mu_p\left(\frac{W}{L}\right)_p}}$$

$$\mu_n \simeq 2\mu_p$$

$$A_V = -\frac{\sqrt{2\cancel{\mu_p}\left(\frac{W}{L}\right)_n}}{\sqrt{\cancel{\mu_p}\left(\frac{W}{L}\right)_p}}$$

$$\boxed{A_V = -\sqrt{\frac{2\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}}}$$

-ve sign indicates Phase difference

Let $A_V = 10$,

$$+10 = -\sqrt{\frac{2(W/L)_n}{(W/L)_p}}$$

$$\frac{100}{2} = -\frac{(W/L)_n}{(W/L)_p}$$

assume, $\left(\frac{W}{L}\right)_n = \frac{20}{2}$, $\left(\frac{W}{L}\right)_p = \frac{10}{50} = \frac{1}{5} \Rightarrow \frac{5}{25}$

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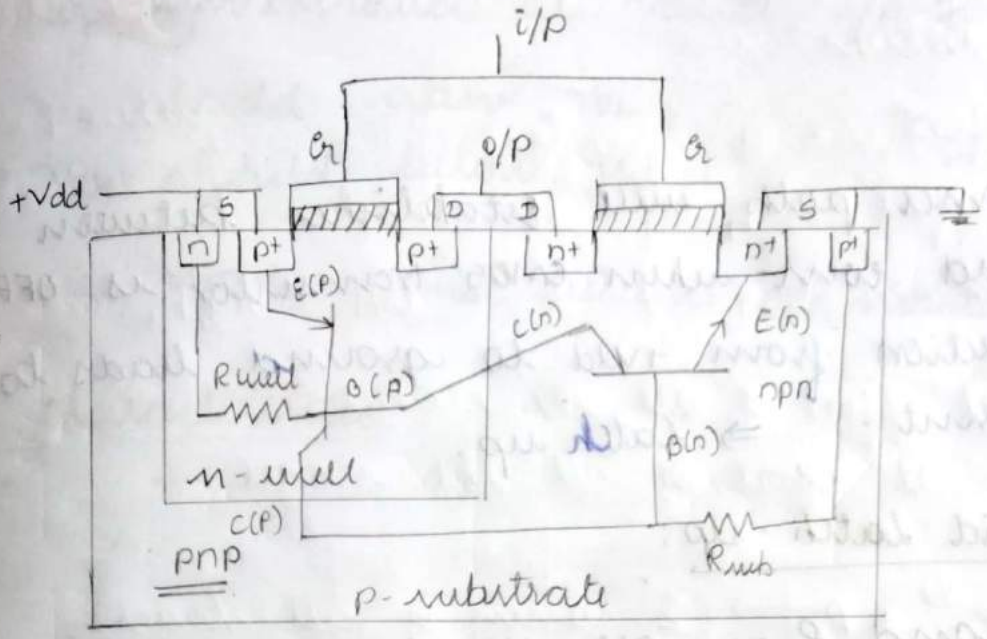
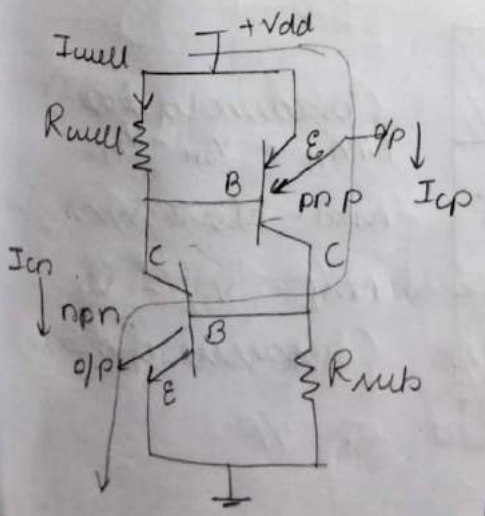
28/04/2022

Latch-up in CMOS inverter:



* CMOS inverter consist of two parasitic bipolars.
* p^+ diffusion (Emitter) + n-well (Base) + p substrate (collector) will form pnp transistor.
* n^+ diffusion (Emitter) + p substrate (base) + n-well (collector) will form npn transistor.
* R_{well} is the parasitic resistance in n-well structure
* R_{sub} is the substrate resistance.
* The collector of pnp is acting as base of npn
* The base of pnp is acting as collector of npn.



pnp → current flows from E→C
npn → current flows from C→E

* Due to +Vdd, some small current I_{well} will flows through R_{well}
* i/p drop across R_{well}
* R_{well} is connected to base of pnp
* ~~when~~ & pnp transistor is ON, I_{cp} current flows from Emitter to collector

Same thing happens in npn transistor.

* I_{cp} current will flows through R_{sub} and turn npn transistor to ON state.

Latch up:

* Least resistance path will establishes between $+V_{dd}$ and ground even when CMOS transistor is OFF
* Direct connection from +Vdd to ground leads to leakage current. ⇒ Latch up.

How to avoid Latch-up:

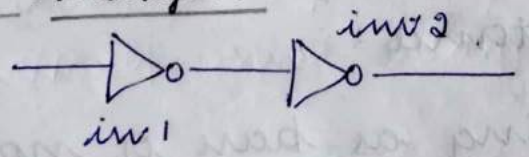
* If the R_{sub} and R_{well} are minimum, base of pnp doesn't have enough voltage to turn ON.

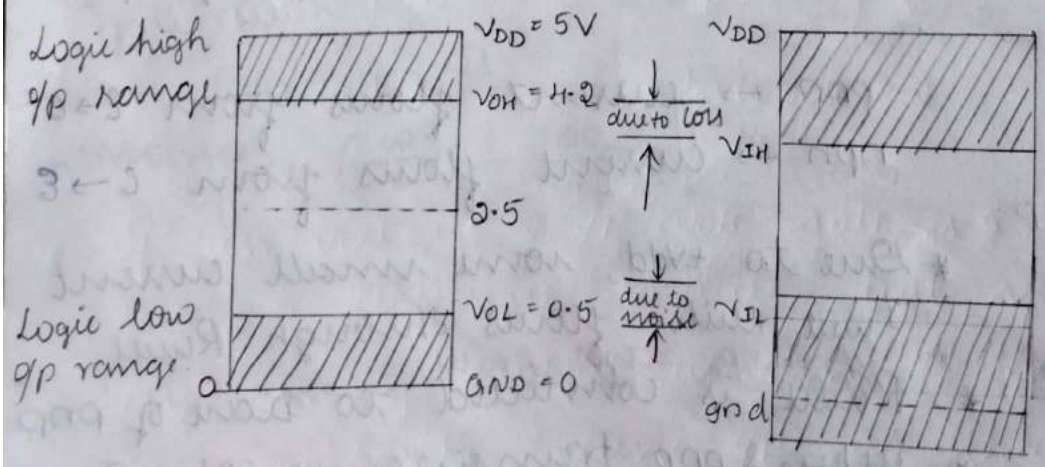
∴ no turn ON of pnp ⇒ no ON of npn.

* To reduce R_{sub} & R_{well}, ↑ the doping concentration

2. Guard rings. → Used in fabrication

Noise margin:





(because of loss)
$NM_H = V_{OH} - V_{IH}$

NM = Noise margin

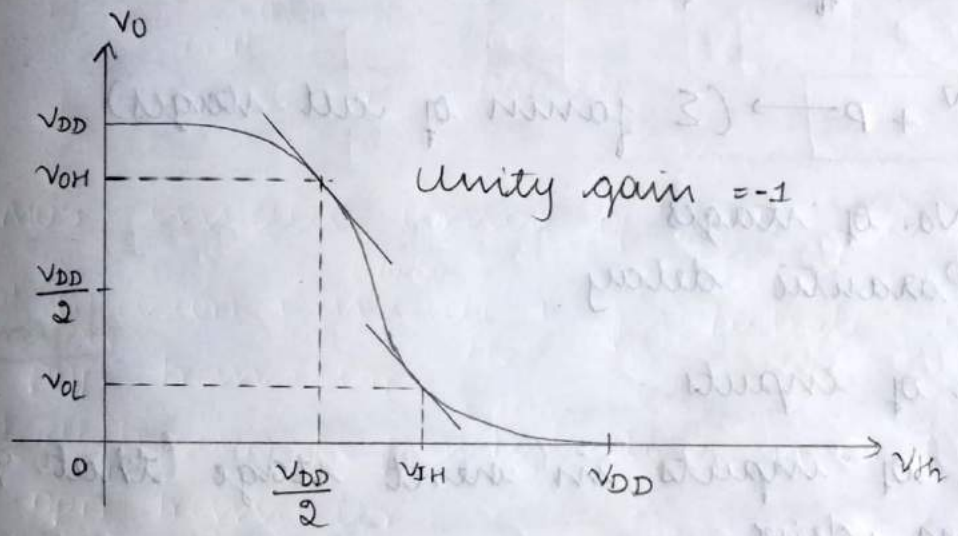
$NM_L = V_{IL} - V_{OL}$
(because of noise)

* V_{IH} should be less than V_{OH} Otherwise it won't take i/p.

* o/p of inv1 should be valid i/p for inv2.
  → V_{IL} should above V_{OL}
  → V_{IH} should below V_{OH}.

* Noise margin exist because of noise.

DC characteristics:



* High skew → Beta ratio > 1 $\left(> \frac{V_{dd}}{2} \right)$
* Low skew → Beta ratio < 1 $\left(< \frac{V_{dd}}{2} \right)$
* No skew → Beta ratio = 1 $\left(= \frac{V_{dd}}{2} \right)$

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Performance estimation :

* Delay estimation

corresponds to single stage

- Logical effort = g
- Electrical effort = h
- Path effort = f

$G = \pi g_i$ where $i = 1, 2$

$H = \pi h_i$

$F = GH = \pi g_i h_i$.

G = Logical effort of all the stages

H = Electrical effort of all the stages

Delay $\boxed{D = NF^{1/N} + P}$ → (Σ fanin of all stages)

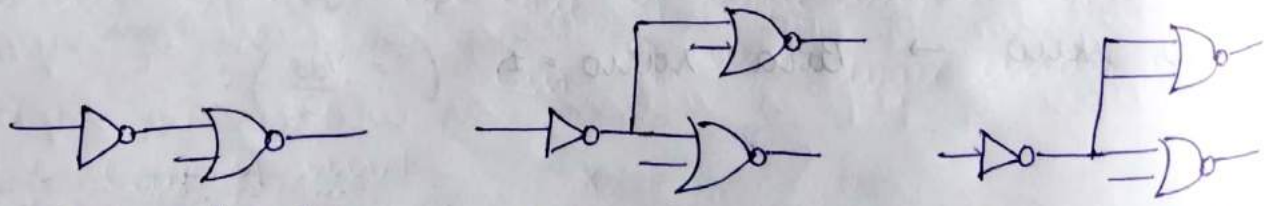
where N = No. of stages

P = Parasitic delay.

Fanin = No. of inputs.

Fanout = No. of inputs in next stage that o/p can drive.

* It is the capability of device driving the no. of i/p of next stage.



Fan out = 1. Fan-out = 2. Fan-out = 3

* If fan-out of 2 i/p NOR gate is 5, then it can drive 5 different inputs. but still o/p of NOR is 1
* By using Buffer we can ↑ the fan-out which can gives the same o/p as that of i/p.

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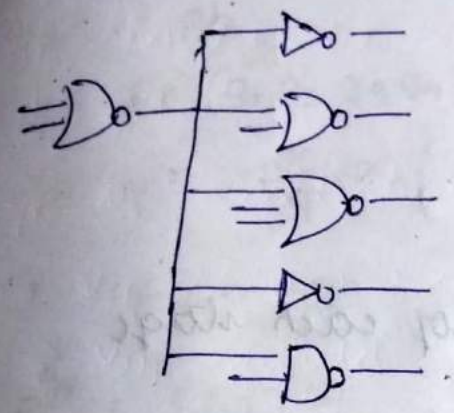
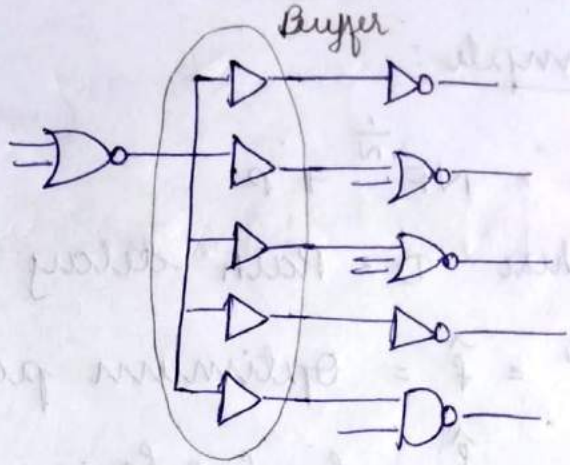


$\Rightarrow$



Logical effort $g = \dfrac{C_{in} \text{ of logic under consideration}}{C_{in} \text{ of inverter}}$

NOTE: 'g' is constant for particular logic and only 'h' will changes

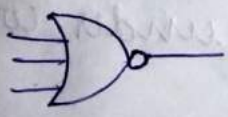
$h = \dfrac{C_{out} \text{ of the logic under consideration}}{C_{in} \text{ of the same logic under consideration}}$

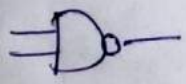
Example:

i Consider a inverter, $g = \dfrac{3C}{3C} = 1$.

Logical effort of inverter is always 1.

ii] $g = \dfrac{5C}{3C} = \dfrac{5}{3}$ $\dfrac{C_{in} \text{ of 2 i/p NOR}}{C_{in} \text{ of inverter}}$

iii]  $g = \dfrac{7C}{3C} = \dfrac{7}{3} \Rightarrow \dfrac{C_{in} \text{ of 3 i/p NOR}}{C_{in} \text{ of inverter}}$

iv]  $g = \dfrac{4C}{3C} = \dfrac{4}{3} \Rightarrow \dfrac{C_{in} \text{ of 2 i/p NAND}}{C_{in} \text{ of inverter}}$

generally, for NAND $\Rightarrow \dfrac{n+2}{3}$ n = no. of i/p.

NOR $\Rightarrow \dfrac{2n+1}{3}$.

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Example:

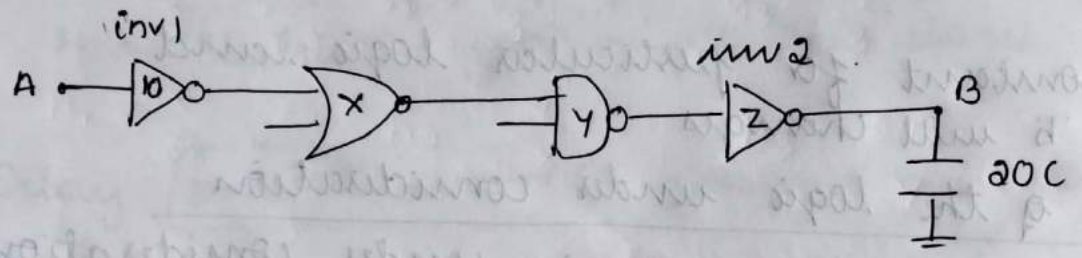
$$D = NF^{\frac{1}{N}} + P$$

where D = Path delay

$F^{\frac{1}{N}} = \hat{f}$ = Optimum path effort of each stage

$\hat{f} = f_1 = f_2 = f_3 \ldots$

1. Find out Path delay for the given circuit -



→ N=4, $g_1 = 1$ $g_2 = \frac{5}{3}$ $g_3 = \frac{4}{3}$ $g_4 = 1$.

10 = C_{in} of the inv1.

X = C_{in} of the 2 i/p NOR = C_{out} of inv1 (w.r.to each i/p

Y = C_{in} of the 2 i/p NAND = C_{out} of 2 i/p NOR

Z = C_{in} of inv2 = C_{out} of 2 i/p NAND.

Electrical effort, $h_0 = \frac{C_{out} \text{ of logic under considera}^n}{C_{in} \text{ of same logic under consider}^n}$

$$h_1 = \frac{C_{out} \text{ of inv1}}{C_{in} \text{ of inv1}} = \frac{X}{10}$$

$$h_2 = \frac{C_{out} \text{ of 2 i/p NOR}}{C_{in} \text{ of 2 i/p NOR}} = \frac{Y}{X}$$

$$h_3 = \frac{C_{out} \text{ of 2 i/p NAND}}{C_{in} \text{ of 2 i/p NAND}} = \frac{Z}{Y}$$

$$h_4 = C_{out} \text{ of inv2} / C_{in} \text{ of inv2} = \frac{20}{Z}$$

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$F = gh$

$F = (g_1 g_2 g_3 g_4) \times (h_1 h_2 h_3 h_4)$

$= \frac{20}{9} \times \left(\frac{20 \times YZ}{10 \times YZ}\right)$

$F = \frac{40}{9}$

$\hat{f} = F^{1/N} = \left[\frac{40}{9}\right]^{1/4} = \underline{\underline{1.452}}$

$D = N F^{1/N} + P$. $P = 6$ (Tanin of all stages)

$D = 4 \times 1.452 + 6$

$D = 11.808$

$\boxed{D \simeq 12}$.

$\hat{f} = f_1 = f_2 = f_3 = f_4 = 1.452$

* $f_1 = g_1 h_1 = \frac{X}{10}$

$X = 10 \times 1.452$

$\boxed{X = 14.52}$

* $f_2 = g_2 h_2 = \frac{5}{3} \times \left(\frac{Y}{X}\right)$

$\frac{1.452 \times 3 \times 14.52}{5} = Y$.

$\boxed{Y = 12.64}$

* $f_3 = g_3 h_3 = \frac{4}{3} \times \frac{Z}{Y}$

$Z = \frac{3 f_3 Y}{4}$

$Z = \frac{3 \times 1.452 \times 12.64}{4}$

$\boxed{Z = 13.76}$

* $f_4 = g_4 h_4 = \frac{20}{Z}$.

$Z = \frac{20}{1.452}$

$\boxed{Z = 13.77}$

$f_1 = g_1 h_1$

$1.452 = 1 \times \frac{(X)}{C_{in}}$

$C_{in} = \frac{14.52}{1.452} = \underline{\underline{10}}$

* when i/p capacitance = 10, we need to scale the ckt.

For p-mos → 6.5 (2×3.33)

n-mos → 3.5 (1 × 3.33)

we have to multiply same factor for both p-mos and n-mos.

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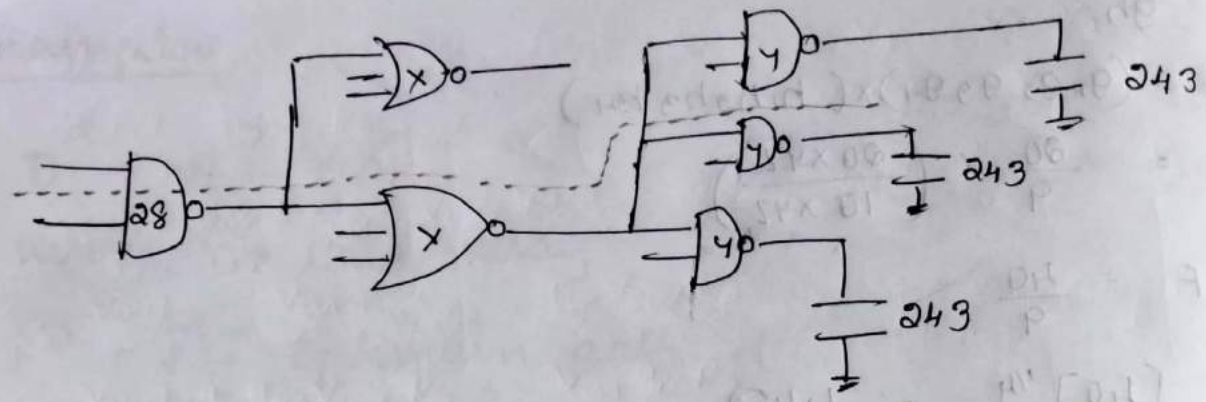
2]



→ $N = 3$, $F = GHB$ where B = branches $(2 \times 3 = 6)$

$g_1 = \frac{4}{3}$, $g_2 = \frac{7}{3}$ $g_3 = \frac{4}{3}$

$h_1 = \frac{X}{28}$, $h_2 = \frac{Y}{X}$ $h_3 = \frac{243}{Y}$

$F = (g_1 g_2 g_3)\times(h_1 h_2 h_3)\,6$

$= \left(\frac{4}{3} \times \frac{7}{3} \times \frac{4}{3}\right) \times \left(\frac{X}{28} \cdot \frac{Y}{X} \cdot \frac{243}{Y}\right) \times 6$

$= 4.148 \times 8.67 \times 6$

$\boxed{F = 216}$

$\hat{f} = F^{1/N} = F^{1/3} = \sqrt[3]{216} = 6$

$\hat{f} = f_1 = f_2 = f_3 = 6$

$D = NF^{1/N} + P$

$D = 18 + 7$

Based on path $P = (2 + 3 + 2) = 7$.

$\boxed{D = 25}$

* $f_3 = g_3 h_3 B$ (no. of branch that o/p has)

$6 = \frac{4}{3} \times \frac{243}{Y} \times 1$

$\boxed{Y = 54}$

* $f_2 = g_2 h_2 \times 3$ (no. of branch that 2nd stage o/p has)

$6 = \frac{7}{3} \times \left(\frac{Y}{X}\right) 3$

$\boxed{X = 63}$

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If the circuit has branches,

$F = GHB$

, while calculating unknown i/p capacitance → we need to multiply with no. of branches.

$f_1 = g_1 h_1$

$6 = \frac{4}{3} \times \left(\frac{x}{28}\right)$

$\boxed{x = 126}$

$f_2 = g_2 h_2$

$6 = \frac{7}{3} \times \frac{y}{x}$

$y = \frac{18 \times 126}{7}$

$\boxed{y = 324}$

$f_1 = g_1 h_1$

$6 = \frac{4}{3} \times \frac{126}{C_{in}}$

If we consider from i/p side

$\boxed{C_{in} = 28}$

$f_1 = g_1 h_1 \times 2$ → no of branches at 1st stage o/p

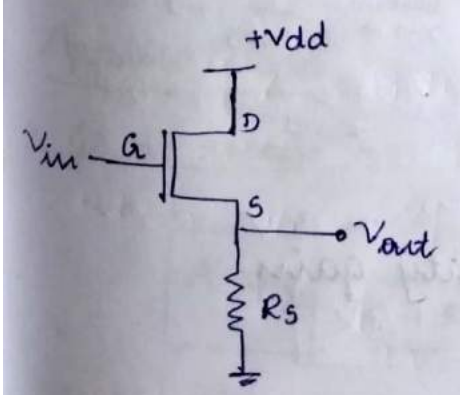
$6 = \frac{4}{3} \times \frac{63}{C_{in}} \times 2$

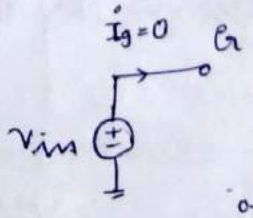
→ If we consider from o/p side

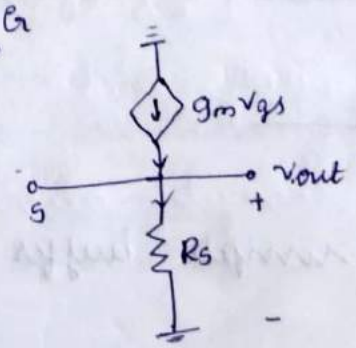
$\boxed{C_{in} = 28}$

10/05/22

Common - Drain Amplifier : For small signal, Vdd doesn't change with time ∴ replace +Vdd by gnd







Small signal model

$V_{out} = IR_S$

$V_{out} = g_m V_{gs} R_S$

$V_{out} = g_m (V_{in} - V_{out}) R_S$

$V_{gs} = V_g - V_S$

$V_{gs} = V_{in} - V_{out}$.

$V_{out} = V_{in} g_m R_S - g_m V_{out} R_S$

$V_{out} + g_m V_{out} R_S = V_{in} g_m R_S$

$V_{out} (1 + g_m R_S) = V_{in} g_m R_S$

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S}$$

$$\boxed{A_V = \frac{g_m R_S}{1 + g_m R_S}}$$

Input impedence, $R_{in} = \infty$, $R_{out} = ?$

* If we keep $(g_m R_S) \to \infty$

$$A_V = \frac{g_m R_S}{1 + g_m R_S}$$

A/c to L-Hospital rule, differentiate numarator and denaminator w.r.to. $g_m R_S$

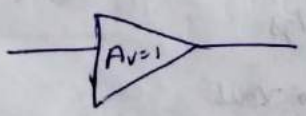
$$A_V = \frac{1}{0+1}$$

$$\boxed{A_V = 1}$$

$$\lim_{x \to \infty} \frac{g_m R_S}{g_m R_S \left(\frac{1}{g_m R_S} + 1\right)}$$

$$\lim_{x \to \infty} \frac{1}{\frac{1}{g_m R_S} + 1}$$

$$= \underline{\underline{1}}$$



This acts as simple buffer with unity gain.

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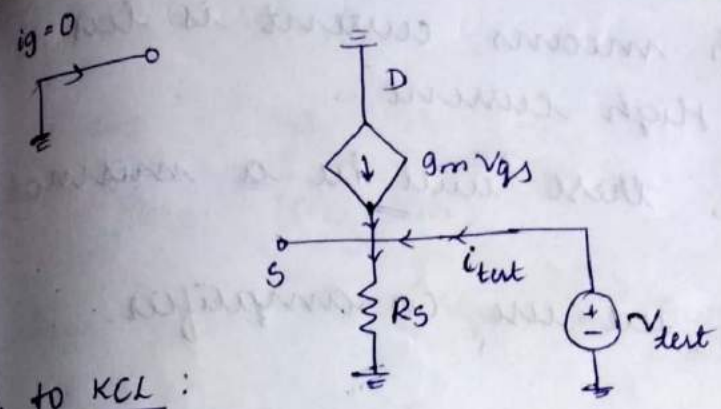


To find R_{out}, ground v_{in}, and apply v_{test} & i_{test} at o/p

A/c to KCL :

$$i_{test} = -g_m v_{gs} + \frac{v_{test}}{R_S}$$

$$v_{gs} = v_g - v_s$$
$$= 0 - (v_{test})$$
$$v_{gs} = -v_{test}$$

$$= -g_m(-v_{test}) + \frac{v_{test}}{R_S}$$

$$i_{test} = g_m v_{test} + \frac{v_{test}}{R_S}$$

$$i_{test} = (R_S g_m v_{test} + v_{test}) / R_S$$

$$i_{test} = \frac{(1 + R_S g_m) v_{test}}{R_S}$$

$$\boxed{R_o = \frac{v_{test}}{i_{test}} = \frac{R_S}{1 + g_m R_S}}$$

If $g_m R_S \to \infty$, $R_o = \text{min}$.

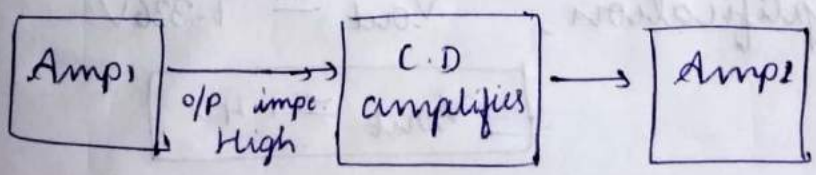
$$R_{in} = \frac{v_{in}}{0} = \infty$$

Inference:

* CD amplifier has high input impedence
* Low o/p impedence.
* It is a unity gain amplifier * Phase shift is zero.

Applications:

* It is used in Impedence matching.



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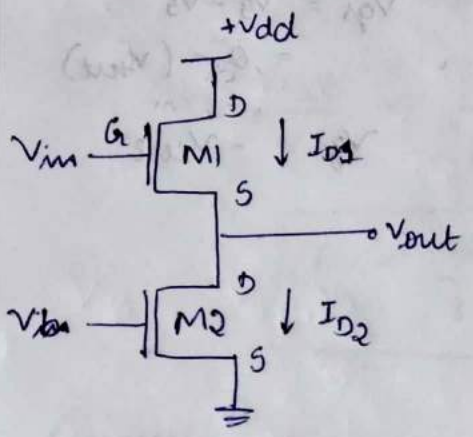
If o/p impedance high means, current is less
Low i/p impedance ⇒ High current.
∴ In cascaded circuit, there will be a mismatch in the current.
In order to solve this, we use CD amplifier.

Design :



M1 and M2 are in saturation

$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{gs} - V_{th})^2$$

$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left((V_{in} - V_{out}) - V_{th}\right)^2$$

given

$$\mu_n = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}}$$ 3.9

Assume, $V_{th} = 0.7$, $V_{in} = 0.5V$
$I_{D_1} = 0.5mA$

Specifications : $\mu_n = 0.045832\ m^2$
$T_{ox} = 1.39 \times 10^{-8}\ m$
$\varepsilon_0 = 8.854 \times 10^{-12}\ F/m$
$\varepsilon_r = 3.9$
$C_{ox} = 2.484 \times 10^{-3}\ F$
$\left(\frac{W}{L}\right)_1 = 1$

$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left((V_{in} - V_{out}) - V_{th}\right)^2$$

$$0.5 \times 10^{-3} = \frac{1}{2}(0.045832)(2.484 \times 10^{-3})(1)\left((0.5 - V_{out}) - 0.7\right)^2$$

After simplification, $V_{out} \simeq 1.336V$

$$\boxed{V_{out} \simeq 1.4V}$$

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$I_{D2} = I_{D1}$

$V_{ds2} = V_{gs} - V_{th}$.

$V_{ds_2} = (V_b - V_{th})$

$I_{D2} = \frac{1}{2} \mu_n C_{ox} (V_{gs} - V_{th})^2 \left(\frac{W}{L}\right)_2$

$= \frac{1}{2} \mu_n C_{ox} (V_b - V_{th})^2 \left(\frac{W}{L}\right)_2$

$I_{D2} = \frac{1}{2} \mu_n C_{ox} (V_{out})^2 \left(\frac{W}{L}\right)_2$.

For M_2,

$V_{gs} - V_{th}$

$= V_b - V_{th}$

$\boxed{V_{ds} = V_{out}}$

V_{out} is the voltage across drain & source of M_2

$0.5 \times 10^{-3} = \frac{1}{2} (0.045832) (2.484 \times 10^{-3}) (1.4)^2 \left(\frac{W}{L}\right)_2$.

$\left(\frac{W}{L}\right)_2 = 4.92$.

Let $L = 4$, $W \simeq 20$.

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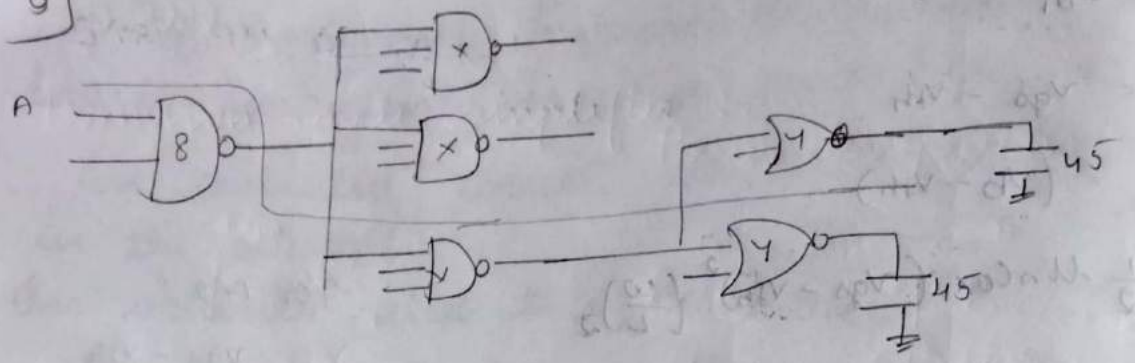
Q



$N = 3$

$g_1 = \frac{4}{3}$ $\quad g_2 = \frac{5}{3}$ $\quad g_3 = \frac{5}{3}$

$h_1 = \frac{x}{8}$ $\quad h_2 = \frac{y}{x}$ $\quad h_3 = \frac{45}{y}$

$F = GHB$

$= \left(\frac{4}{3} \times \frac{5}{3} \times \frac{5}{3}\right)\left(\frac{x}{8} \times \frac{y}{x} \; \frac{45}{y}\right) \times 6$

$\boxed{F = 125}$

$F^{1/3} = 5 = f_1 = f_2 = f_3$

$D = NF^{1/N} + P$

$= (3 \times 5) + 7$

$\boxed{D = 22}$

$f_1 = g_1 h_1 b$

$5 = \frac{4}{3} \times \frac{x}{8} \times 3$

$\boxed{x = 10}$

$f_2 = g_2 h_2 b$

$5 = \frac{5}{3} \times \frac{y}{10} \times 2$

$\boxed{y = 15}$

$f_3 = g_3 h_3 b$

$5 = \frac{5}{3} \times \frac{45}{y} \times 1$

$\boxed{y = 15}$

$f_2 = g_2 h_2 b$

$5 = \frac{5}{3} \times \frac{15}{x} \times 2$

$\boxed{x = 10}$

$f_1 = g_1 h_1 b$

$5 = \frac{4}{3} \times \frac{10}{C_{in}} \times 3$

$\boxed{C_{in} = 8}$

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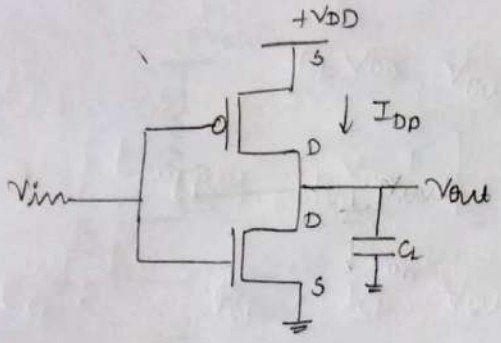
18/05/22

Power Dissipation :

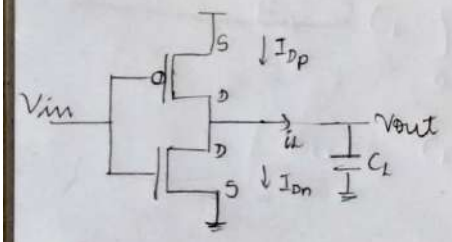


Power dissipation = $P_{static} + P_{dynamic}$

$P_{dynamic}$ → $P_{switching}$:
* Charging & discharging of C_L
⇒ capacitor comes into picture

→ $P_{short\ circuit}$:
when both the transistors are ON, least resistance path will establish b/w +Vdd and ground.

Static Dissipation :



Load current $i_L = 0$
when $I_{DP} = I_{Dn}$.

$$i_L = C_L \frac{dv}{dt} = 0.$$

i. when $v_{in} = 0$,
P-mos becomes ON. and n-mos ~~becomes~~ is OFF
⇒ current flowing through n-mos is zero i.e. $I_{Dn} = 0$
since $I_{Dn} = I_{DP}$, $I_{DP} = 0$.

ii when $v_{in} = 1$,
P-mos - OFF, n-mos - ON, ⇒ $I_{DP} = 0$ ⇒ $I_{Dn} = I_{DP} = 0$

* when any one of the transistor is OFF, circuit will not deliver any current from the supply.
∴ Power dissipation is zero.

* $P_{static} = 0$ - Ideally (for long channel transistor)
* $P_{static} \neq 0$ for short channel (Some leakage in the device)

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Practically, $P_{static} \neq 0$, because

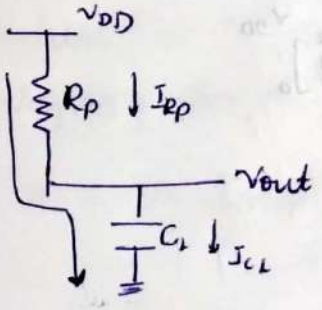
Leakage current
- → Tunneling current ($I_g \neq 0$)
- → Junction current (Punch through)
- → Subthreshold conduction
  [$V_{gs} < V_{th}$ · n-mos]

Dynamic dissipation :

$P_{dynamic}$
- → $P_{switching}$
- → $P_{short\ circuit}$

$P_{switching}$:

1. $V_{in} = 0$



when $V_{in} = 0$, n-mos · OFF, p-mos · ON

* dissipation happens in resistor (R_p)
* capacitor C_L, stores the energy.

$$E_{supply} = E_{dissipated}\big|_{pmos} + E_{CL}$$

$$E_{dissipation}\big|_{pmos} = E_{supply} - E_{CL}$$

E_{supply},

$$P_{supply} = I \cdot V$$
$$= I_{supply} \cdot V_{DD}$$
$$= I_{CL}\ V_{DD}.$$

$$I_{supply} = I_{R_p} = I_{CL} = C_L \frac{dV}{dt}$$

$$P_{supply} = C_L \cdot \frac{dV_{out}}{dt} \cdot V_{DD}$$

$$E_{supply} = \int_0^\infty P_{supply} \cdot dt = \int_0^\infty C_L \frac{dV_{out}}{dt} \cdot V_{DD} \cdot dt = V_{DD} C_L \int_0^\infty dV_{out}$$

[C_L → capacitance is constant, but voltage across the capacitor will varies.]

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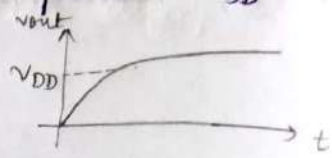
Change limits → 0 to V_{DD}.

$V_{out_{max}} = V_{DD}$

Capacitor can charge upto V_{DD}



$$E_{supply} = C_L V_{DD} \int_0^{V_{DD}} dV_{out}$$

$$= C_L V_{DD} V_{out} \Big]_0^{V_{DD}}$$

$$\boxed{E_{supply} = C_L V_{DD}^2}$$

E_{C_L} :

$$P_{C_L} = I_{C_L} \cdot V_{out} = C_L \frac{dV_{out}}{dt} \cdot V_{out}$$

$$E_{C_L} = \int_0^{\infty} P_{C_L} \cdot dt = \int_0^{\infty} C_L \cdot \frac{dV_{out}}{\cancel{dt}} \cdot V_{out} \cdot \cancel{dt}$$

$$E_{C_L} = C_L \int_0^{\infty} dV_{out} \cdot V_{out}$$

Change the limits, (0 to V_{DD})

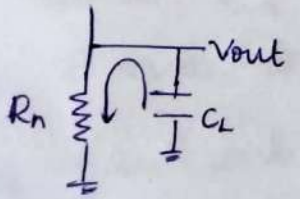
$$E_{C_L} = C_L \int_0^{V_{DD}} V_{out} \cdot dV_{out} = C_L \left[\frac{V_{out}^2}{2}\right]_0^{V_{DD}}$$

$$\boxed{E_{C_L} = \frac{C_L V_{DD}^2}{2}}$$

Power dissipation during charging,

$$E_{dissipation} = C_L V_{dd}^2 - \frac{1}{2} C_L V_{dd}^2 = \frac{1}{2} C_L V_{dd}^2$$

ii) when $V_{in} = 1$



$$E_{initial} = \frac{1}{2} C_L V_{dd}^2.$$

Current flows from load to ground during discharging.

$$E_{final} = 0.$$

Complete energy $\left(\frac{1}{2} C_L V_{dd}^2\right)$ will discharge at resistor R_n

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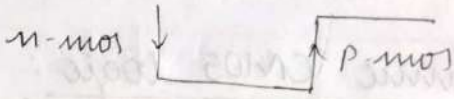
$$E_{dissipation} = E_{dissipation\,(p\text{-}mos)} + E_{dissipation\,(n\text{-}mos)}$$

$$= \frac{1}{2} C_L V_{dd}^2 + \frac{1}{2} C_L V_{dd}^2$$

$$\boxed{E_{dissipation} = C_L V_{dd}^2}$$



Average power dissipation, $P_{avg} = \dfrac{E_{dissipation}}{Time}$

$$= \frac{1}{T} \cdot C_L V_{dd}^2$$

For one clock period $\boxed{P_{average} = f C_L V_{dd}^2}$

In general, $\boxed{P_{\substack{average \\ switching}} = \alpha f C_L V_{dd}^2}$

where α = activity factor (gives how many times charging and discharging happens for every clock period)

If $\alpha = 1$ → Every clock pulse have charging and discharging for 1 time

α should be ≤ 1. $\boxed{\alpha \leq 1}$

<u>$P_{short\ circuit}$</u> :

$$P_{SC} = I_{supply} \cdot V_{DD}$$

$$\boxed{P_{SC} = \frac{\beta}{12} (V_{DD} - V_{th})^3 \tau_f}$$

Total power, $P_T = P_{static} + P_{dynamic}$

$$P_T = P_{leakage} + (P_{switching} + P_{short\ circuit})$$

$$\boxed{P_T = P_{leakage} + \left(\alpha C_L V_{dd}^2 f + \left(\frac{\beta}{12} (V_{DD} - V_{th})^3 \tau_f\right)\right)}$$

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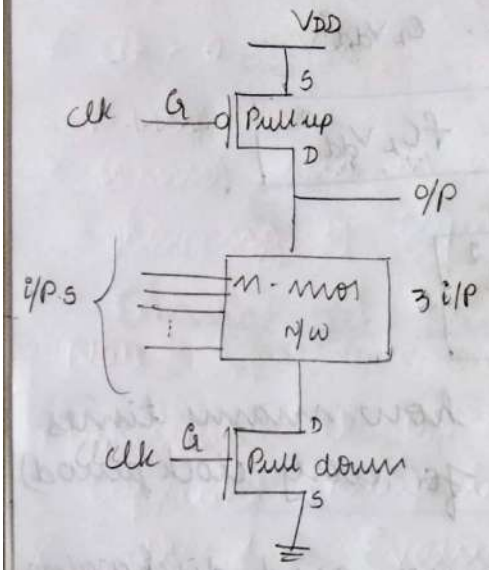
Drawback of CMOS logic :

As the no. of transistor increases in the CMOS logic circuit complexity increases, leads to power dissipation

Dynamic CMOS logic :

* Dynamic CMOS logic is used to reduce the no. of transistor which interns reduces the power dissipation.



For 3 i/p NAND gate :

CMOS logic : 3 pmos + 3 n-mos

Totally 6 transistors are required.

Dynamic CMOS logic :

n-mos N/w - 3 i/p
n-mos - 1 i/p
p-mos - 1 i/p

Totally 5 i/p

For 4 i/p NAND gate :

CMOS logic : 4P + 4N = 8 transistors required.

Dynamic CMOS logic : n-mos N/w - 4 i/p
n-mos - 1 i/p
p-mos - 1 i/p

6 i/p

In generally, for dynamic CMOS logic, no. of Transistor

$= (n+2)$ or $((\underbrace{n+1}_{n\text{-mos}}) + \underbrace{1}_{p\text{-mos}})$ Transistor

For CMOS logic, no. of transistor = $2n$

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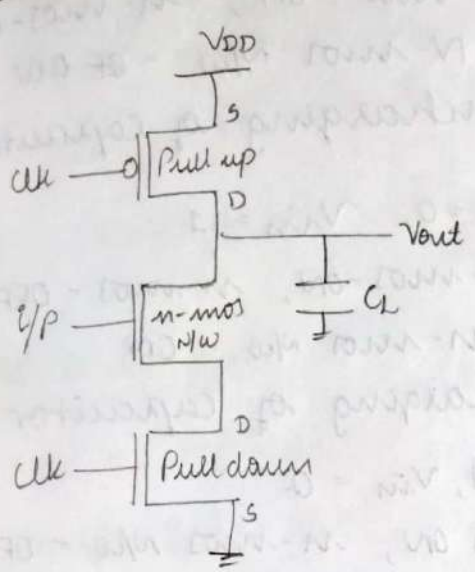
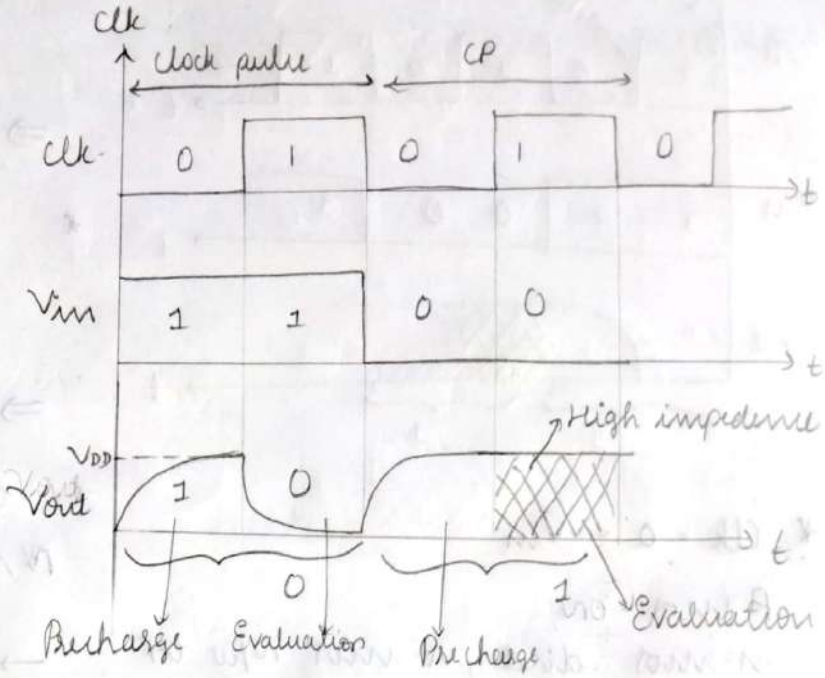
Inverter:





* Same clk i/p will go for both Pull up & Pull down transistor

* when clk = 0 and V_{in} = 1.

  P-mos becomes ON, N-mos OFF, n-mos N/w ON capacitor will charge to max. and Transition is due to charging of RC component).

* when clk = 1, and V_{in} = 1.

  n-mos and n-mos N/w → ON, P-mos - OFF. discharging of capacitor takes place.

* when clk = 0, and V_{in} = 0.

  P-mos - ON, n-mos and n-mos N/w - OFF.
  ⇒ Charging of capacitor.

* when clk = 1, and V_{in} = 0.

  Pull down transistor - ON, Pull up & n-mos N/w - OFF Circuit doesn't have any path for charging or discharging. o/p remains constant / retain. becomes high impedance region.

* At the end of the clock pulse, for V_{in} = 1, → V_{out} = 0, for V_{in} = 0, → V_{out} = 1.

* ∴ Dynamic cmos logic works properly as that of cmos logic

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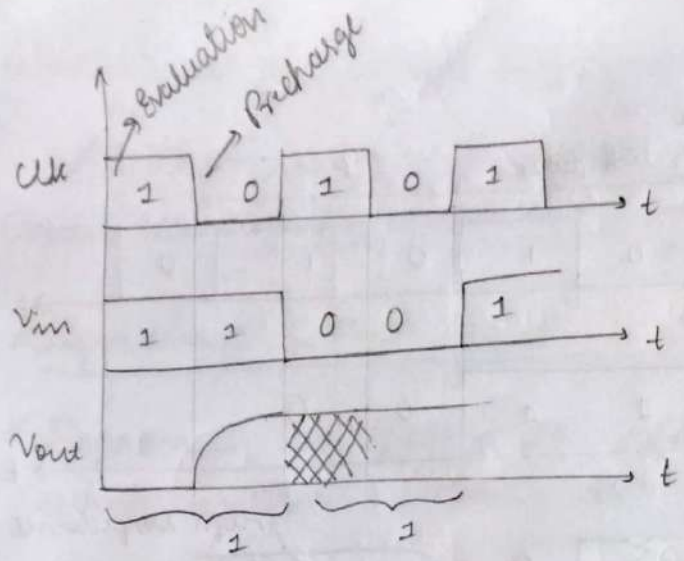


* Clk = 0 = Vin

P-mos - ON,
n-mos and n-mos N/w - OFF
⇒ Charging of capacitor

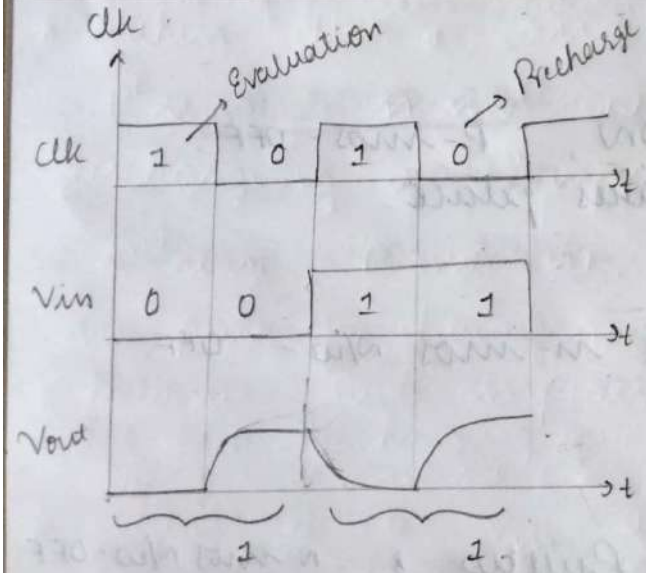
* Clk = 1, Vin = 1
P-mos - OFF, n-mos - ON
N-mos N/w - ~~of~~ ON
⇒ discharging of capacitor.

* Clk = 0, Vin = 1.
P-mos - ON, n-mos - OFF
n-mos N/w - ON
⇒ Charging of capacitor

* Clk = 1, Vin = 0.
- ~~P~~ mos ON, n-mos N/w - OFF
P-mos OFF
→ o/p remains same

NOTE:

* whenever Clk = 0, Precharge capacitor charge to max irrespective of i/p.
* Clk = 1 - Evaluation.



* ~~when~~
* If Evaluation comes before the precharge, circuit doesn't work properly. or proper output doesn't obtained.

For Vin = 0, → Vout = 1
Vin = 1 → Vout = 1.

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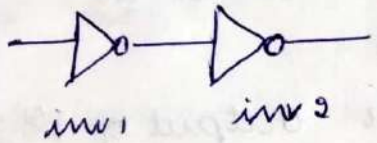
Dis Advantages: of Dynamic CMOS logic:

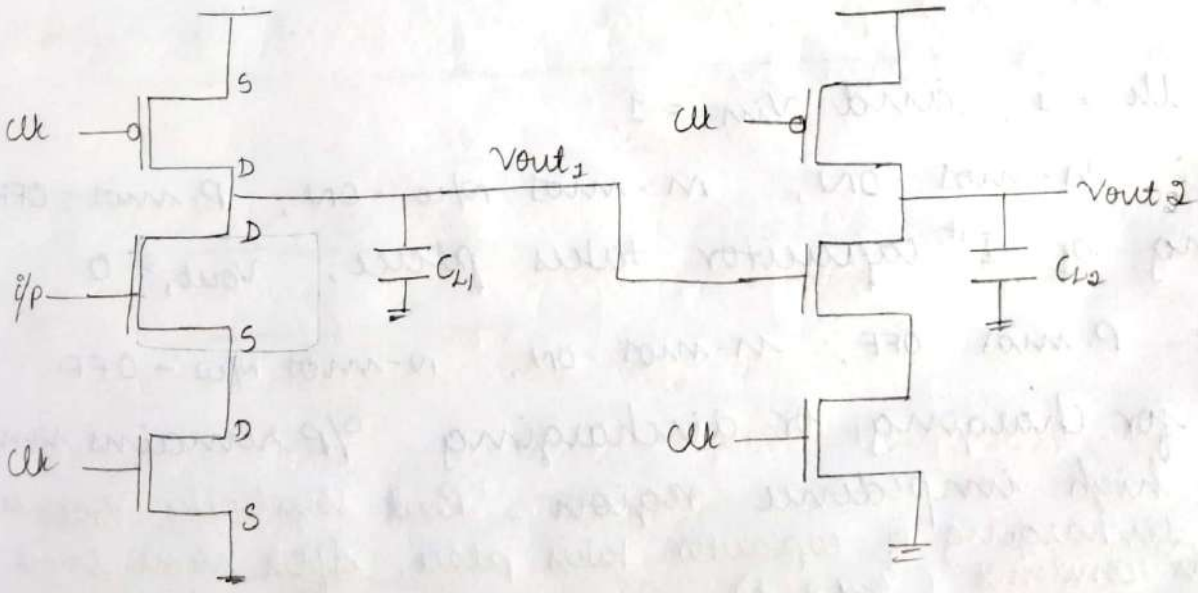
* Before doing Evaluation, need to perform precharge.
* High impedance.
* Cascading issue.

Advantages:

* No. of transistor is reduced.
* Output voltage swing is better.

Cascading issue:





* Irrespective of no. of stages, all the transistor will have same clk.

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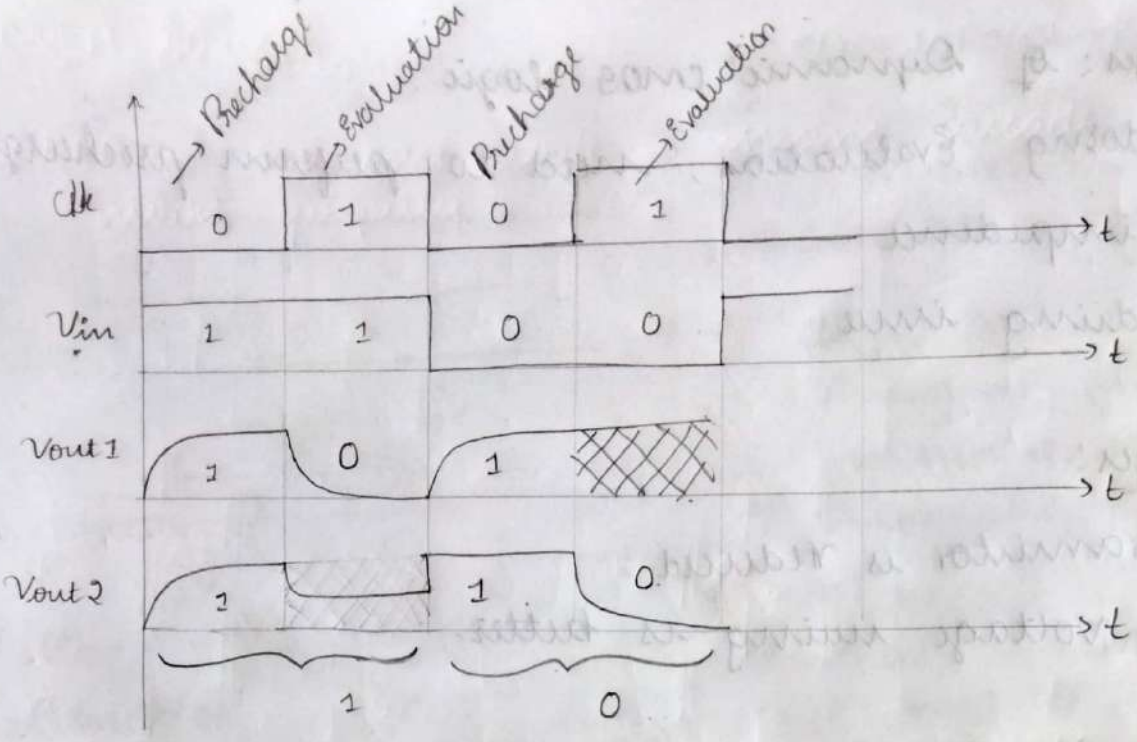

* when clk = 0, and $V_{in} = 1$.

Pull up transistors and 1st n-mos n/w becomes ON.
C_{L1} charged to maximum ($V_{out_1} = 1$)
2nd n-mos n/w becomes ON (because output of 1st inverter is the i/p to the 2nd inverter)
C_{L2} charge to maximum.

* when clk = 1, and $V_{in} = 1$.

1st stage: n-mos - ON, n-mos n/w - ON, P-mos - OFF.
discharging of 1st capacitor takes place, $V_{out_1} = 0$

2nd stage: P-mos - OFF, n-mos - ON, n-mos n/w - OFF
no path for charging or discharging. o/p remains same
~~* becomes high impedance region~~. But initially V_{out_2} is still high ∴ discharging of capacitor takes place. After some time o/p remains constant ($V_{out_2} = 1$)

* when clk = 0, $V_{in} = 0$.

1st stage: Pull-up transistor ON, n-mos & n-mos n/w - OFF, → charging of C_{L1} - $V_{out_1} = 1$.

2nd stage: Pull-up transistor ON, n-mos OFF, n-mos n/w ON
charging of C_{L2}, $V_{out_2} = 1$

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* when clk = 1, and $V_{in} = 0$

<u>1st stage</u>: Pull down transistor ON, pull up transistor and n-mos N/w OFF.

no path for charging or discharging. o/p remains same

$V_{out1} = 1$ (high impedance region)

<u>2nd stage</u>: Pull down transistor - ON, n-mos N/w ON

Pull up transistor OFF. → discharging of capacitor.

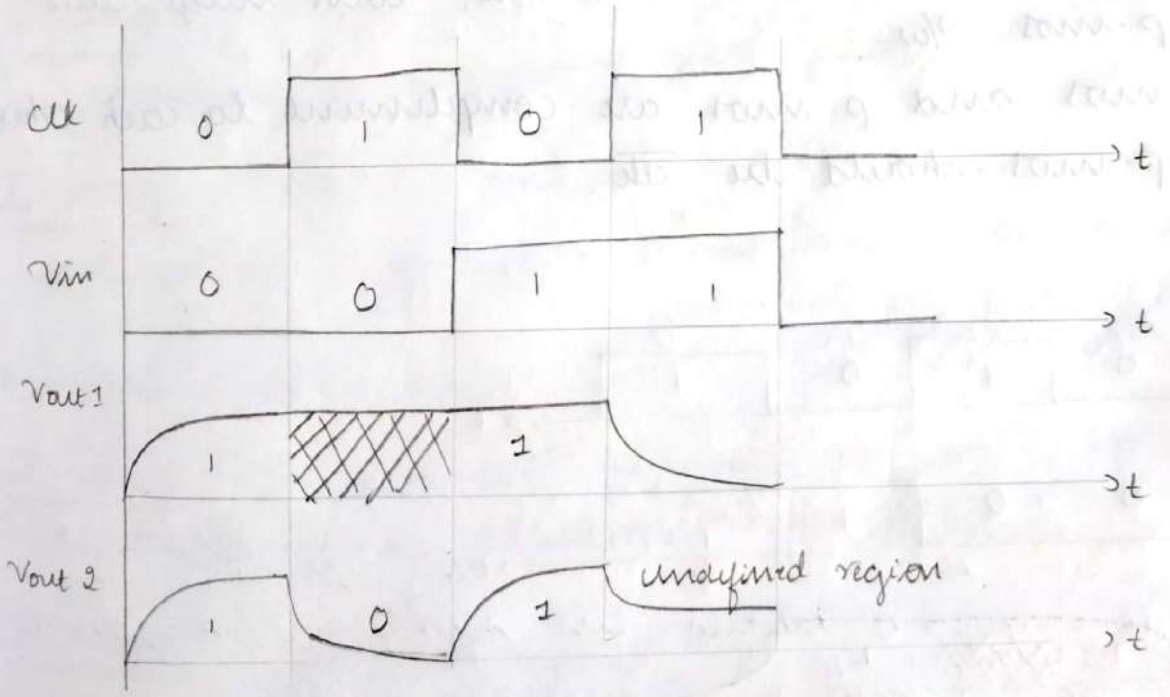
$V_{out2} = 0$

At the end of every clock pulse,

for $V_{in} = 1$, $V_{out1} = 0$, $V_{in} = 0$, $V_{out1} = 1$ (1st stage)

for $V_{out1} = 0$, $V_{out2} = 1$, $V_{out1} = 1$, $V_{out2} = 0$. (2nd stage)

<u>25/05/22</u>



* when clk = V_{in} = 0, $V_{out1} = 1$, and $V_{out2} = 1$
* clk = 1, $V_{in} = 0$. V_{out1} = High impedance region. $V_{out2} = 0$.
* clk = 0, $V_{in} = 1$, $V_{out1} = V_{out2} = 1$
* clk = V_{in} = 1, $V_{out1} = 0$. Initially V_{out1} is still high. discharging of C_{L2} takes place. Then o/p remains same ($V_{out2} = 1$)

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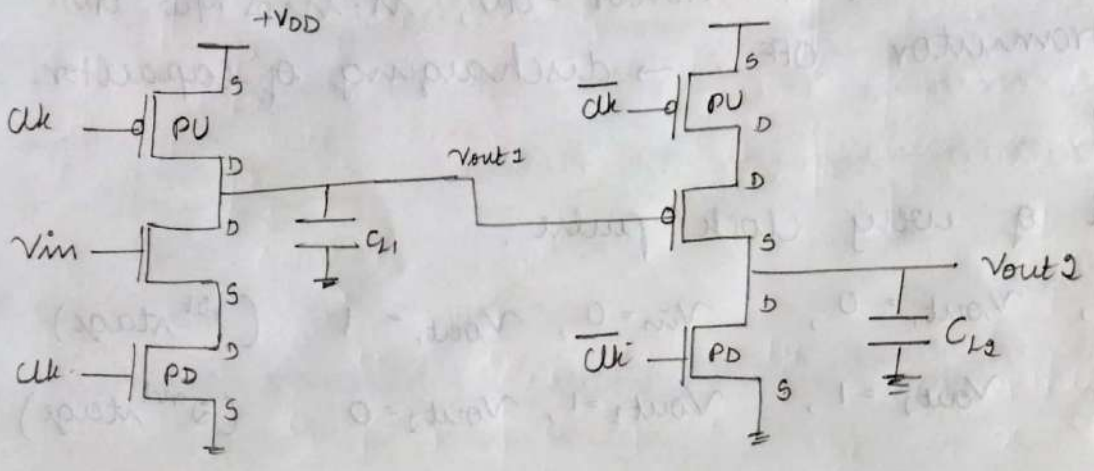
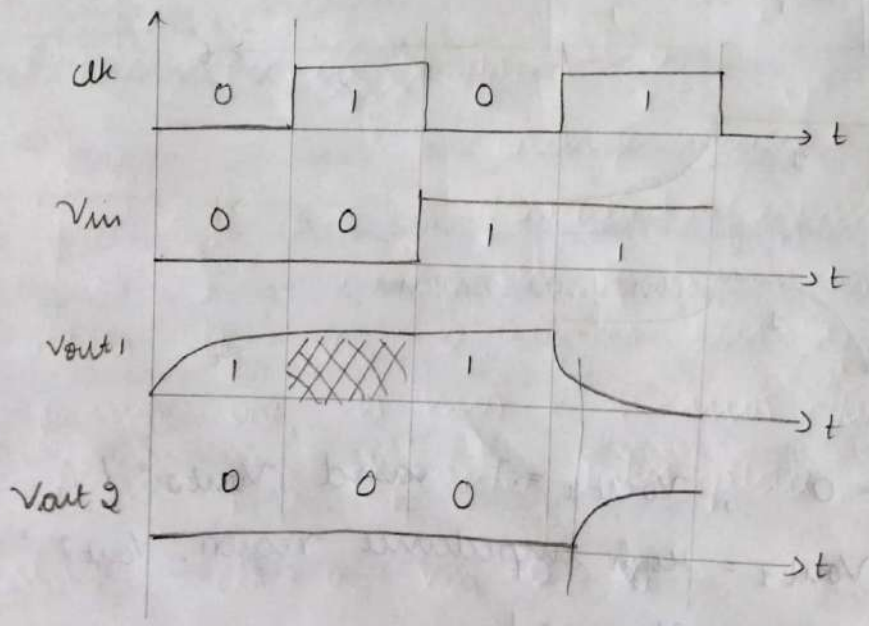
NORA logic:

NORA → no race logic → means cascade circuit works properly.



* Odd stages will have n-mos n/w, even stage will have p-mos n/w
* Since n-mos and p-mos are compliment to each other gate of p-mos should be $\overline{clk}$.



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* when $clk = 0$ and $V_{in} = 0$.

I - p-mos ON, n-mos and n-mos N/w OFF
charging of capacitor takes place ($V_{out_1} = 1$)

II stage: $\overline{clk} = 1$, $V_{out_1} = 1$.
n-mos ON, p-mos N/w - ON, p-mos = OFF
discharging of capacitor ($V_{out_2} = 0$)

* when $clk = 1$, $V_{in} = 0$.

I stage: n-mos ON, p-mos & n-mos N/w = OFF
no path for charging or discharging. o/p remains same.

I stage: $\overline{clk} = 0$, $V_{out_1} = 1$
p-mos ON, p-mos N/w = OFF n-mos OFF ⇒ o/p remains same.

* when $clk = 0$, $V_{in} = 1$.

I stage: p-mos ON, n-mos N/w ON, n-mos OFF
charging of capacitor takes place

II stage: $\overline{clk} = 1$, $V_{out_1} = 1$
n-mos ON, p-mos & p-mos N/w = OFF ⇒ discharging of C_{L2}

* when $clk = 1$, $V_{in} = 1$

I stage: n-mos ON, n-mos N/w - ON, p-mos - OFF
discharging of capacitor takes place.

II stage: $\overline{clk} = 0$, $V_{out_1} = 0$.
n-mos OFF, p-mos & p-mos N/w - ON.
Charging of C_{L2} takes place. [but initially V_{out_1} is still high, p-mos ON, p-mos N/w - OFF, n-mos OFF.
o/p remains same ($V_{out_2} = 0$)]
After some time, p-mos N/w becomes ON and charging of capacitor happens

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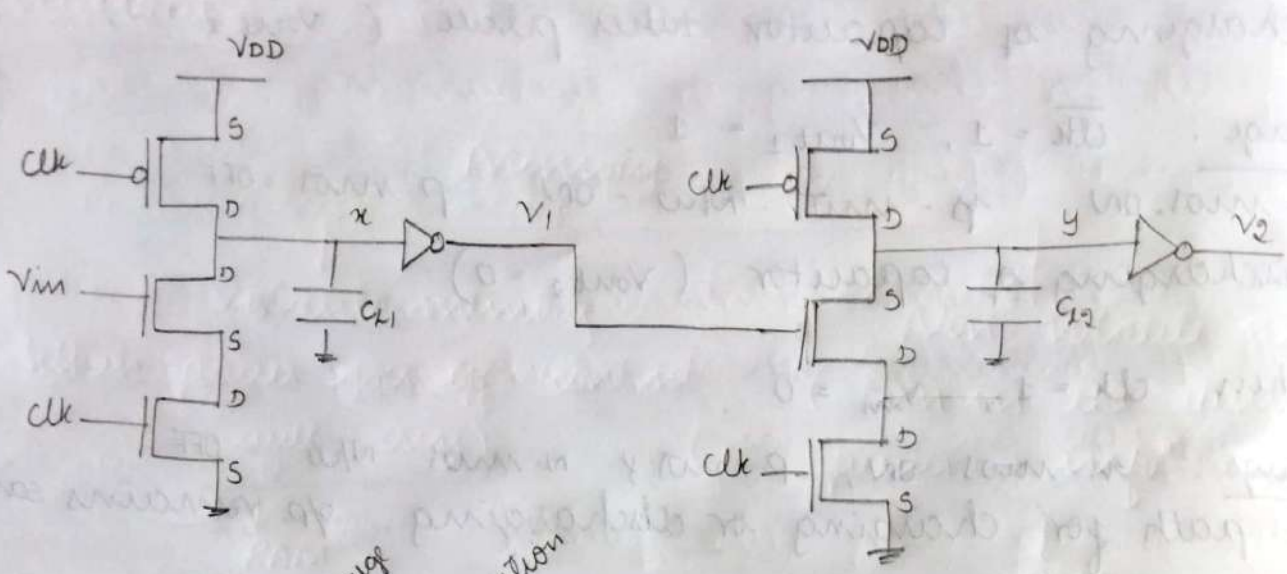
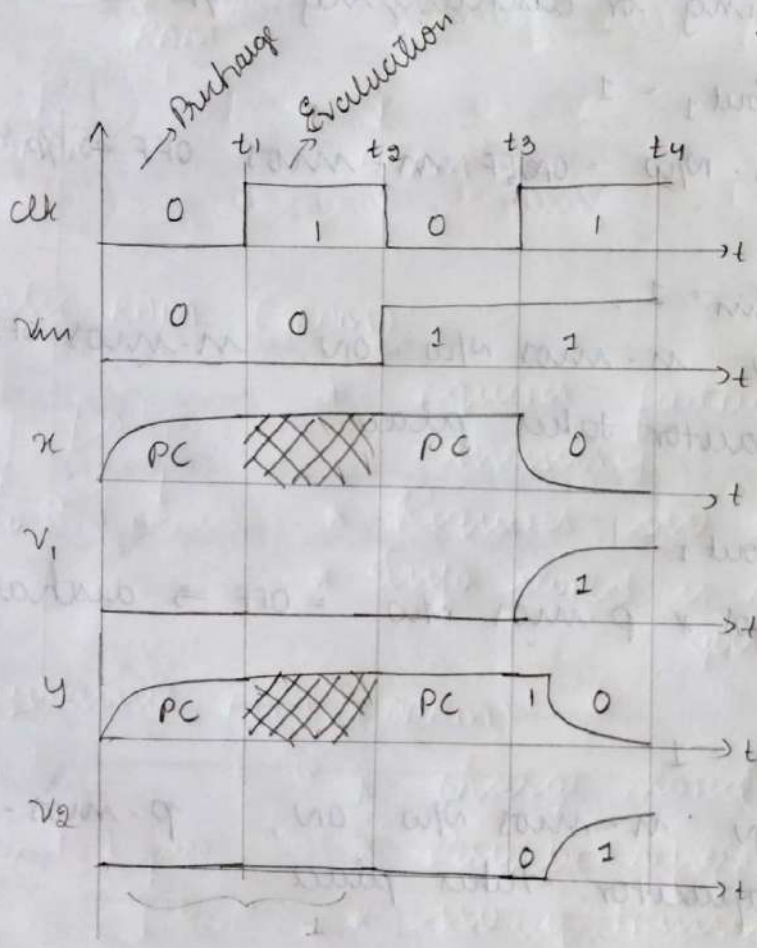
II. Introducing inverter in b/w the stages.





where
x = 1st stage o/p
V_{in} = 1st stage i/p
V_1 = 2nd stage i/p
V_2 = 2nd stage o/p

PC - pre-charge

* when $Clk = V_{in} = 0$.

<u>1st</u>: p-mos - ON, n-mos & n-mos N/w - OFF
charging of capacitor takes place. $x = 1$, $V_1 = 0$.

<u>2nd stage</u>: $Clk = 0$, $V_{in} = 0 = V_1$
p-mos ON, n-mos & n-mos N/w = OFF
charging of C_{L1} ⇒ $y = 1$ & $V_2 = 0$

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* when $clk = 1$, $V_{in} = 0$.

1st stage: n-mos ON, p-mos & n-mos N/w = OFF

no path for charging or discharging, o/p remains same

becomes high impedance region. $x = 1$, $V_1 = 0$.

2nd stage: $clk = 1$, $V_{in} = V_1 = 0$. ⇒ o/p remains same.

$y = 1$, $V_2 = 0$.

* when $clk = 0$, and $V_{in} = 1$.

1st stage: p-mos and n-mos N/w = ON, n-mos OFF

charging of C_{L1} ⇒ $x = 1$. and $V_1 = 0$.

2nd stage: $clk = 0$, and $V_1 = 0$ ⇒ $y = 1$ and $V_2 = 0$

* when $clk = 1 = V_{in}$

1st stage: n-mos & n-mos N/w ON, p-mos OFF

discharging of C_{L1} takes place ⇒ $x = 0$, $V_1 = 1$

2nd stage: $clk = 1$, $V_1 = 1$, n-mos - ON, p-mos - OFF

Initially $V_1 = 0$, ⇒ n-mos N/w - OFF

no path for charging or discharging. o/p remains same. ($y = 1$)

after some time $V_1 = 1$, ⇒ n-mos N/w ON.

discharging of capacitor takes place → $y = 0$.

similarly, initially $y = 1$ ⇒ $V_2 = 0$

after some time $y = 0$ ⇒ $V_2 = 1$.

NOTE:

* In this method, no. of transistors required is more

⇒ power dissipation

Therefore NORA method is best.

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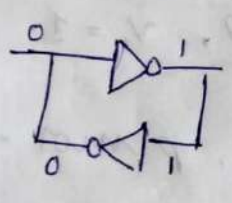
26/05/22

Memory:

Memory

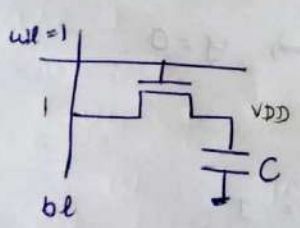
- Volatile memory (When power goes off - content will erise)
  - RAM
    - SRAM
    - DRAM
- Non-volatile memory (Even in the absence of power. → info^n retain)
  - ROM
    - EPROM
    - EEPROM

* Static RAM (SRAM):



* requires fedback to maintain the memory
* Requires no refreshment
* Info stored is not lost until power goes off.

* Dynamic RAM (DRAM):



* charge stored
* Periodic refreshment is required.
* no. of transistor less. ∴ ~~requ~~ Occupies less space than SRAM.

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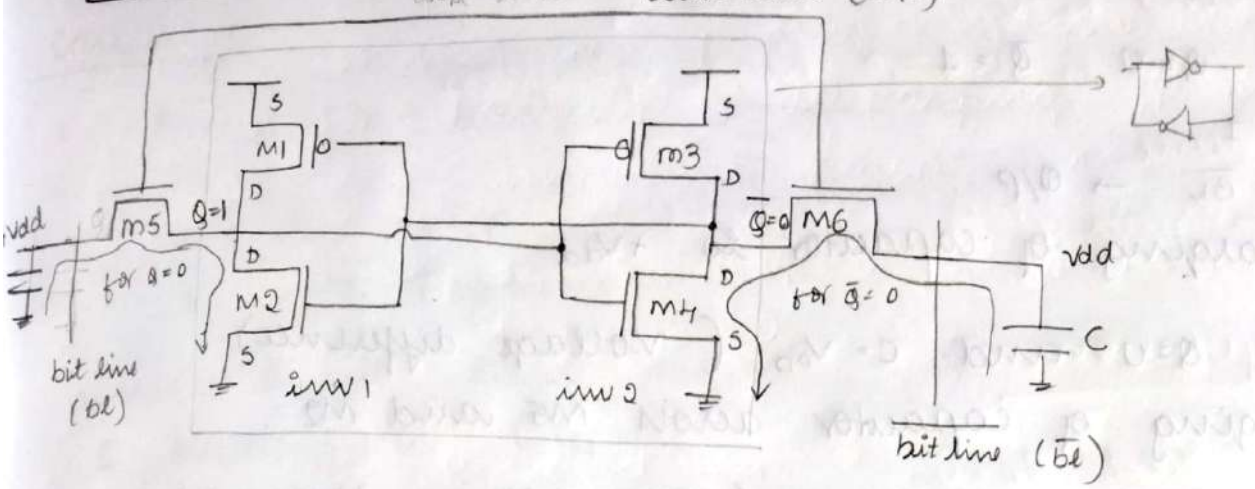
SRAM : 6T SRAM

6T → T = transistor



1. If WL = 1 → (Read / write) R/W
   WL = 0 → Hold.

2. Bit line and $\overline{\text{Bit line}}$ (BL & $\bar{BL}$) ⇒ i/p (write) when writing into memory
   o/p (read)

where M5 and M6 are pass transistors

Read operation : case 1 :

1. M : Q = 1
   $\bar{Q}$ = 0.
2. WL = 1 (Read)
3. BL & $\bar{BL}$ = o/p.
4. we need to precharge the capacitor to +Vdd

At M5 : since there is no volt. difference, ⇒ no. path to discharge → V_{DD} retain.

5. At M6 : $\bar{Q}$ = 0, c = Vdd (Potential / voltage difference)
   discharging of capacitor takes place across M6 & M4
   Now c = 0,
   BL = 1 → we are accessing Q = 1
   $\bar{BL}$ = 0 → we are accessing $\bar{Q}$ = 0.

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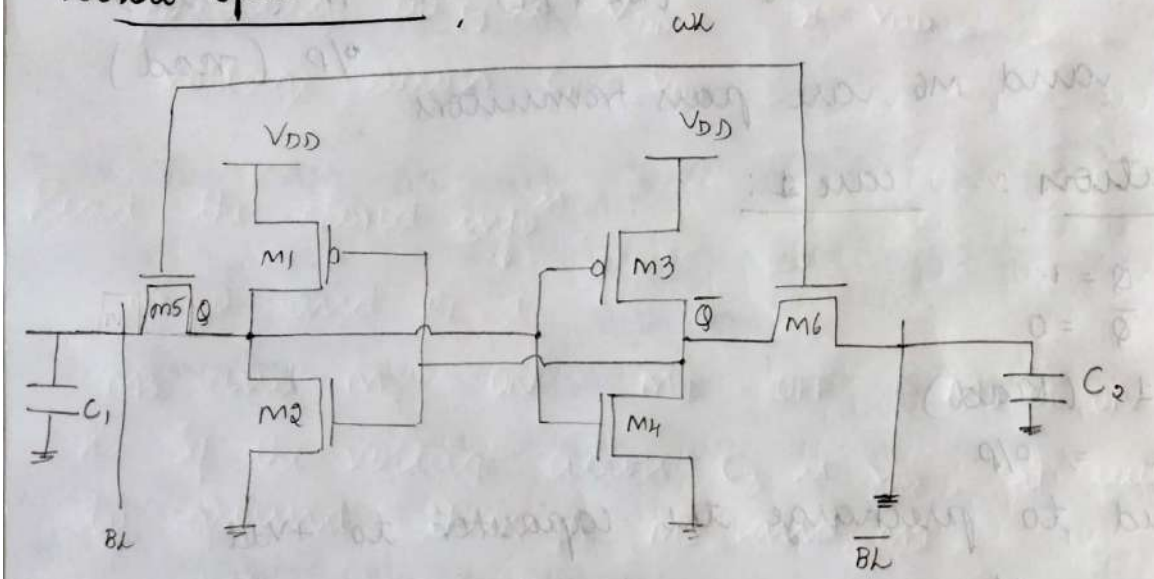
Case 2

1. M : $Q = 0$, $\bar{Q} = 1$
2. $WL = 1$
3. BL & $\overline{BL}$ → O/P.
4. Precharging of capacitor to $+V_{dd}$.

At M5 : $Q = 0$ and $C = V_{DD}$ (voltage difference) discharging of capacitor across M5 and M2.

At M6 : $\bar{Q} = 1$, and $C = V_{DD}$ (no. voltage difference) V_{DD} retain.

Write operation :



Case 1 : 1. $Q = 0$, $\bar{Q} = 1$

2. $WL = 1$, 3] BL & $\overline{BL}$ → i/p

4. $\overline{BL}$ = GND, → offers least resistance path. C_2 never charges $\bar{Q}$ becomes '0'

~~since~~ $\bar{Q} = 0$, inv 1 i/p = 0 ⇒ $Q = 1$.

5. Charge the capacitor to max. ($Q = 1$) ⇒ $BL = 1$.

we wrote '1' to memory

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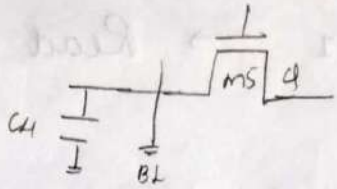
Case 2:



1. M : $Q = 1$, $\bar{Q} = 0$
2. $WL = 1$
3. BL & $\overline{BL}$ → i/p.
4. BL = '0' (ground)

since $BL = 0$, least resistance path will establishes & Q becomes '0' ($C_1 = 0$)

$Q = 0$ → i/p of inv 2 = 0 ⇒ $\bar{Q} = 1$.

C_2 charges upto V_{DD}

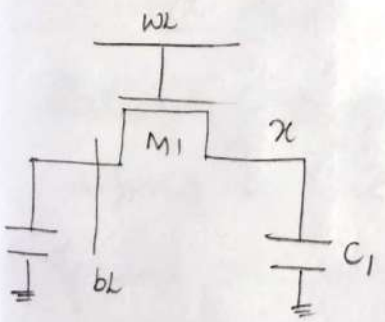
$\overline{BL} = 1$.

01/06/22

Dynamic RAM (DRAM)

DRAM < 1T DRAM (One transistor Dynamic RAM)
3T DRAM.

1TDRAM



M_1 acts as pass transistor.

write operation

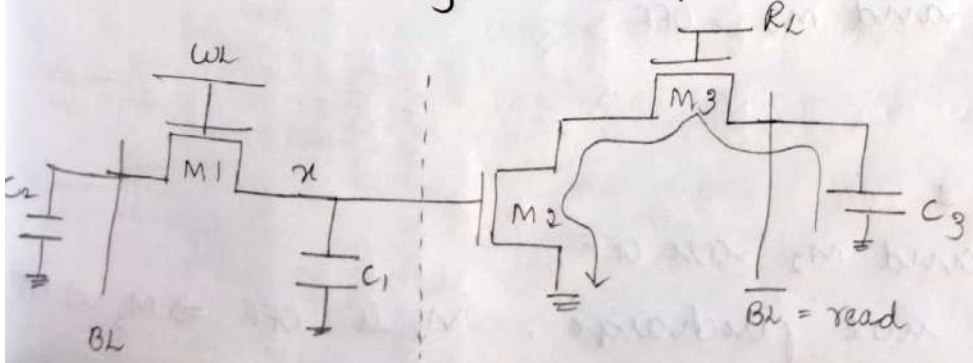
1. $WL = 1$, $BL = 1$ ⇒ $x = V_{dd}$

C_1 charges to max.

2. $WL = 0$, $BL = 0$ (i/p)

for read operation, BL = o/p.

3T DRAM using 1TDRAM:



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$WL = 1$ and $RL = 0$ → write operation
$WL = 0$ and $RL = 1$ → Read operation

BL → write
$\overline{BL}$ → read.

Write operation:

$WL = 1$ and $RL = 0$.
M_1 - ON, M_3 and M_2 = OFF.

* If write = 1.
  precharge the C_2 to V_{DD} $x = V_{DD}$
  voltage across $C_1 = V_{DD}$

Read the stored info^n:

$WL = 0$ and $RL = 1$.

$M3$ and M_2 - ON M_1 = OFF (M_2 is ON because $x = V_{DD}$)
x = If the voltage across C_3 is V_{DD}, it will discharge to ground through $M3$ and $M2$.
Now voltage at $C_3 = 0$.
$\overline{BL} = 0$, $BL = 1$.
↓
Read = '0'.

* If write = 0.
  $WL = 1$, and $RL = 0$.
  $M1$ = ON, $M2$ and $M3$ = OFF

bl = 0/gnd, $x = 0$

$WL = 0$, $RL = 1$.
M_3 = ON, M_1 and M_2 are OFF.

if the capacitor is not precharge, M_2 is OFF ⇒ M_3 is OFF

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∴ no connection b/w source and drain terminals of M3.

∴ $\overline{BL} = 0$ (x is also '0')

This is not correct.

∴ capacitor should charge to $+V_{DD}$ ($\Rightarrow M_2 = ON$)

hence $\overline{BL} = 1$ and $BL = 0$.

Power reduction methods:

1. $P_{dynamic} = P_{switching} = \alpha C_L V_{dd}^2 f$

In order to reduce the power.

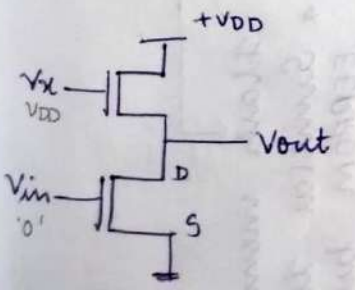
* Reduce the 'α' by sending s/m into sleep. (sleep → processes will reduces)
* Decrease / reducing the switching frequency (Trade off delay increases)
* Reducing V_{DD} (By using appropriate supply voltage make circuit to work properly).

2. $P_{short\ circuit}$:

Ratioed Transistors:

sizing or scaling. ($\omega \propto C$, $\omega \frac{1}{\propto} R$)

If we reduce the size of Transistor / Resistor, power dissipation will reduces)



$V_x = V_{DD}$, $V_{in} = 0 \Rightarrow V_{out} = V_{DD} - V_{th}$,

Effect of ↓ the o/p:

If the Vout driving the next stage, there will be a noise margin.

∴ swing from 0 to V_{DD} or V_{DD} to 0 should be proper.

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Voltage boost mapping : Avoids any o/p drop at the o

09/06/22

ROM : Read only memory.

ROM

- PROM
  - * Programable ROM
  - * One time writing rest all time reading
- EPROM
  - * Erasable, programmable ROM
  - * Program can be done many time
  - * Bulk erasing can be possible
  - * Erasing done by word by word
- EEPROM
  - * Electrically EPROM
  - * More no. of erasing & programming can be possible than EPROM.
  - * Erasing → Bit by bit
- Flash memory
  - * Similar to EEPROM but erasing will done by word to word

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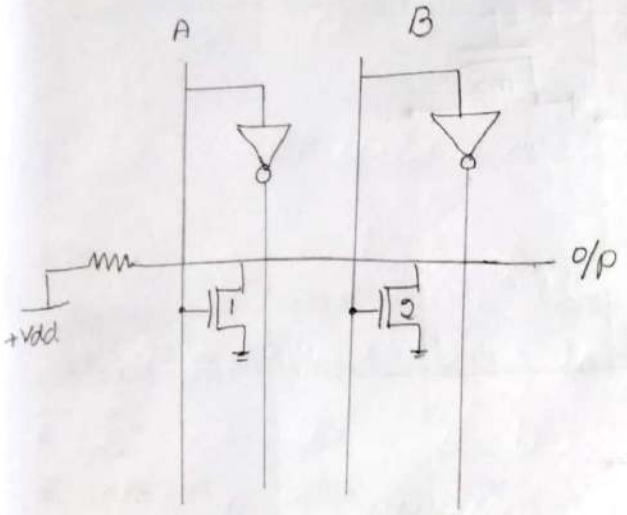
PROM :

PLD (Programmable logic device) →
- PLA - Programmable logic Arrays
- PAL - P. Array logic
- PROM

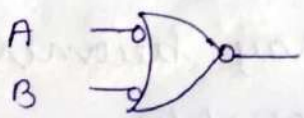


* R - current connecting resistor.
* MOSFET can be connected to any of the i/p (Either for compliment or uncompliment)
* when $A = B = 0$
  both the transistor OFF
  $o/p = 1$.
  (no path & establish b/w $+V_{DD}$ & ground)

* when $A = 0$, $B = 1$.
  M_1 = OFF, M_2 = ON, path establish b/w V_{DD} & gnd
  $o/p = 0$.
* when $A = 1$, $B = 0$, M_1 = ON, M_2 = OFF, ⟹ $o/p = 0$.
* when $A = B = 1$, $M_1 = M_2$ = ON ⟹ $o/p = 0$.

A	B	o/p
0	0	1
1	0	0
0	1	0
1	1	0

⟶ NOR logic.
To convert NOR logic to AND give the compliment i/p.



$\overline{\bar{A} + \bar{B}} = \bar{\bar{A}} . \bar{\bar{B}} = A . B$

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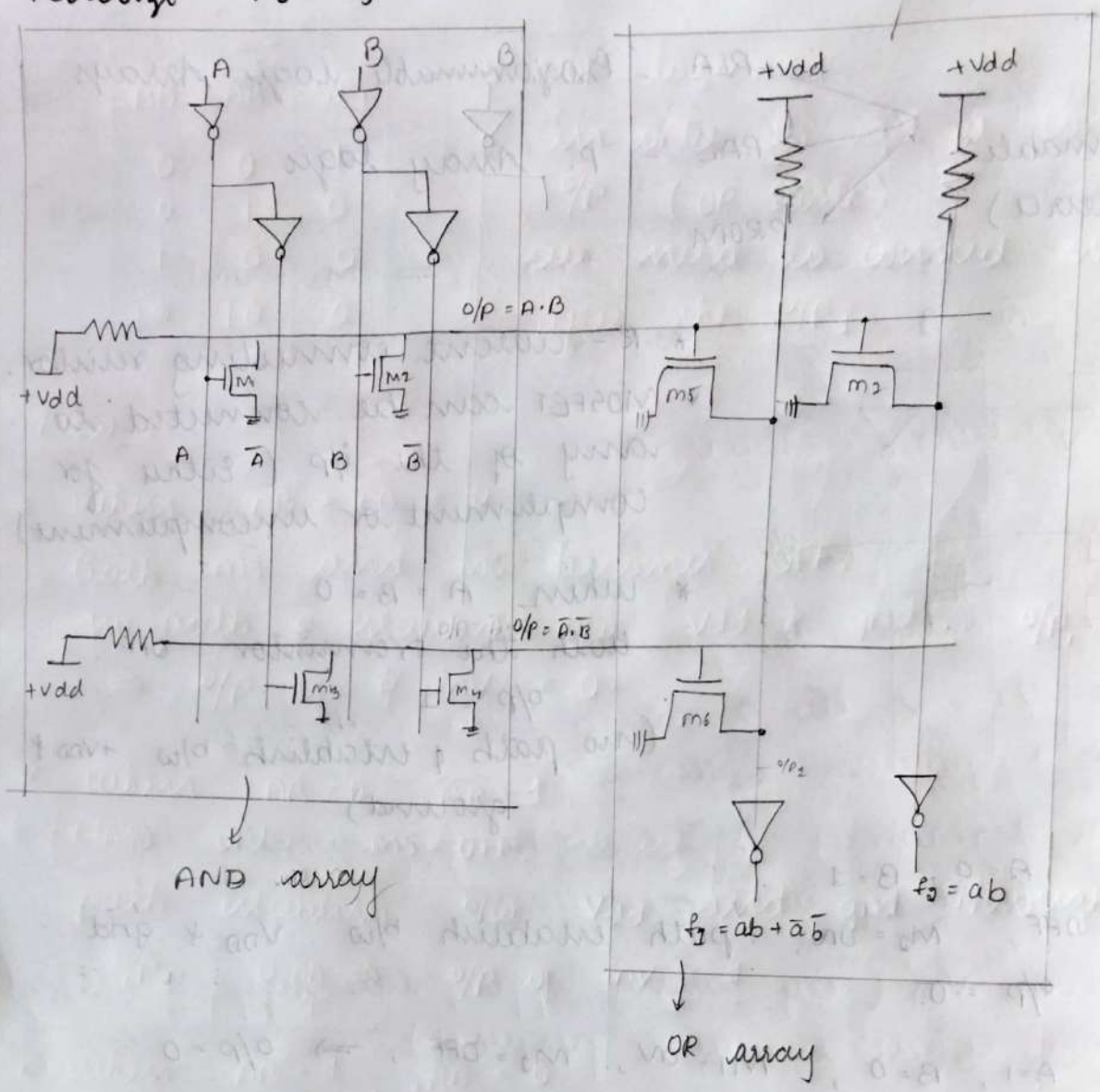
Realize $f(a,b) = ab + \bar{a}\bar{b}$



For AND array

columns → i/p variables

rows → o/p. (AB & $\bar{A}\cdot\bar{B}$)

For OR array :

o/p of AND array becomes i/p.

rows → i/p variables

columns → o/p.

If we consider transistor M_1 and M_2 → o/p = A.B

for M_3 and M_4 → o/p = $\bar{A}\cdot\bar{B}$.

* ~~Since f1 and f2~~

AB	$\overline{\overline{A}\,\overline{B}}$	o/p$_1$
0	0	1
0	1	0
1	0	0
1	1	0

→ NOR logic.

In order to get a compliment o/p (OR logic).

we need to connect inverter after the o/p$_1$.

Now.

* when $AB = \overline{\overline{A}\,\overline{B}} = 0$,

Both M5 and M6 becomes OFF.

no path is establish b/w Vdd & gnd ∴ o/p$_1$ = 1 = Vdd

⇒ o/p of inv = 0.

* when $AB = 0$, $\overline{\overline{A}\,\overline{B}} = 1$.

M6 = ON, M5 = OFF,

path establish b/w Vdd and gnd through M6

∴ o/p$_1$ = 0 = AB ⇒ o/p of inv = 1

* when $AB = 1$, $\overline{\overline{A}\,\overline{B}} = 0$.

M5 = ON, M6 = OFF.

Path establish b/w Vdd and gnd through M5

o/p$_1$ = 0 ⇒ o/p of inv = 1.

* when $AB = \overline{\overline{A}\,\overline{B}} = 1$.

Both M5 = M6 = ON. ⇒ o/p$_1$ = 0 ⇒ inv o/p = 1

AB	$\overline{\overline{A}\,\overline{B}}$	o/p
0	0	0
0	1	1
1	0	1
1	1	1

→ OR logic.

SOP → AND followed by OR logic

POS → OR followed by AND.

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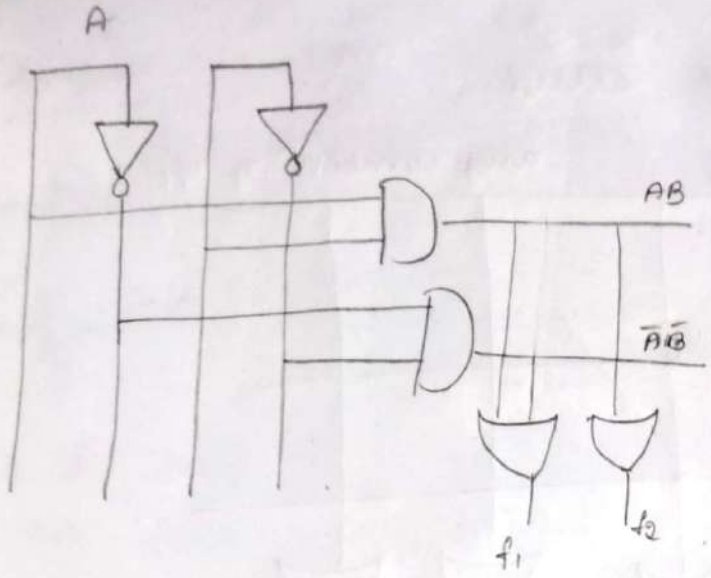
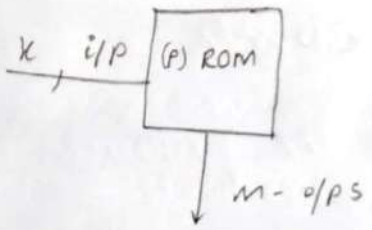


$f_1 = ab + \bar{a}\bar{b}$

$f_2 = ab$

* PLA → Both AND array and OR array are programmable
* PAL → Only AND array programmable, OR - fixed
  means we can change the info^n inside the AND array.
* PROM → AND array - fixed
  OR array - Programmable.
  we can increase or decrease no. of product terms.



size of ROM is $2^k \times n$

k = address line

n = word length.

AND array is a kind of decoder — for n i/ps we get 2^n o/p.

i.e. $n : 2^n$ or $k : 2^k$.

* In PROM, ~~o/p~~
  all the o/p of AND ~~array~~ gates are applied as i/ps to each OR gate.
  ∴ o/p of PROM is in SOP form.

  x indicates - Programmable
  0 indicates - fixed.

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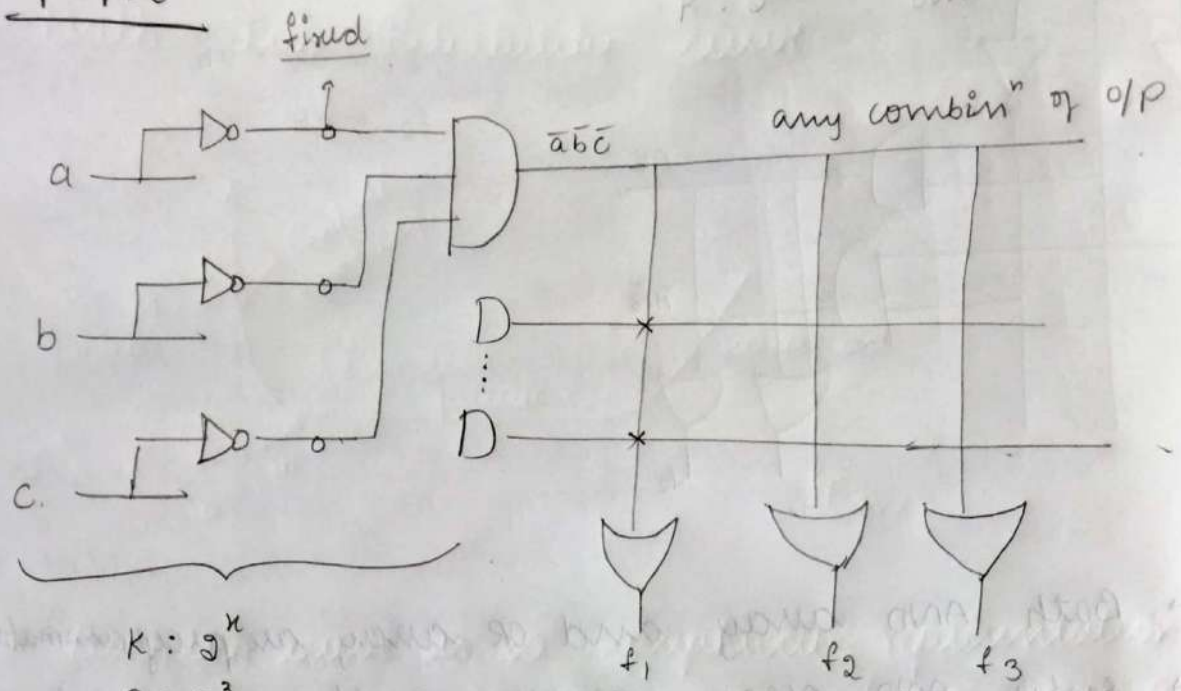
06/06/22



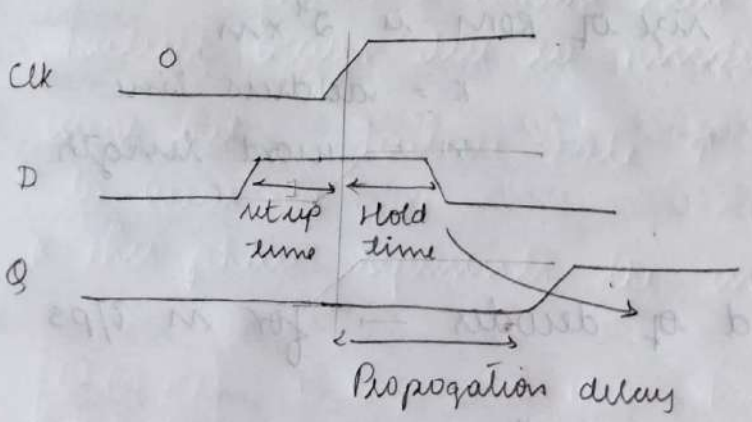
$K : 2^n$

$3 : 2^3$

3 : 8 decoder $\quad f_1 = \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + \dots + abc$

* $\boxed{\text{PROM} = \text{Decoder} + \text{OR array}}$

D - flip flop:



$Q \simeq D$

Setup time : Minimum time for which D is valid before the clock appears.

Hold time : Minimum time for which D is valid after the clock appears.

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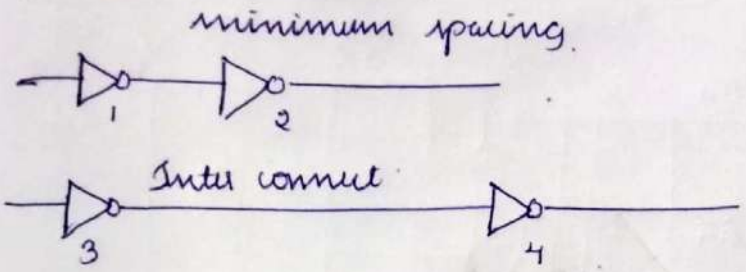
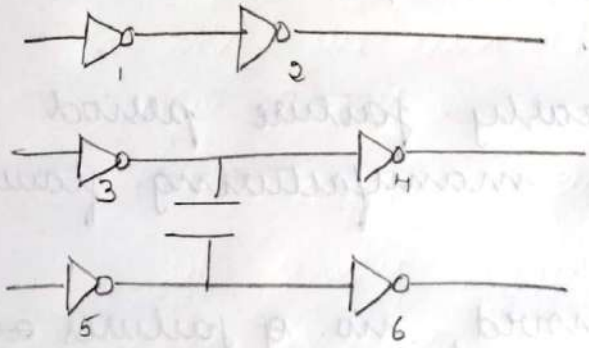
Design aspects:



As the wire connection ↑, RLC is also ↑
⇒ delay is also ↑

* If two interconnect are close to each other, capacitance comes into picture



* Longer the length of inter connect, power dissipation increases

Reliability, Testing:

* Reliability test → done before fabrication
  Tells about life span of a device.

* Testing → Done after fabrication.
  ~~the~~ Test, whether device is working properly or not.

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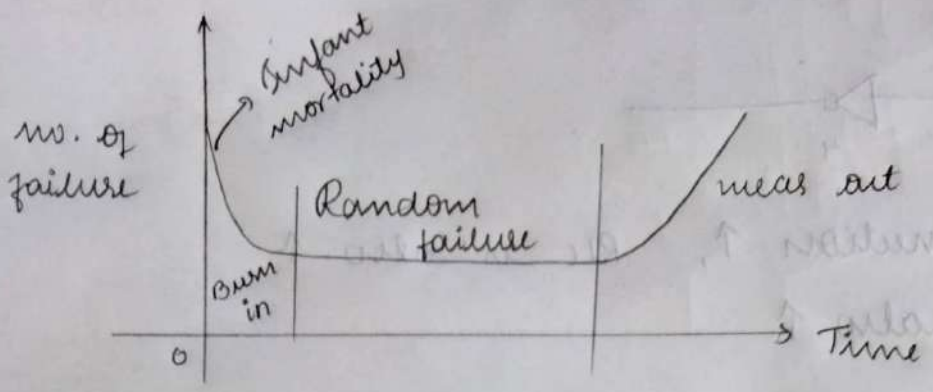
Bath - Tub Reliability curve.

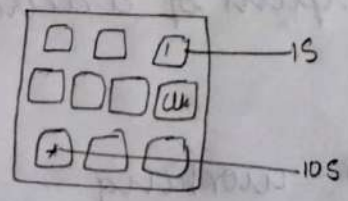


* Bathtub curve is a graphical representation of rate of failure of a product / device over a time.

* Infant mortality is an early failure period. Failure occurs because of manufacturing flaws, material defects etc.
  As the early failures removed, no. of failures ~~also~~ ↓

* Random failure: Failure rate is almost constant. Failure occurs due to random events.

* wear out: Failure rate ↑, as the products begin to wear out.
  * This phase represents the end of life cycle of product



Chip

10 - 1 = 9S Skew

Skew = 0

Skew → Difference b/w max time to min. time

* Simply a time delay.
* It should be minimum.

Circuit :

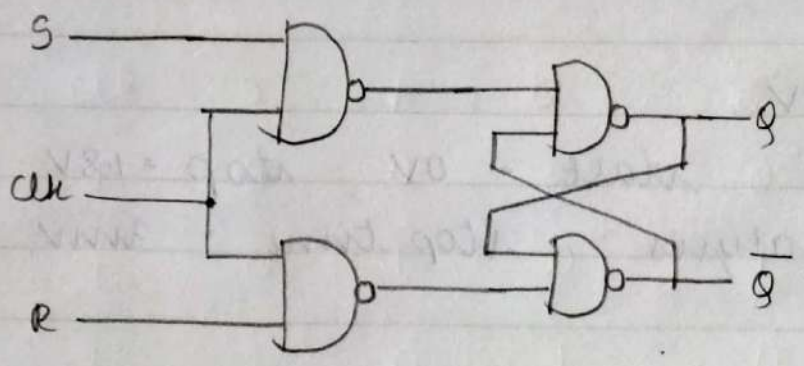


Figure 9.1 : Clocked SR latch based on NAND gate

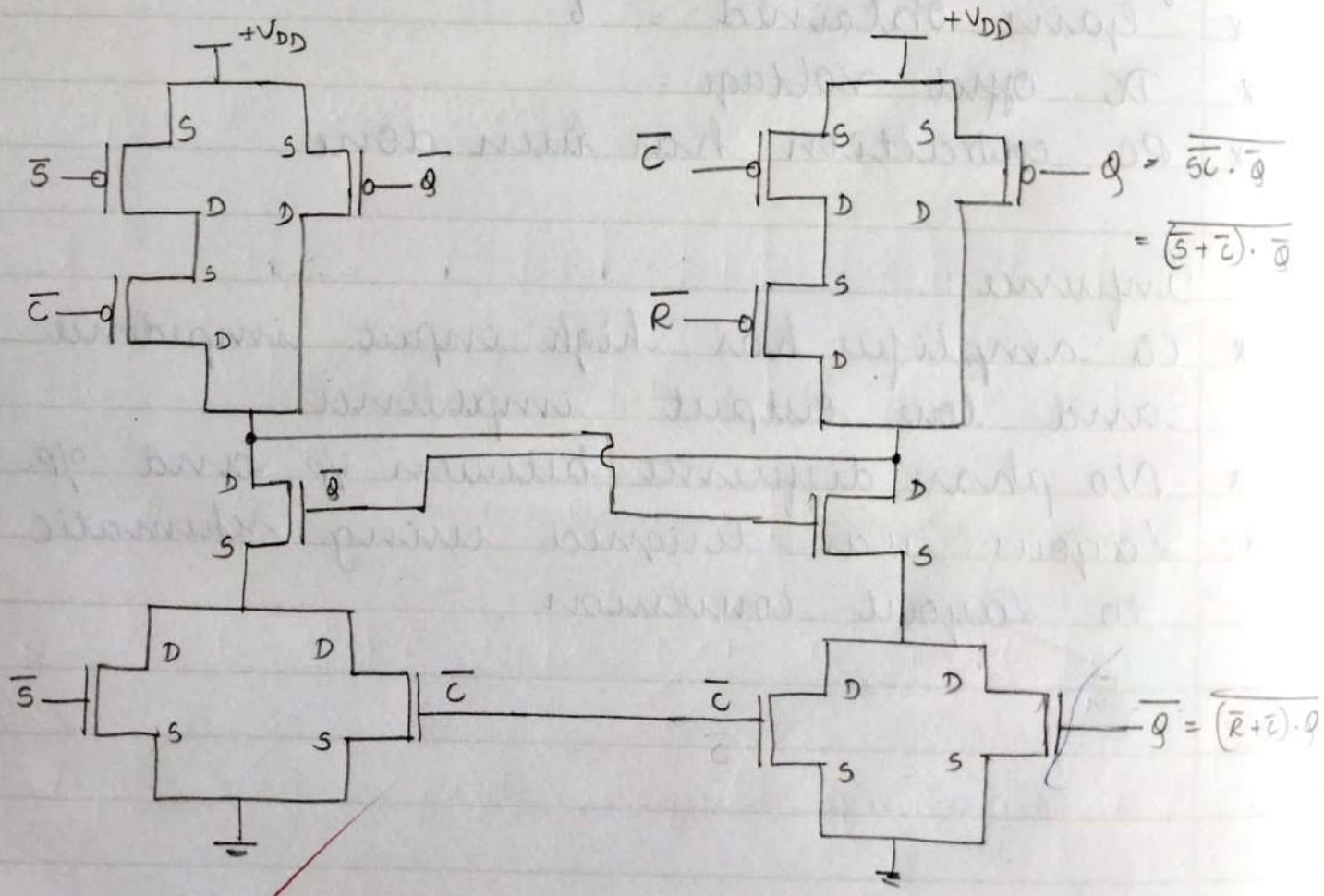


Figure 9.2 : Clocked SR latch using CMOS

Circuit :

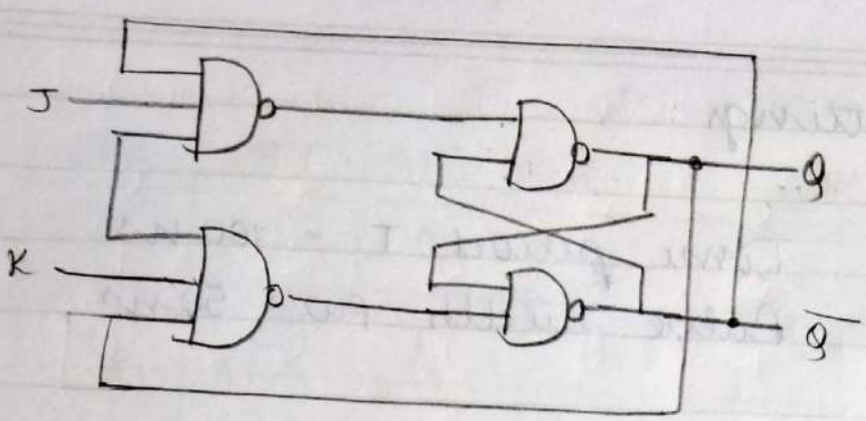
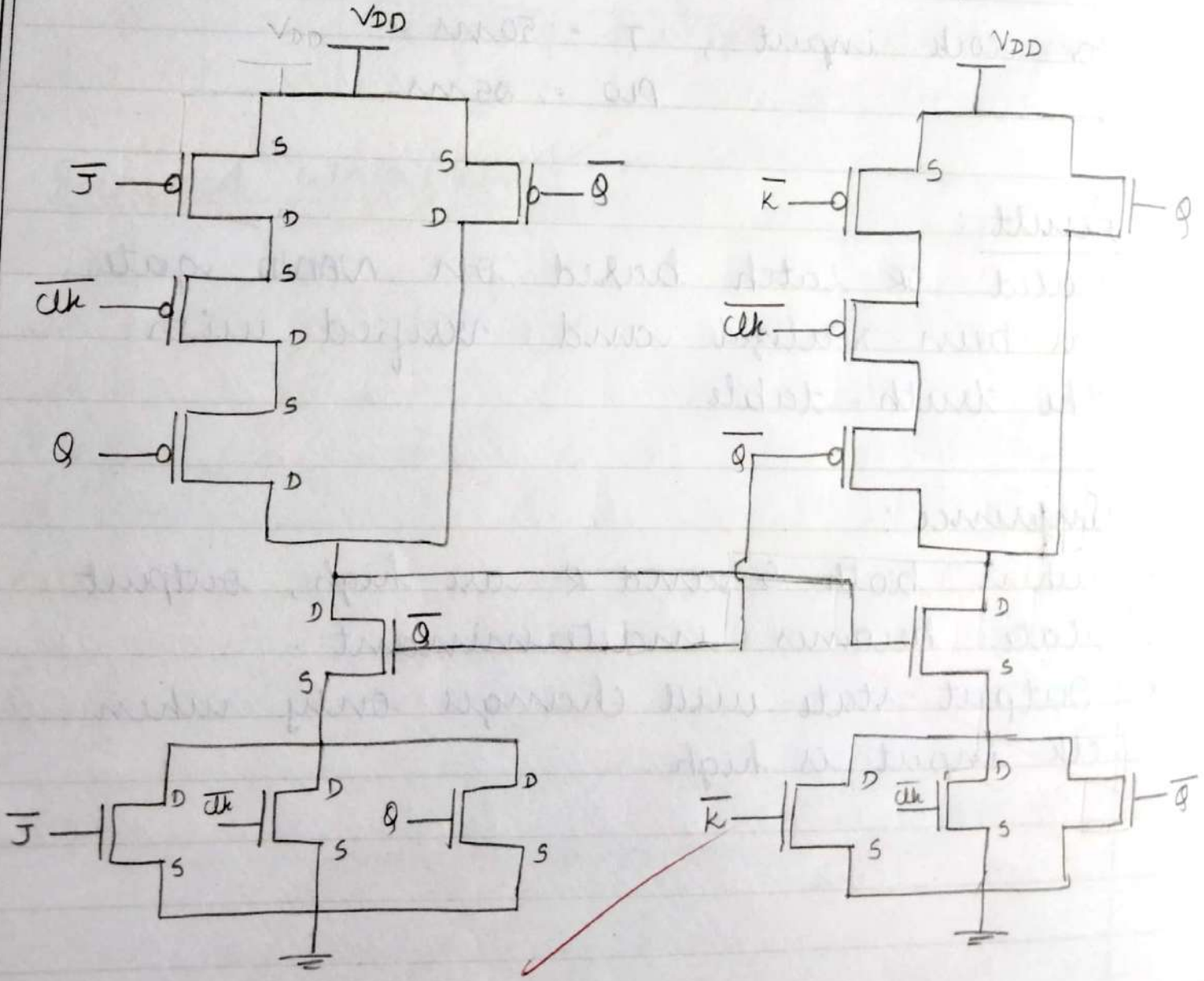


Figure 9.4 : Circuit diagram of JK flip flop



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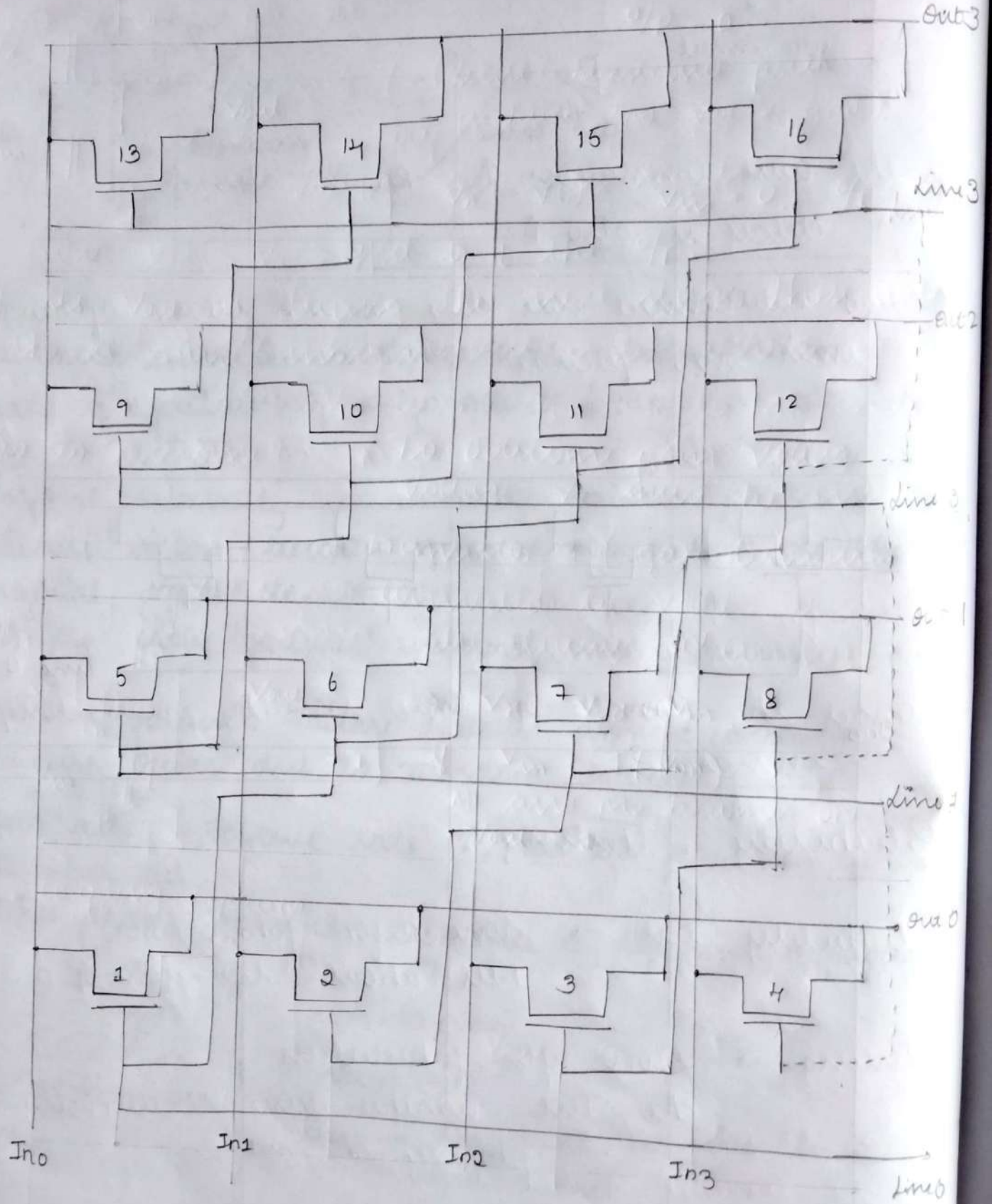
Barrel shifter :



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Transistor 1, 6, 11, 16 → driven by line 0
2, 7, 12, 13 → driven by line 3
4, 5, 10, 15 → line 1
3, 8, 9, 14 → line 2

i) when line 0 = enable
In0 → o/p at Out 0
Out 1 = In 1 , Out 2 = In 2 , Out 3 = In 3 , Out 0 = In 0

ii) when line 1 enable:
Out 0 = In 3, Out 1 = In 0 , Out 2 = In 1 , Out 3 = In 1.

iii) when line 2 enable:
Out 0 = In 2 , Out 1 = In 3 , Out 2 = In 0 , Out 3 = In 1

iv) when line 3 enable:
Out 0 = In 1 , Out 1 = In 2 , Out 3 = In 3 , Out 4 = In 0

∴ By enabling only one line, we can perform no of shifts at a time.

<u>Advantages over conventional shifter:</u>

* Delay reduced
* Any shift, at any time

Depending on transistor matrix.
For 4×4 matrix → 3 shift
8×8 matrix → 7 shift.

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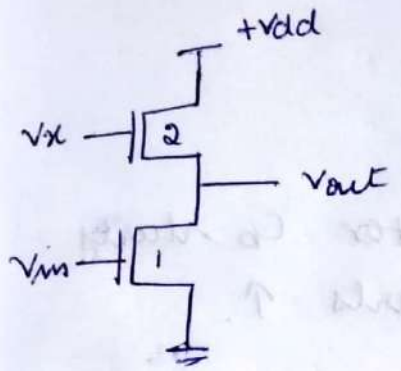
Voltage boot strapping:



i] when $V_x = V_{in} = 1$.
M1 and M_2 (ON)
Least resistance path establish b/w Vdd and ground
$V_{out} = 0$.

where M1 & M2 are pass transistors.

ii] when $V_x = V_{dd}$, $V_{in} = 0$.
$V_{out} = V_{dd} - V_{th}$.

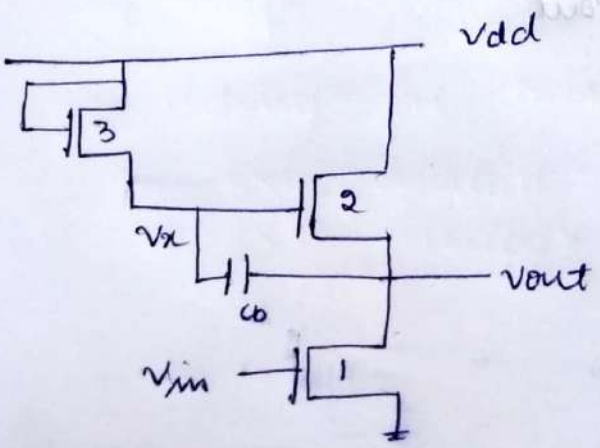
Effect of ↓ of the o/p:

If the Vout is driving the next stage, then there will be a noise margin.

How to overcome?

" Voltage bootstrapping is a technique to overcome the threshold voltage drops of the output voltage in the pass transistor and logic gates".

* To overcome the voltage drop, the voltage V_x must be increased. This can be achieved by adding a third transistor M3 into the circuit.



* The gate terminal of M3 is connected to Vdd, M3 is always ON.

$V_x = V_{dd} - V_{th}$.

If $V_{in} = 1$ (High)

$V_{out} = 0$. (Low)

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ii] $V_x = V_{dd} - V_{th}$.

$V_{in} = 0$.

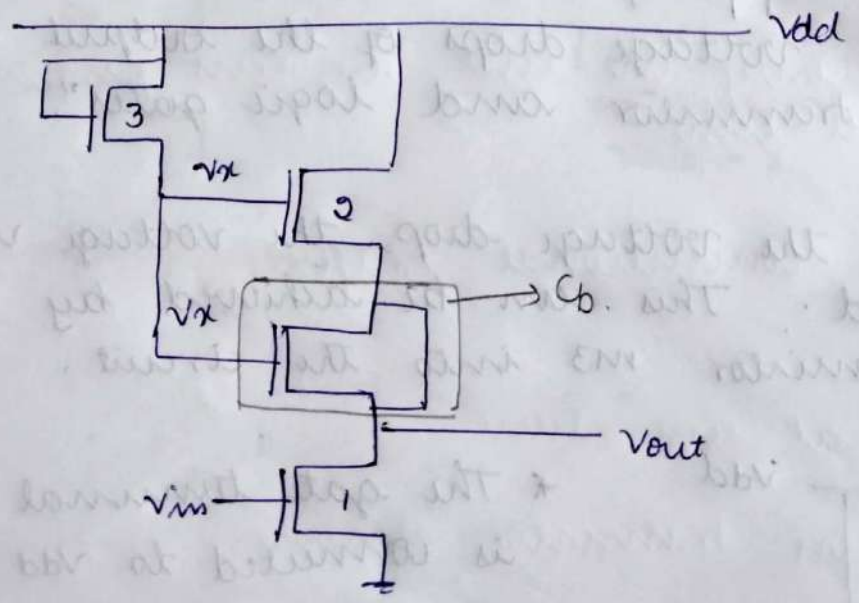
M2 is ON, M1 - OFF.

→ V_{out} starts charging (starts to rise)
at the same time, coupling capacitor C_b starts charging and voltage across V_x starts ↑.

Now $V_{dd} = V_x > V_{dd}$.

∴ The goal of the above circuit is to provide a high enough voltage V_x to let V_{out} go to V_{DD} instead of $V_{DD} - V_{th}$.

This coupling capacitor can be replaced by another n-mos pass transistor by shorting the drain & source terminal and gate terminal is connected to V_x



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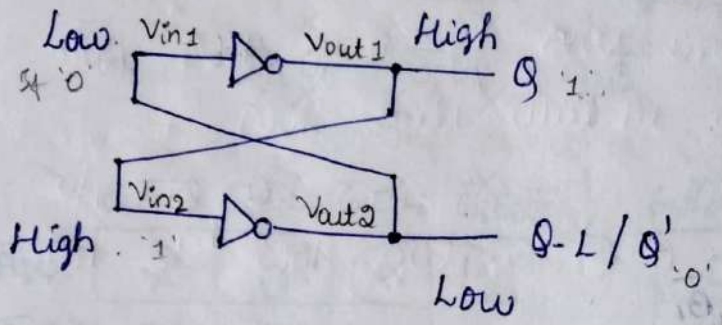
02/11/2020

UNIT - 3

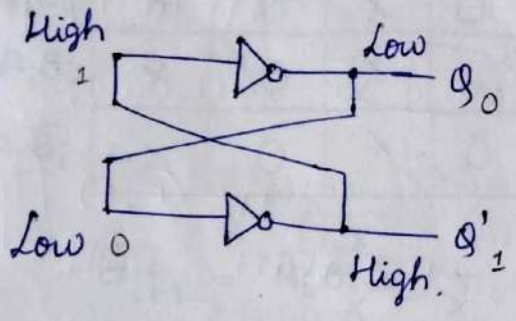
SEQUENTIAL CIRCUITS

FLIP - FLOPS AND ITS APPLICATION :

* **Bistable element**
* The simplest sequential circuit.
* Two stages.
  - One stage variable, says Q = 0/1.



One stable state '1'



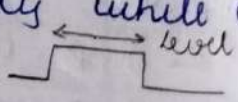
Another stable state '0'

Flip - Flops :

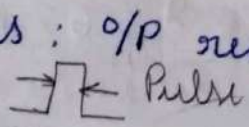
* A flip flop is a bi-stable device : a circuit having 2 stable condition (0 or 1)

* 3 Classes of flip flops.

i. Latches : o/p respond immediately while enabled (level sensitive) (no timing control)



ii Pulse triggered flip flops : o/p response to the triggering pulse



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iii edge - triggered flip flops : o/p responses to the Control input edge. ↑ ↓ edge

Conventions :

* The circuit is set means o/p = 1
* The circuit is reset means o/p = 0.
* Flip flops have two o/p Q & Q' or (Q and $\bar{Q}$)
* Q_t or Q : Present state

  Q_{t+1} or Q^+ : next state.

  Q_{t-1} or Q^- : Previous state

set = 1
reset = 0

Types of Flip flops :

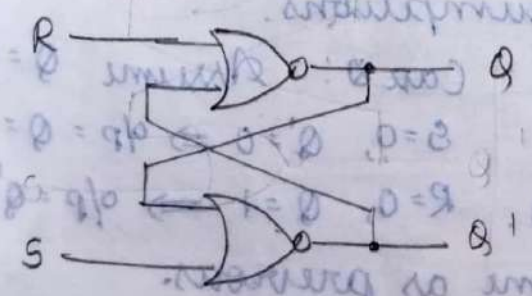
1. SR Latch (set - reset Latch)
2. JK flip flop
3. D - flip flop (Delay FF)
4. T - flip flop. (Toggle FF)

SR Latch :

An SR latch consist of.

* S (set) input : set the ckt
* R (reset) i/p : reset the ckt
* Q & Q' o/p : Output of the SR latch in normal and compliment form.

SR Latch using NOR gate :



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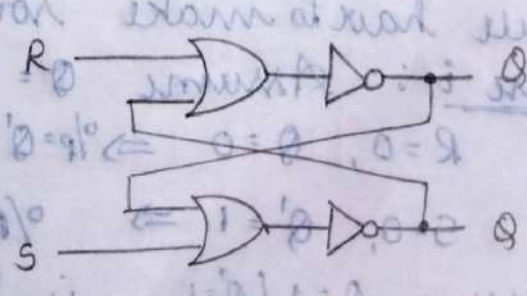

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Inputs		Outputs		
S	R	Q	Q'	
0	0	Q	Q'	→ Previous
0	1	0	1	→ reset
1	0	1	0	→ set
1	1	0	0	→ Invalid.

Simplified TT

Previous

Q	S	R	Q^+	$\bar{Q}^+$
0	0	0	Q(0)	$\bar{Q}(1)$
0	0	1	0	1
0	1	0	1	0
0	1	1	–	–
1	0	0	Q(1)	$\bar{Q}(0)$
1	0	1	0	1
1	1	0	1	0
1	1	1	–	–

Cases :

i. (0 1) i/p :
(S R)

In NOR gate If any one of the i/p is 1, o/p = 0
∴ 1st NOR gate will be enabled & produces the o/p Q = 0.
for 2nd NOR gate → S = 0, Q = 0 → o/p = 1 = Q'

ii] (1, 0) i/p :
Procedure is same as (1, 0) i/p.

iii] (1, 1) i/p :
Here, Both the NOR gate ~~are~~ will be enabled & Produces the o/p Q = 0 & Q' = 0. respt.
But when Q = 0, Q' ≠ Q ≠ Q'
But Q ≠ Q' ≠ 0 ∴ This is invalid

iv] (0, 0) i/p :
Here non of the NOR gate will be enabled.
∴ we have to make some assumptions.

Case i : Assume Q = 0.
R = 0, Q = 0 ⇒ o/p = Q' = 1
S = 0, Q' = 1 ⇒ o/p = Q = 0.

~~Case 2~~ : Assume Q' = 0
S = 0, Q' = 0 ⇒ o/p = Q = 1
R = 0, Q = 1 ⇒ o/p = Q' = 0

III Assume Q = 1 / Q' = 1 ∴ o/p is same as previous.

Scanned with CamScanner

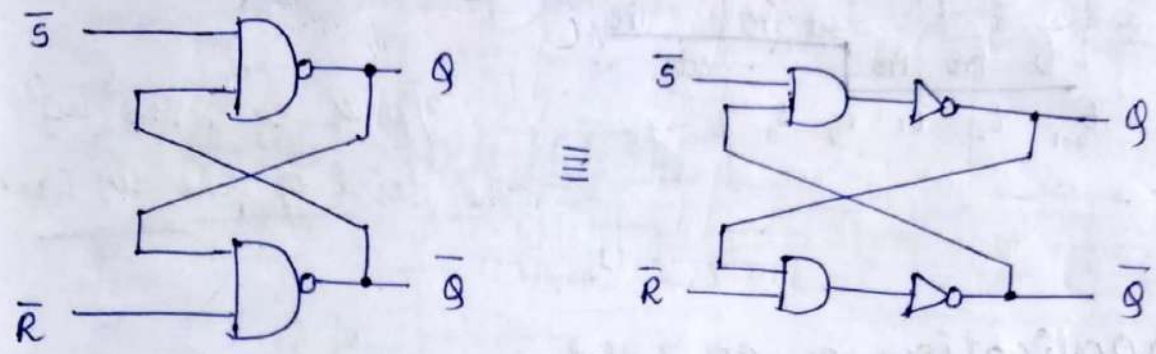
03/11/2020

SR Latch using NAND gate :

T.T for both SR using NAND & NOR is same.

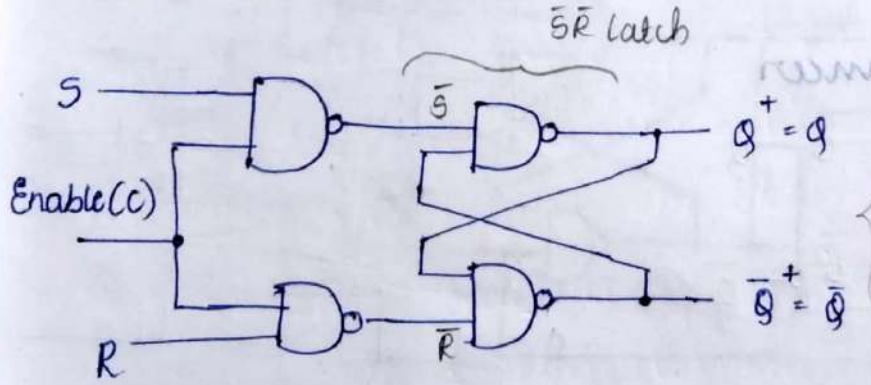
NAND → If one of the i/p is 0, o/p = 1

$\bar{S}\bar{R}$ Latch :

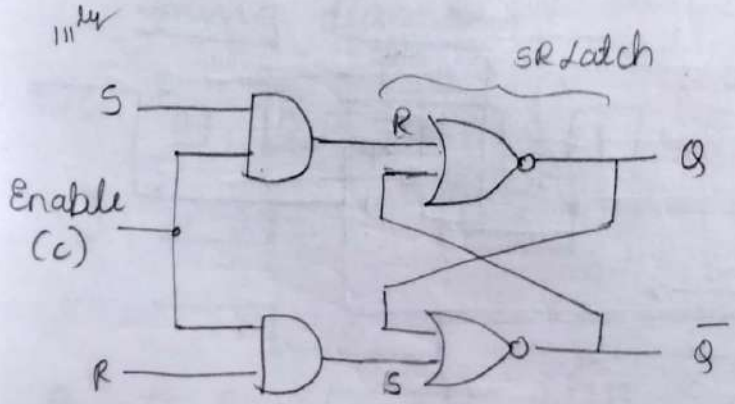


	I/P		O/P		
S R	$\bar{S}$	$\bar{R}$	Q^+	$\bar{Q}^+$	
1 1	0	0	1*	1*	→ Unpredictable
1 0	0	1	1	0	→ set
0 1	1	0	0	1	→ reset
0 0	1	1	Q	$\bar{Q}$	→ Previous

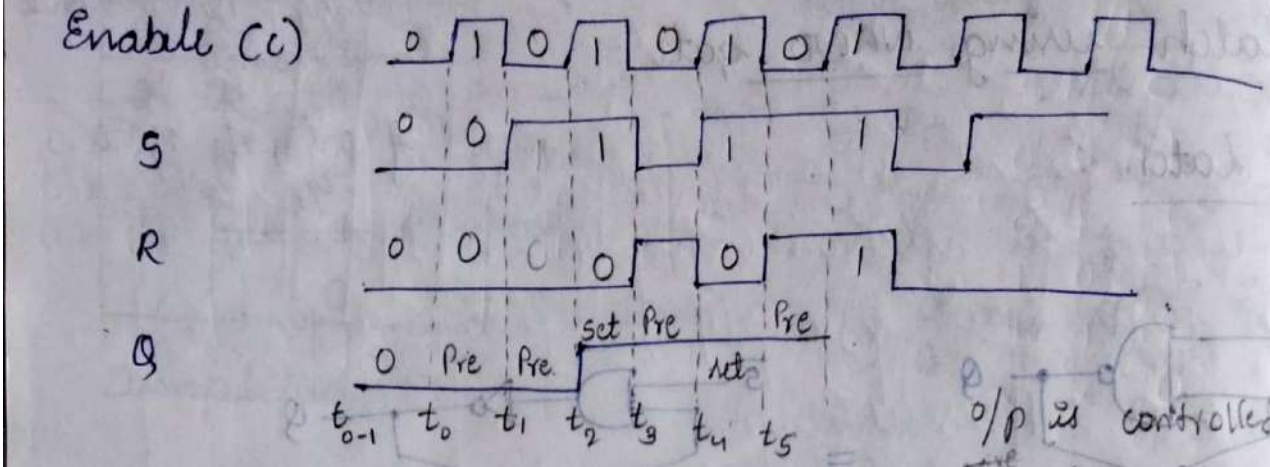
Gated SR latch.



i/p			o/p	
S	R	C	Q^+	$\bar{Q}^+$
0	0	1	Q	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1* — unpredi
X	X	0	Q	$\bar{Q}$



Timing diagram

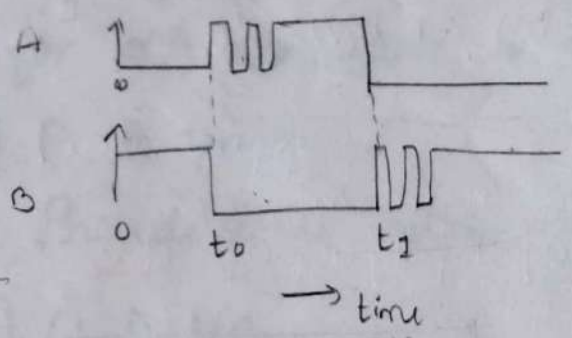


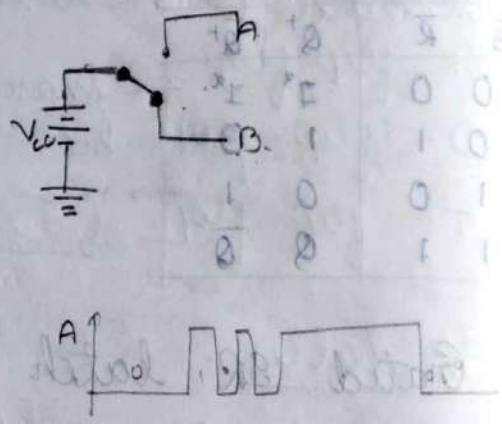
o/p is controlled by the level of the clk input

05/11/2020

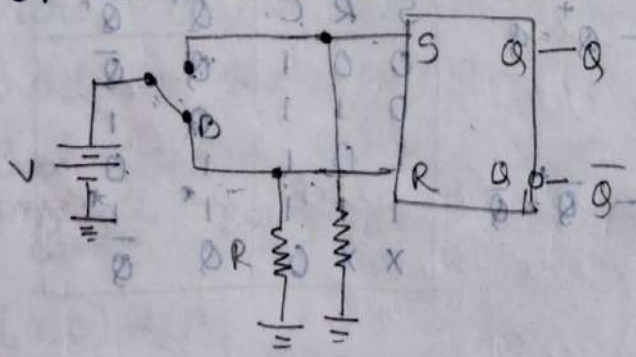
An application of SR latch:

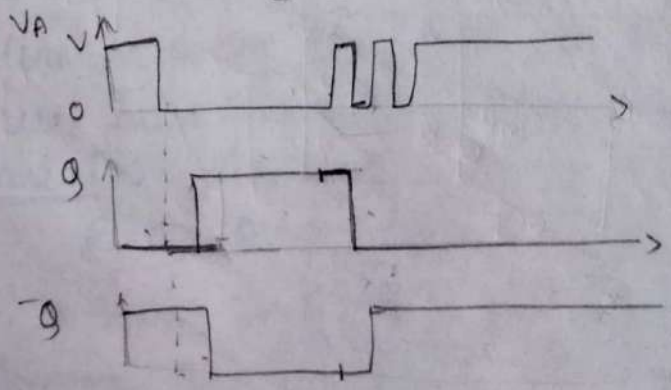
a) Effects of contact bounce:

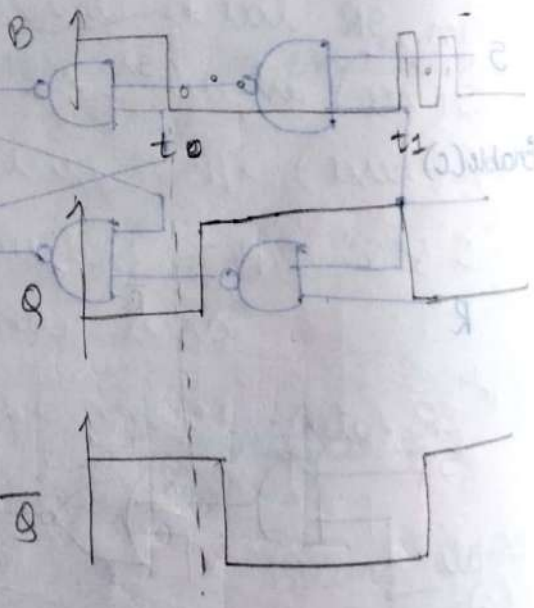




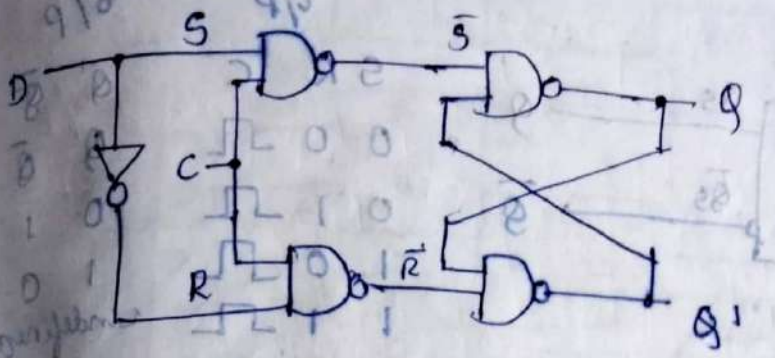
b) A switch debouncer



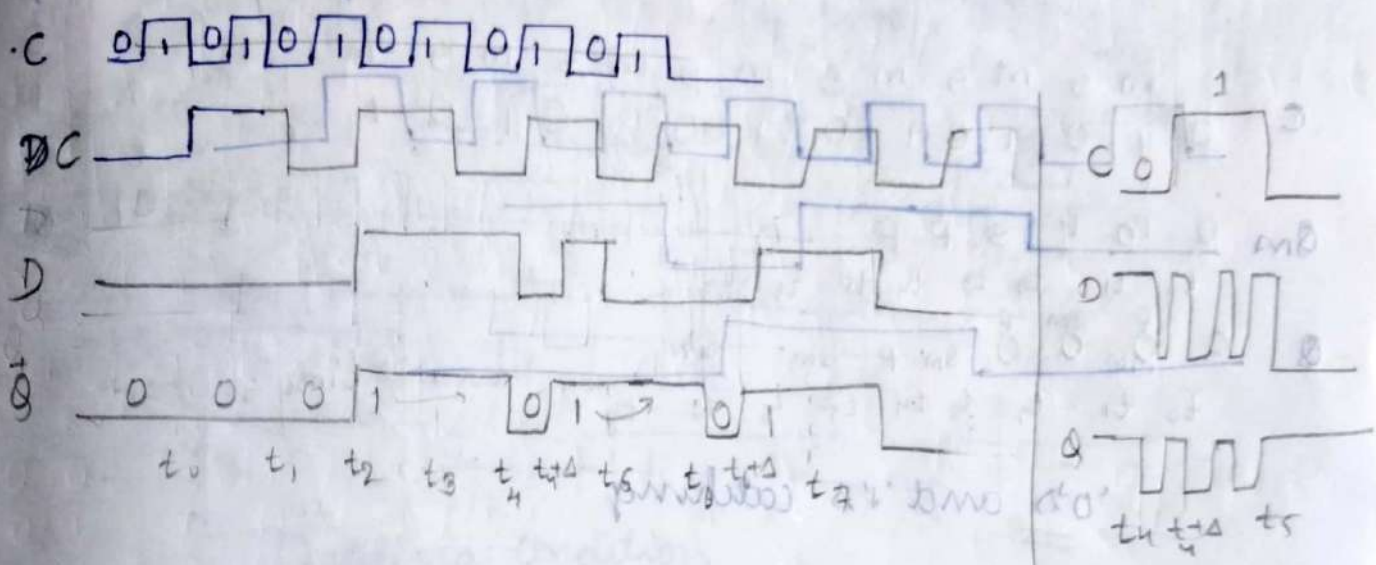




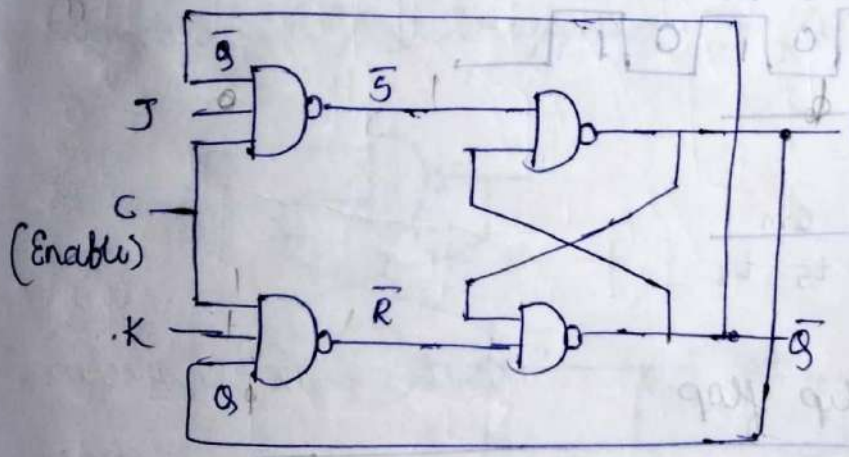
Gated D Latch



i/p		o/p	
D	C	Q^+	$\overline{Q^+}$
0	1	0	1
1	1	1	0
X	0	Q	$\bar{Q}$

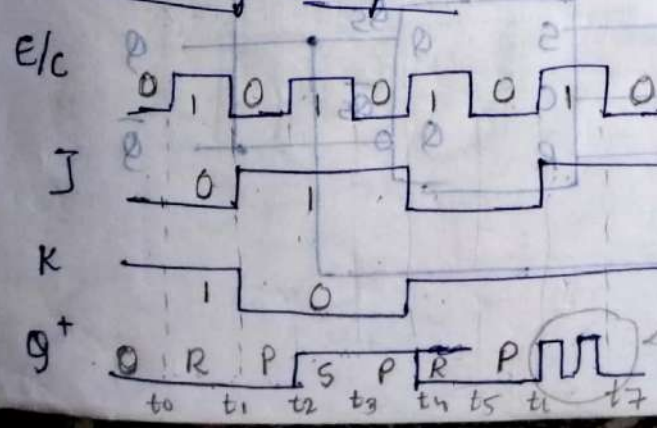


Gated J-K flip flop



C	J	K	Q	S	R	Q^+	$\overline{Q^+}$
0				X	X	Q	$\bar{Q}$
1	0	0		0	0	Q	$\bar{Q}$
1	0	1		0	1	0	1
1	1	0		1	0	1	0
1	1	1				~~invalid o/p~~	
						$\bar{Q}$	Q

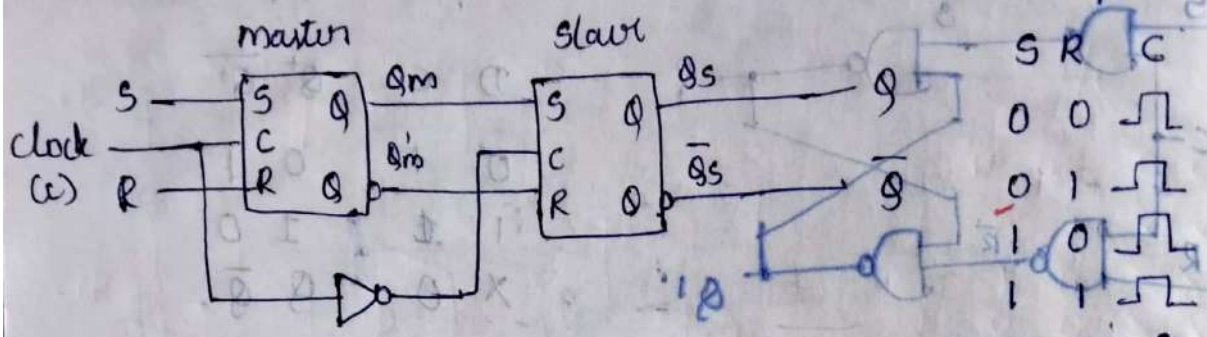
Timing diagram



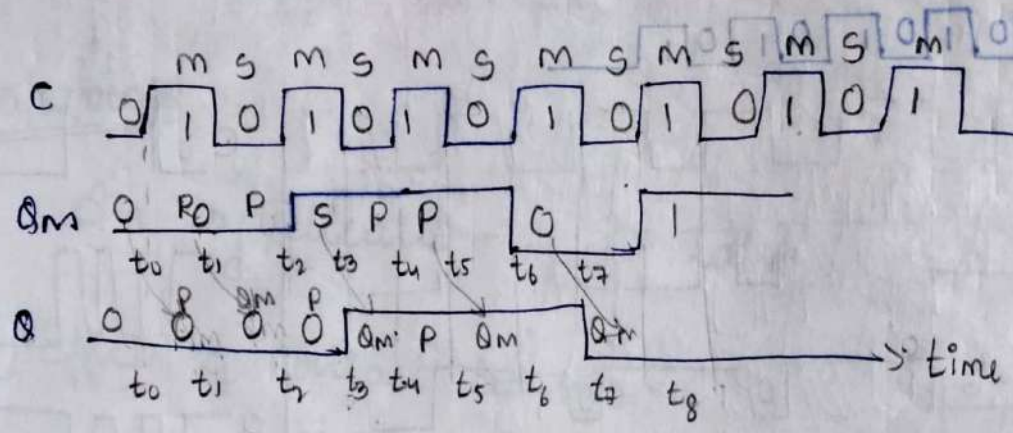
for JK, if J=1, K=1, clk=1 for a long period of time, Q o/p will toggle as long as clk is high, which makes the o/p of the flip flop unstable. This problem is called race around condition

Rage around condition

Master-Slave SR flip flop

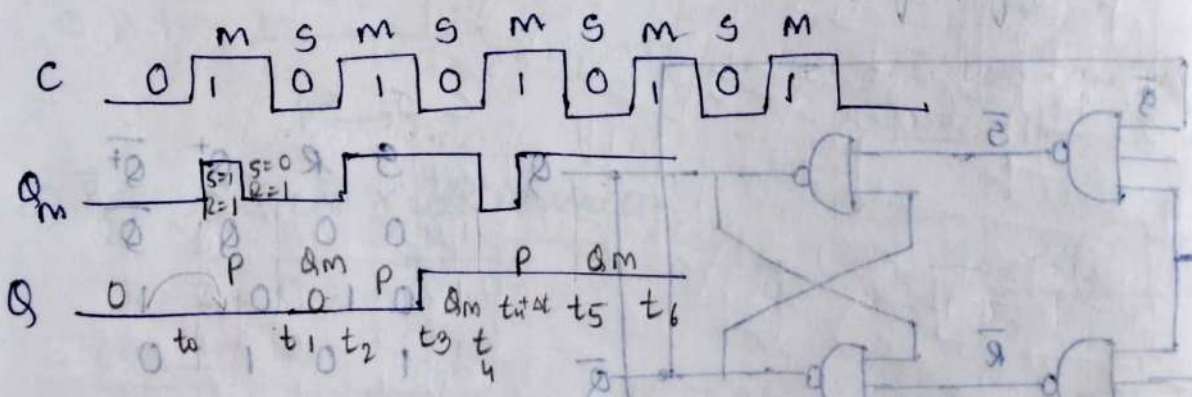


i/p S	R	C	o/p Q	Q̄
0	0	↑	Q	Q̄
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	undefined	
x	x	0	Q	Q̄

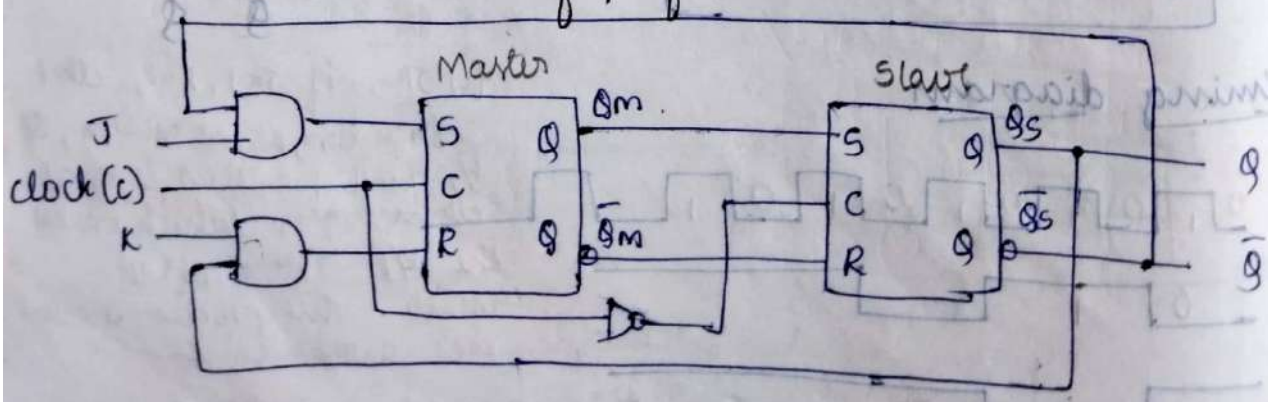


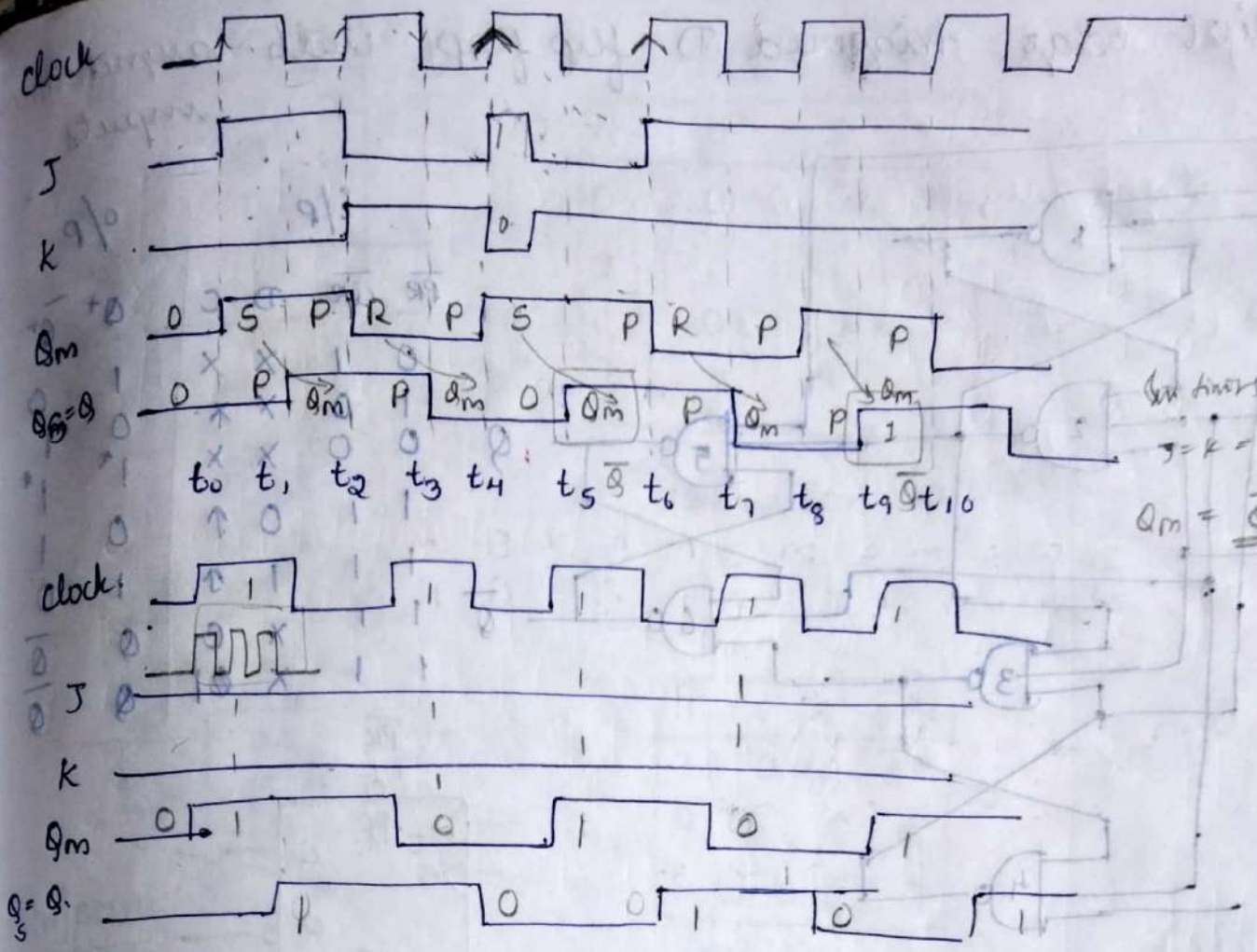
'0's and '1's catching

* Pulse triggered.



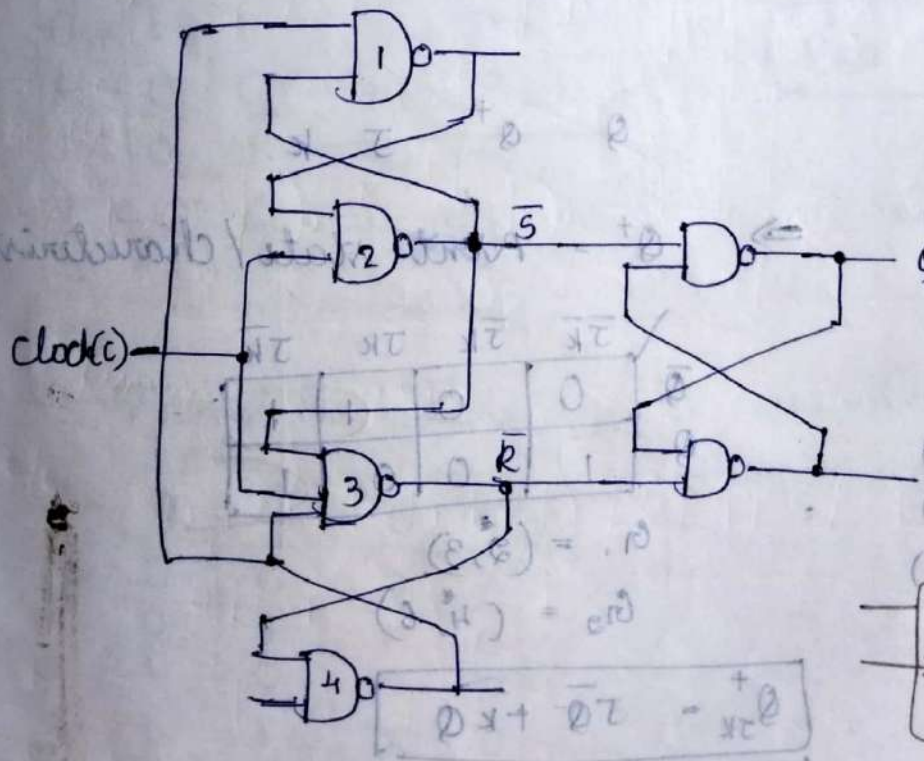
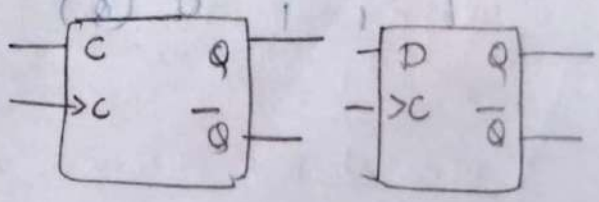
Master slave JK flip flop.





Toggling condition

Positive edge - triggered D flip flop.



i/P		o/P	
D	C	Q^+	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$