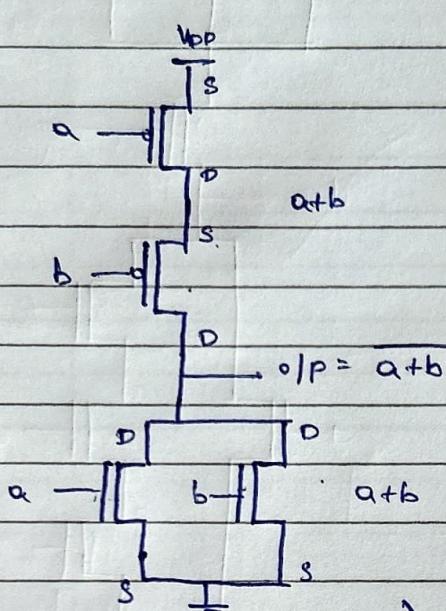


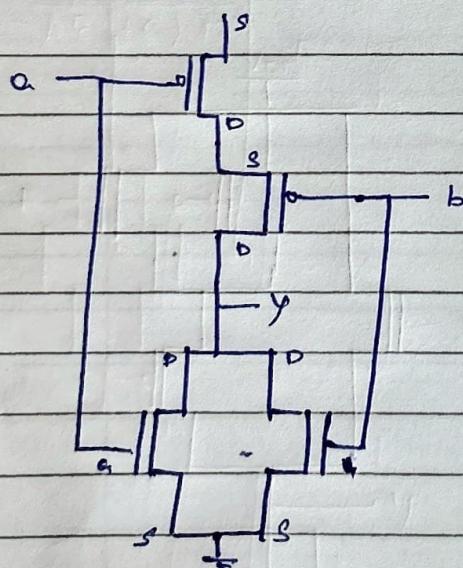
1. NAND gate \rightarrow Refer obs book:

2. NOR gate:-

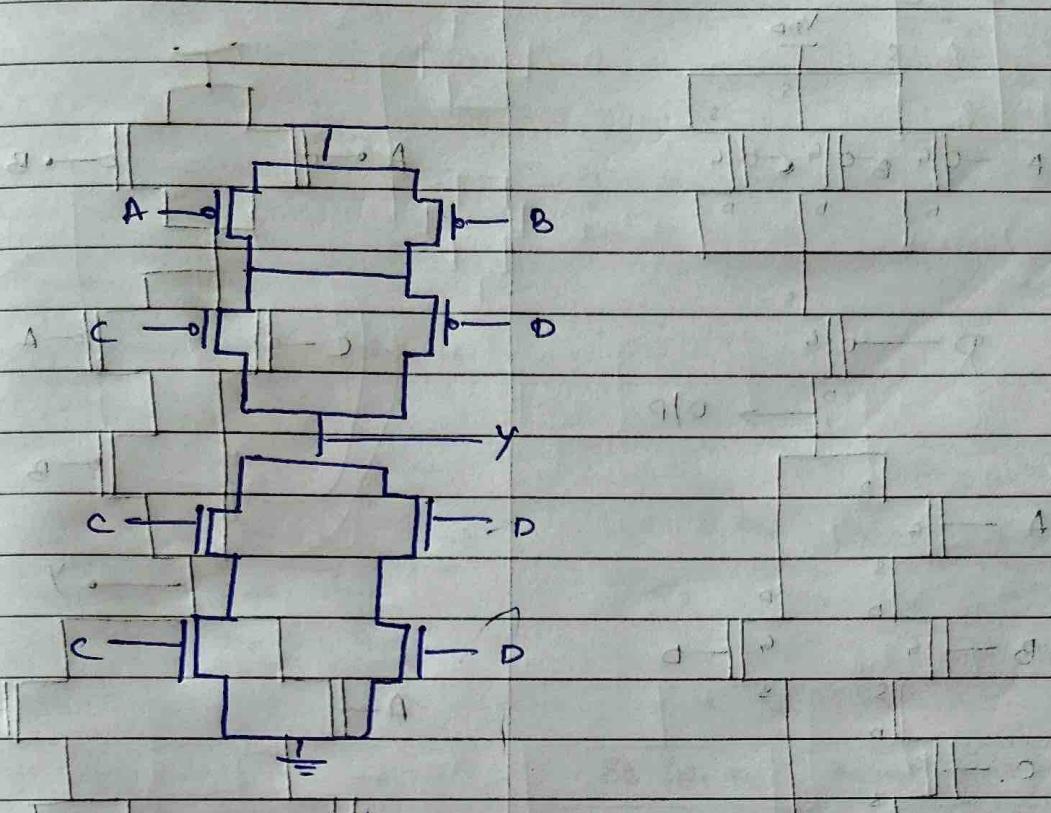


a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

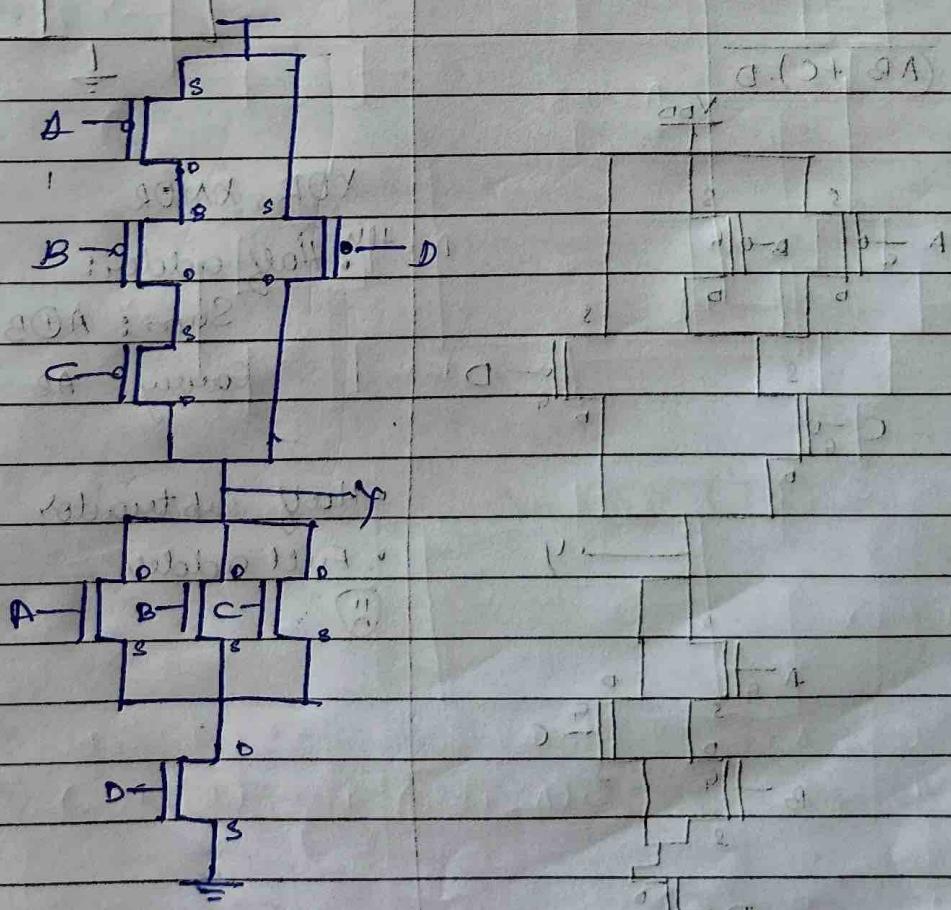
) Same



$$1. \quad Y = \overline{AB} + CD$$



$$2. \quad Y = \overline{(A+B+C)} \cdot D$$



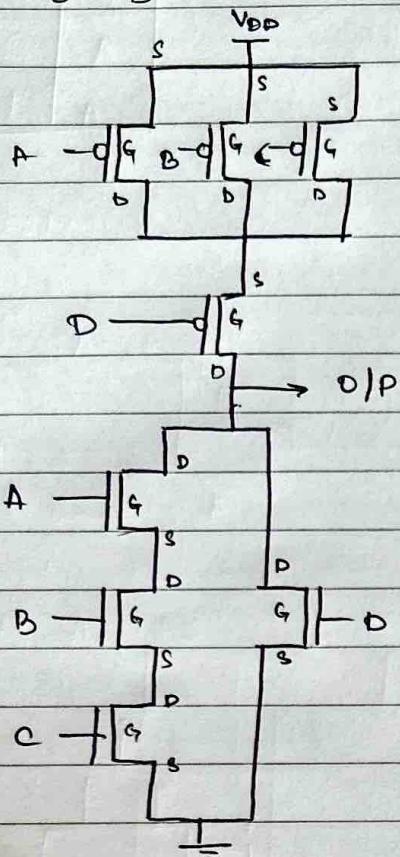
$A \oplus B$

$V_{GS} > V_t$
 $V_{GS} < -V_{tL}$

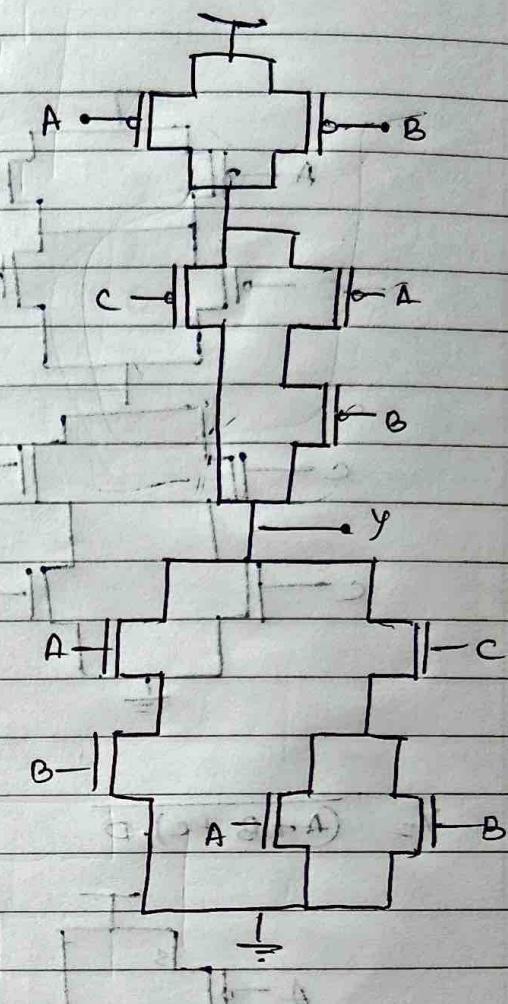
classmate

Date _____
Page _____

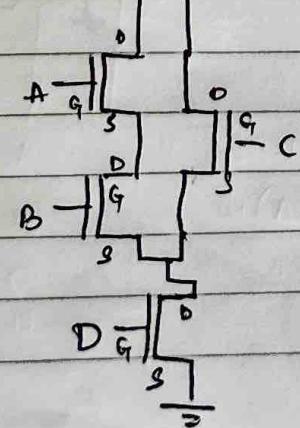
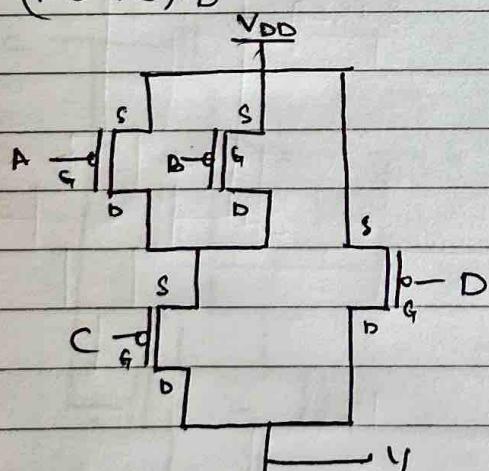
3. $y = \overline{ABC + D}$



5. $\overline{AB + C(A+B)}$



4. $y = \overline{(AB + C) \cdot D}$



XOR, XNOR

HW: Half adder:

Sum: $A \oplus B$

Carry: AB

• Half subtractor

• Full adder



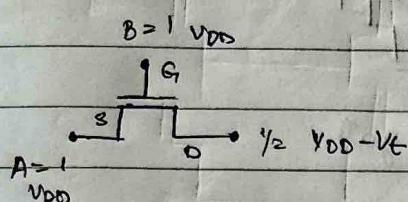
Transfer information
only when MOS is ON'

Pass transistors:

Either nMOS or pMOS

Ex: NAND \rightarrow L \rightarrow CMOS

but in pass, only 2 are required.



Density \uparrow Power \downarrow

$$nMOS: V_{GS} \geq V_{th}$$

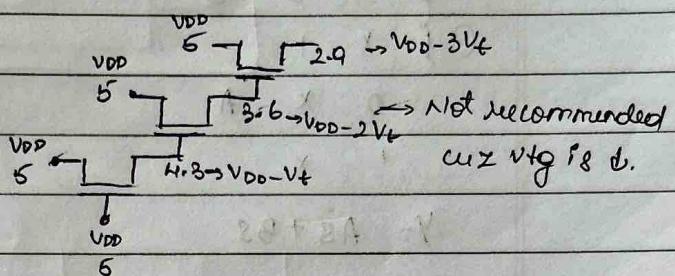
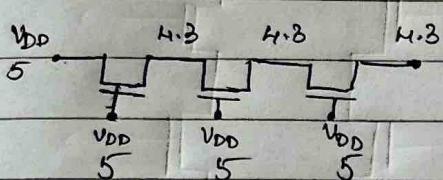
$$\text{min: } V_{GS} = V_{th}$$

$$V_{th} - V_g$$

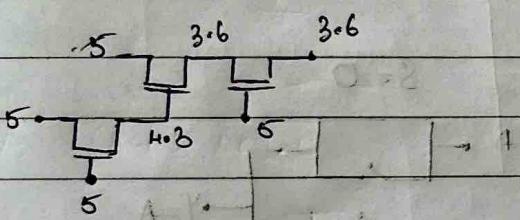
$$V_g - V_s \geq V_{th}$$

$$\sqrt{V_s} = V_g - V_{th}$$

$$\text{min: } S = V_{DD} - V_{th}$$



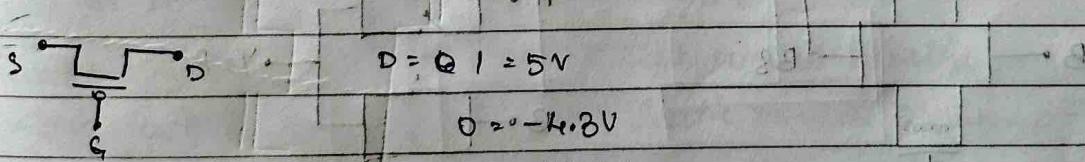
So for each transistor OLP will be the vtg at
gate - V_t



$$D = 0 = 0V$$

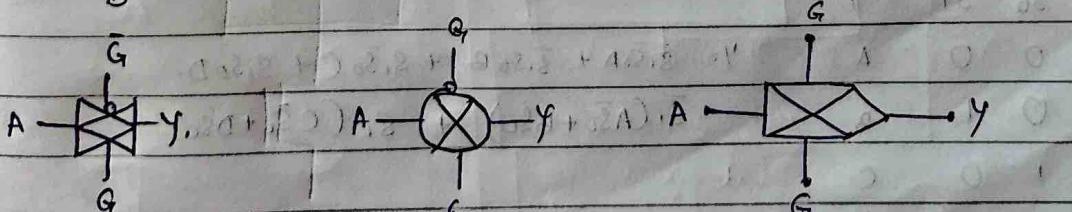
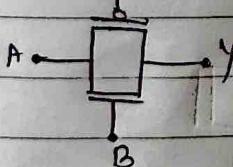
$$= 1 = 4.3V$$

should be 5V.

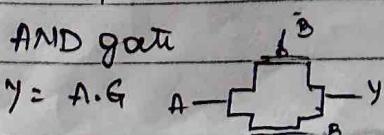


should be 0.

\rightarrow Transmission Gate (T_G)

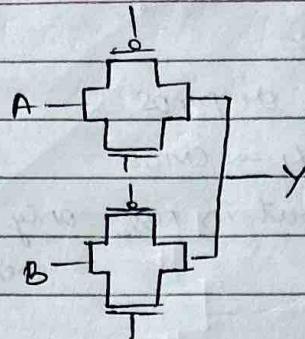


AND gate



G	Y
O	A
I	A

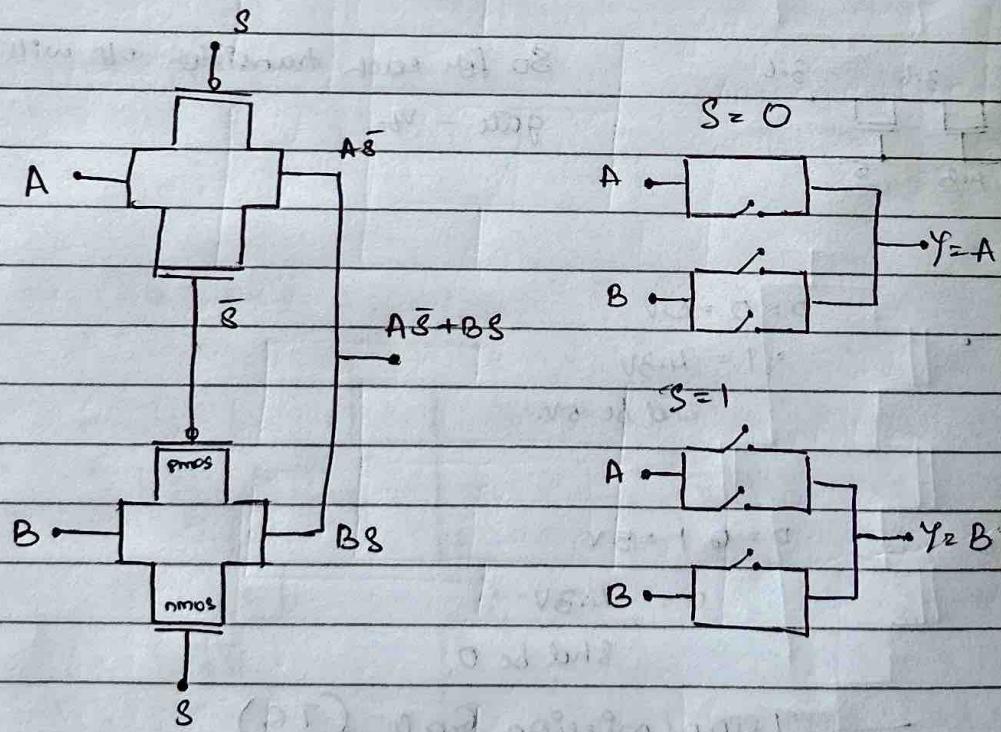
2:1 MUX



S	A	B	Y
1	x	0	B
0	x	1	A
0	x	A	
1	x		

OR gate

$$Y = A\bar{S} + B\bar{S}$$



4:1 MUX

$$S_0 \quad S_1 \quad Y$$

$$0 \quad 0 \quad A$$

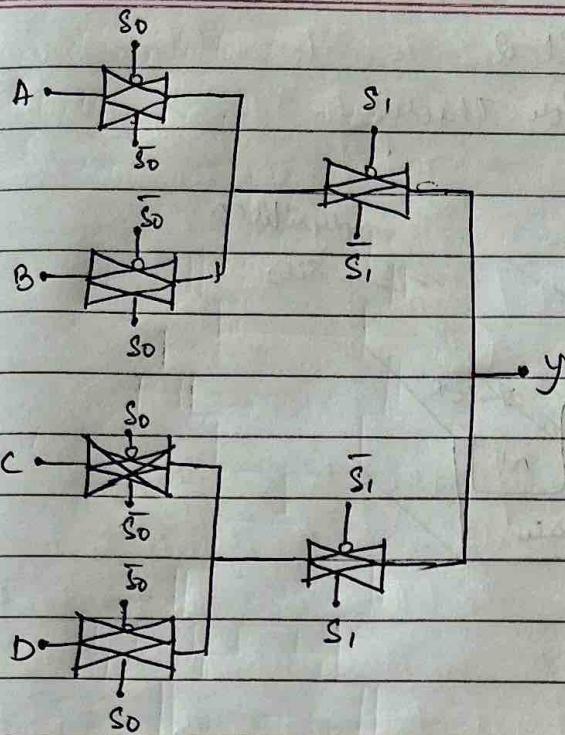
$$Y = \bar{S}_1 \bar{S}_0 A + \bar{S}_1 S_0 B + S_1 \bar{S}_0 C + S_1 S_0 D.$$

$$0 \quad 1 \quad B$$

$$- \bar{S}_1 (\bar{A}\bar{S}_0 + B\bar{S}_0) + S_1 (C\bar{S}_0 + D\bar{S}_0)$$

$$1 \quad 0 \quad C$$

$$1 \quad 1 \quad D$$



- Fabrication
 - VLSI design flow
- } At the last
of
after II unit

BJT

- * Current controlled \mathbb{I}_B
- * Low input imp
- * $g_m \tau$
- * Low packing density
- * more static power consumption
- * Low noise margin

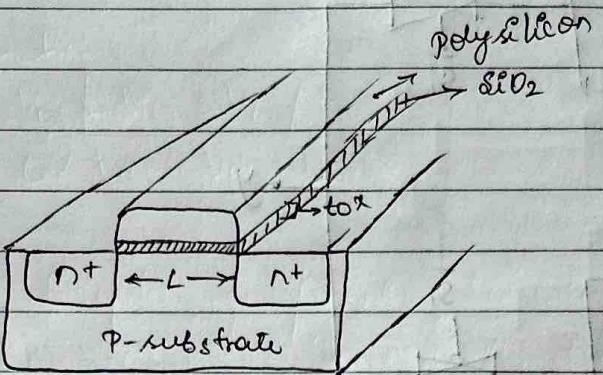
MOSFET

- * Voltage controlled (V_{GS})
- * High τ_{mp} is \mathbb{I}/P imp
- * g_{mb}
- * High packing density
- * Static power consumption ↓
- * High noise margin.

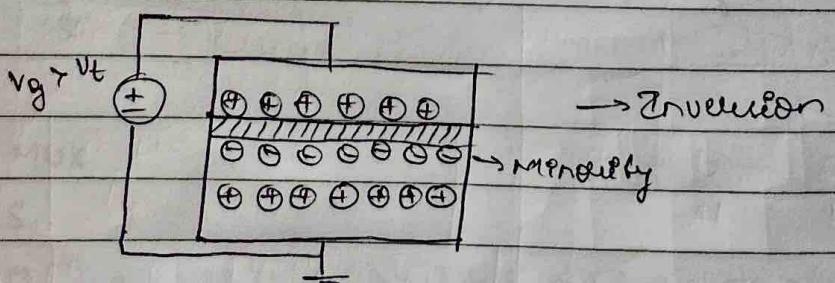
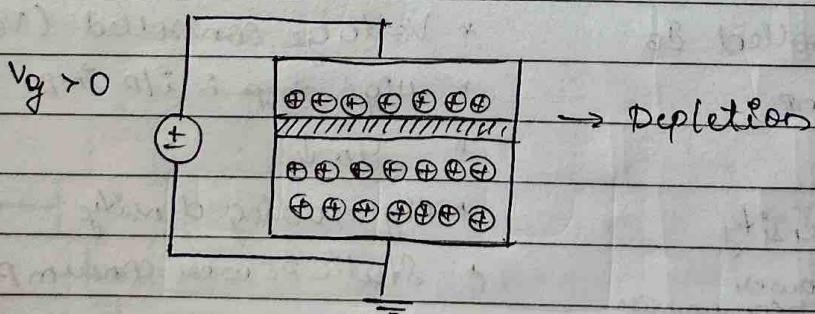
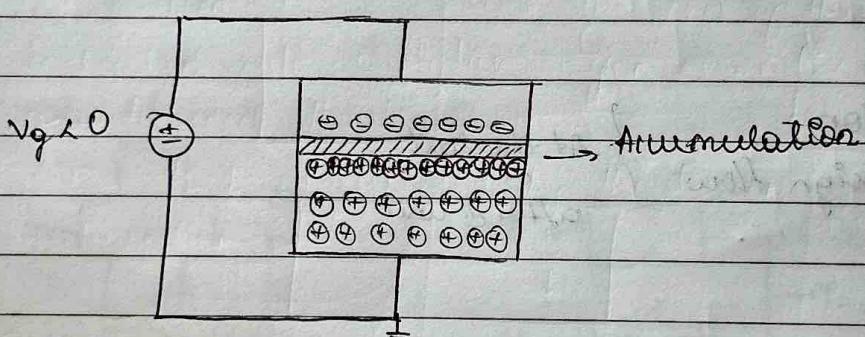
Unit-2

MOS transistor Theory

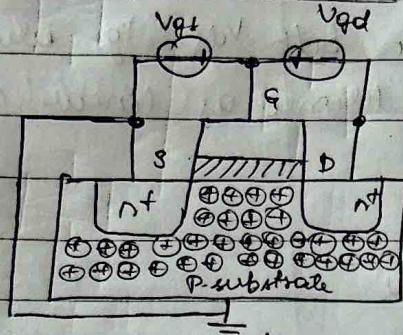
nmos:



Channel creation:-

 V_t can be varied using* $t_{ox} \rightarrow t_{ox} \downarrow \rightarrow V_t \downarrow$ * ϵ_{ox}

Operation of nmos device:



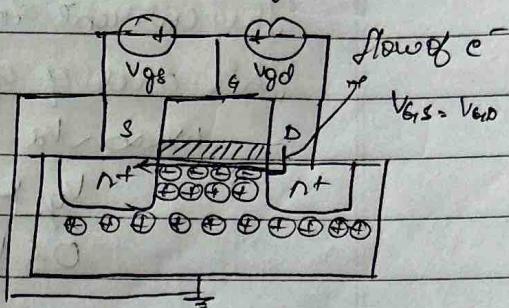
1. Cutoff / Subthreshold

$$V_{gs} < V_t$$

$$V_{ds} = 0$$

2 Linear region

2 Linear region



$$V_{gs} > V_t$$

$$V_{ds} > V_t$$

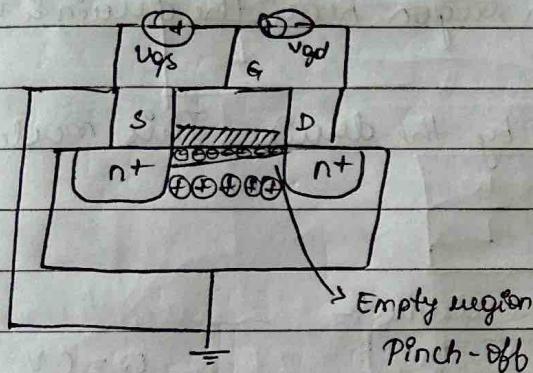
$$V_{ds} = V_{gs} - V_{gd}$$

$$V_{ds} = 0$$

$$V_{gs} > V_{ds} > V_{gd}$$

$$0 < V_{ds} < V_{gs} - V_t$$

3 Saturation



$$V_{ds} > V_{gs} > V_{gd}$$

• $V_{ds} > V_{gs} - V_t$

$$V_{ds} > V_{gs} - V_t$$

Consider fig.a. Gate to source V_{gs} i.e. $V_{gs} < V_t$. In this case only source and drain are having p_n

The junction b/w body & source /drain are zero biased so no current flows. We say that transistor is OFF & this mode of operation is called cut-off.

In fig.b. the $V_g > V_t$ the inversion region of e^- i.e. channel connects the source & drain, creating a conducting path & flowing on the transistor. But P.D b/w the drain & source is $V_{ds} = V_{gs} - V_{gd}$. Since $V_{gs} = V_{DD}$, $V_{ds} = 0$: There is no electric field tending to push current from drain to source when

a current i_{ds} flows from drain to source

The current increases when both V_{ds} & V_{gs} are increased

This mode of operation is termed as linear, non-saturated
when

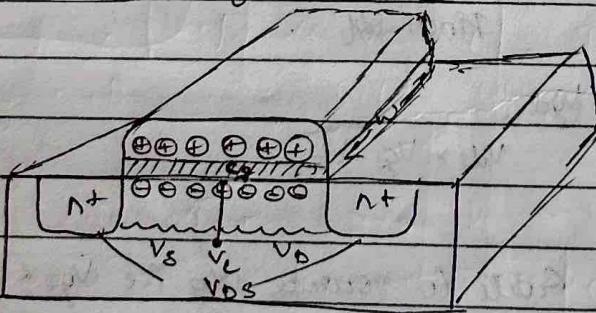
$$V_{gs} > V_{ds} > V_t$$

$$\text{Or } V_{ds} < V_{gs} - V_t$$

When V_{ds} becomes sufficiently larger i.e. $V_{gs} \downarrow$, the channel is no longer inverted near the drain & becomes pinched off as shown in fig. In this case the conduction is due to drift of e^- under the influence of +ve voltage applied at the drain. As e^- reach the end of the channel, they are inducted into depletion region near the drain & accelerated near towards the drain.

ceases to be influenced by the drain. This mode is called saturation.

I-V characteristics of MOS device :-



$$Q = CV$$

$$= C_g (V_{gc} - V_t)$$

$$V_{gc} = ?$$

$$V_C = V_g + V_d$$

∴

$$= V_g + V_{ds} \rightarrow (3)$$

$$C = \frac{\epsilon A}{d} \rightarrow (5)$$

$$V_{gc} = V_{gs} - V_{ds}^2 \rightarrow (4)$$

$$C_g = \frac{\epsilon_0 \epsilon_r L W}{t_{ox}} \rightarrow (6)$$

$$I_{ds} = \frac{Q}{4t} = \frac{Q}{L/V} = \frac{QV}{L}$$

$V_d \propto E$

$$I_{ds} = \frac{\epsilon_0 \epsilon_r W}{t_{ox}} \frac{(V_{gs} - V_{ds} - V_t)}{2} \cdot \frac{W}{L} \cdot \frac{V_{ds}}{L}$$

$V_s \propto E \propto \frac{V_{ds}}{L}$

$$= \frac{C_{ox} W}{L} \mu \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$E = \frac{V_{ds}}{L} \rightarrow (8)$$

$$V = \frac{W V_{ds}}{L}$$

a current i_{ds} flows from drain to source

The current increases when both V_{ds} & V_{gs} are increased

This mode of operation is termed as linear, non-saturated when

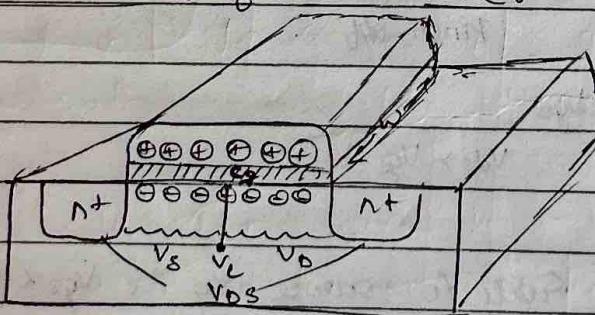
$$V_{gs} > V_{ds} > V_t$$

$$\text{OR } V_{ds} < V_{gs} - V_{gd}$$

When V_{ds} becomes sufficiently larger i.e. V_{gs} , the channel is no longer inverted near the drain & becomes pinched off as shown in fig. In this case the conduction is due to drift of e^- under the influence of +ve voltage applied at the drain. As e^- reach the end of the channel, they are induced into depletion region near the drain & accelerated towards the drain.

ceases to be influenced by the drain. This mode is called saturation.

I-V characteristics of MOS device :-



$$Q = CV$$

$$= C_g (V_{gc} - V_t)$$

$$V_{gc} = ?$$

$$V_C = V_s + V_D$$

$$= V_s + \frac{V_{Dg}}{d} \rightarrow (3)$$

$$C_s = \frac{\epsilon A}{d} \rightarrow (5)$$

$$tgc = V_{gs} - \frac{V_{Dg}}{d} \rightarrow (4)$$

$$C_g = \frac{\epsilon_0 \epsilon_r L W}{t_{ox}} \rightarrow (6)$$

$$I_{ds} = \frac{Q}{4t} = \frac{Q}{L/V} = \frac{QV}{L}$$

$$V \propto E$$

$$V \propto M E \rightarrow (7)$$

$$V \propto M \frac{V_{DS}}{L}$$

$$E = \frac{V_{DS}}{L} \rightarrow (8)$$

$$V = \frac{M V_{DS}}{L}$$

$$I_{ds} = \frac{\epsilon_0 \epsilon_r L W}{4t} \left(\frac{V_{gs} - V_{ds} - V_t}{2} \right)^2 \cdot M_{NDS} \cdot \frac{1}{L}$$

$$= \frac{C_{ox} W M}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \rightarrow (9)$$

$$I_{DS} = \beta \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right] \rightarrow \text{Linear}$$

$$V_{DS} = V_{GS} - V_t = V_{DSAT}$$

$$I_{DS} = \beta \left[(V_{GS} - V_t)^2 - V_{GS} \cdot V_t \right]$$

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_t)^2$$

MOS tr. operates in 3 regions - Cutoff, linear & saturation.

* Cut-off : $V_{GS} < V_t$. There is no channel & almost 0 current flows from D to S. E.g., $I_{DS} = 0$.

- * In the other two regions the gate attracts the carrier to form a channel.
- * The e^- drifts from S to D at a rate proportional to the E. field b/w these regions.
- * Thus if we compute i.e., the amount of charge in the channel & the rate at which it moves.

$$Q = CV$$

$$Q_{\text{channel}} = C_g (V_{GS} - V_t)$$

where $C_g \rightarrow$ gate capacitance

$V_{GC} \rightarrow$ gate channel potential

$V_{GS} - V_t \rightarrow$ min amount of V_G that has inverted from P to N

Average $V_L = \frac{V_S + V_D}{2} = \frac{V_S + V_{DS}}{2}$	$\rightarrow (3)$
--	-------------------

* The mean diff b/w gate & channel potential V_{GC} is

$$V_{GC} = V_{GS} - V_{DS} \rightarrow (4)$$

* To find gate cap C_g :

* If the gate has length L, width w & oxide thickness t_{ox}

$$C_g = \frac{\epsilon_0 \epsilon_r L w}{t_{ox}} \quad C_{ox} = \epsilon_0 \epsilon_r \quad \text{where } \epsilon_{ox} = \epsilon_0 \epsilon_r$$

where $C_{ox} = \text{cap of unit area of gate oxide}$

- * Each carrier in the channel is accelerated to an avg velocity (drift velocity) proportional to the lateral E. field & constant of proportionality is called carrier mobility

$$V_d \propto E$$

- * The E. field is the vdg diff b/w D & S by channel length

$$E = \frac{V_{DS}}{L}$$

- * The time req. for carrier to cross channel length by drift velocity (L/V_d) is the current.

$$I_{DS} = \frac{Q}{\Delta t} = \frac{Q}{\frac{L}{V_d}} = \frac{QV_d}{L}$$

$$B = \mu C_o n \frac{W}{L}$$

- * When $V_{GS} > V_t$ but V_{DS} is relatively small, the device is resistive but $\frac{V_{DS}}{\Delta t} \ll V_{GS} - V_t$. It increases almost linearly with V_{DS} just like ideal resistor.

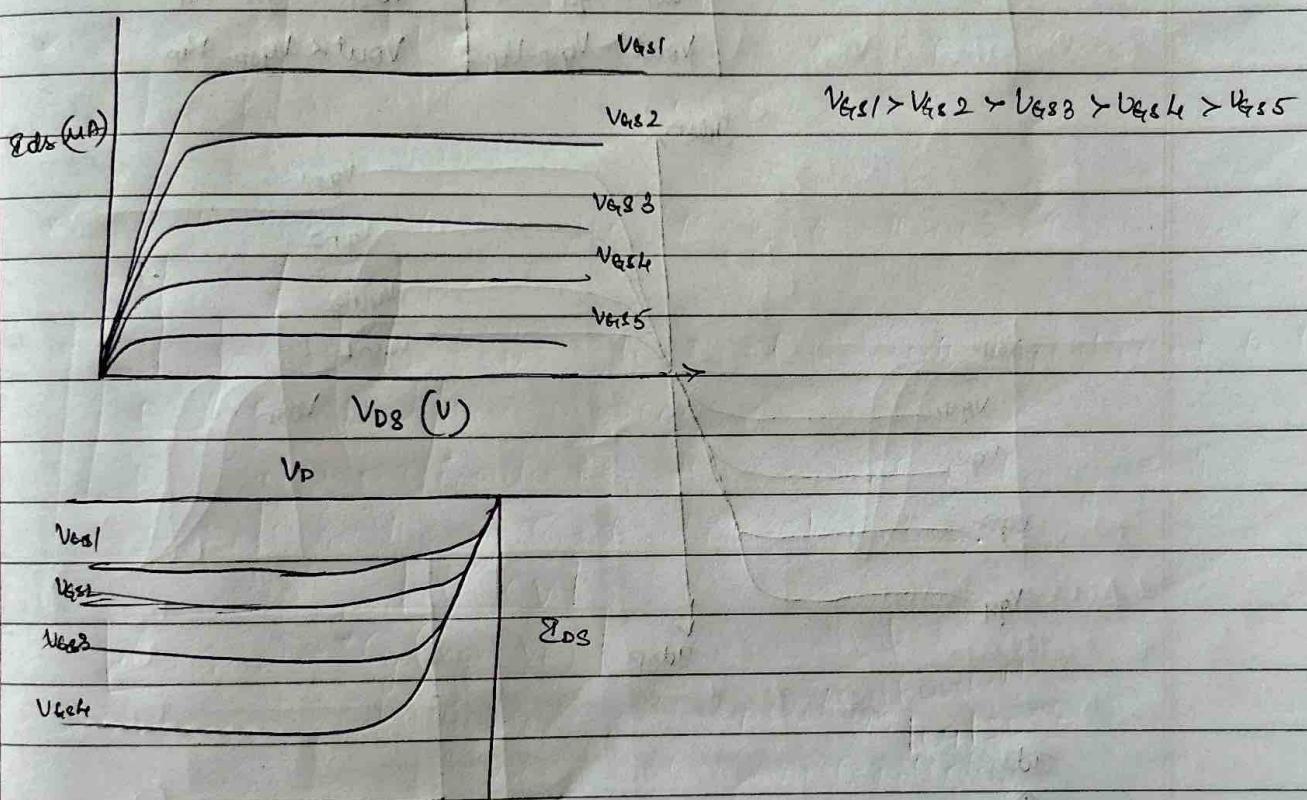
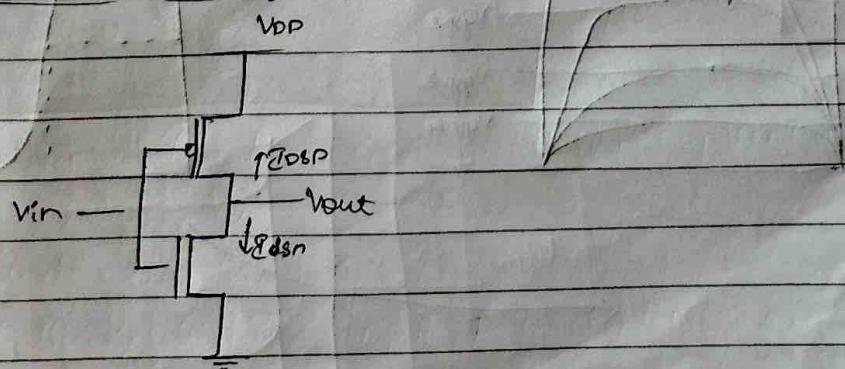
- * In the saturation region, $V_{DS} > V_{DSat} \equiv V_{GS} - V_t$. The channel is no longer inverted in the vicinity of D. we say channel is pinched off. Beyond this point the V_{DSat} increasing drain voltage V_D has no further effect on current

$$I_{DS} = \frac{B}{2} (V_{GS} - V_t)^2$$

$$V_{DSat} = \frac{B}{2} (V_{DD} - V_t)^2$$

Summary:

Region /	I_{DS}	Condition
Cut-off	$I_{DS} = 0$	$V_{GS} < V_t$
Linear	$I_{DS} = B \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$	$V_{GS} > V_t$ $V_{DS} < V_{break}$
Saturation	$I_{DS} = \frac{B}{2} (V_{GS} - V_t)^2$	$V_{GS} > V_t$ $V_{DS} > V_{out}$

DC characteristics of CMOS inverter:

Skew,

$$B_n = B_p$$

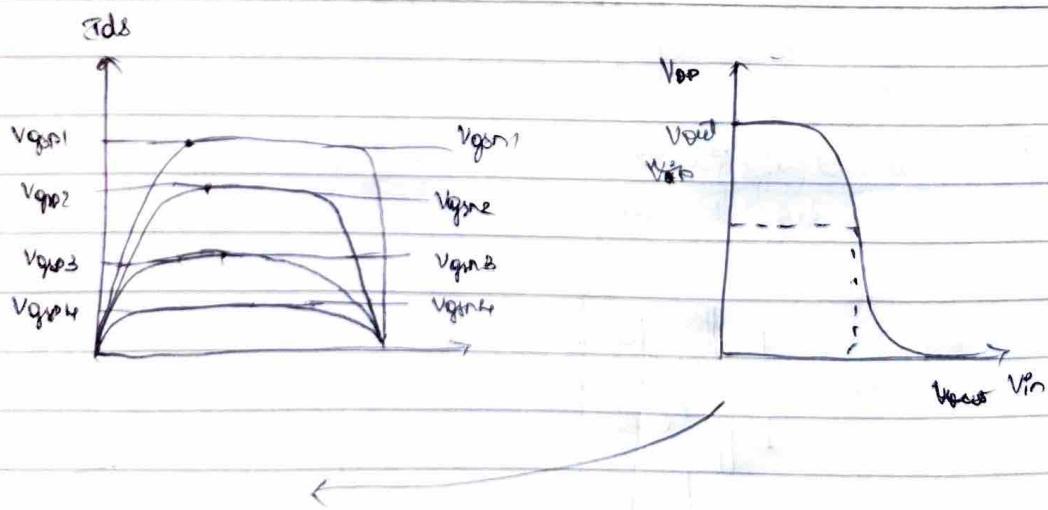
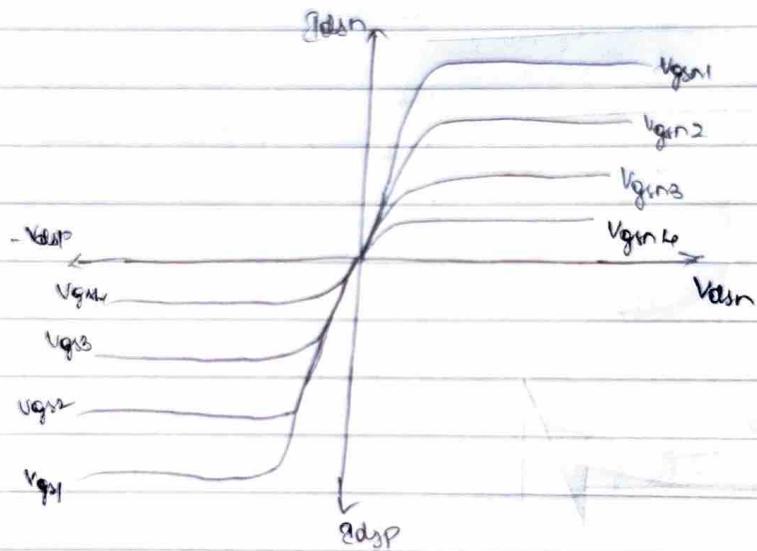
$$nMOS: V_{GSn} = V_{in}$$

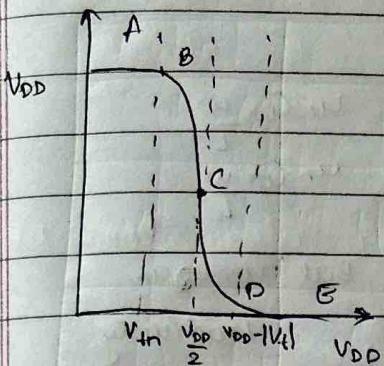
$$V_{out}$$

$$pMOS: V_{GSp} = V_{in} - V_{DD}$$

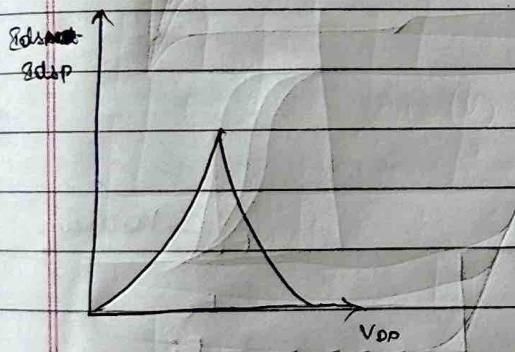
$$V_{out} =$$

	Cut off	Linear	Saturation
nmos	$V_{GSN} < V_{TN}$ $V_{IN} < V_D$	$V_{GSN} > V_{TN}$ $V_{IN} > V_{DN}$ $V_{DS} < V_{GSN} - V_{TR}$ $V_{OUT} = V_{GSN} - V_{TR}$	$V_{GSN} > V_{TN}$ $V_{IN} > V_{DN}$ $V_{DS} > V_{GSN} - V_{TR}$ $V_{OUT} >$
pMOS	$V_{GSP} > V_{TP}$ $V_{IN} - V_{DD} > V_{TP}$	$V_{GSO} < V_{TO}$ $V_{IN} - V_{DD} < V_{TO}$ $V_{DSP} > V_{GSP} - V_{TP}$ $V_{OUT} > V_{GSP} - V_{TP}$	$V_{GSP} < V_{TP}$ $V_{IN} - V_{DD} < V_{TP}$ $V_{DSP} < V_{GSP} - V_{TP}$ $V_{OUT} < V_{GSP} - V_{TP}$





Region	Condition	PMOS	NMOS	V_{out}
A	$0 < V_{in} < V_{tN}$	Linear	Cutoff	V_{DD}
B	$V_{tN} < V_{in} < \frac{V_{DD}}{2}$	Linear	Sat	$V_{DD} - \frac{V_{DD}}{2}$
C	$\frac{V_{DD}}{2} < V_{in} < V_{DD} - V_{tP}$	Saturation	Sat	$\frac{V_{DD}}{2}$
D	$V_{DD} - V_{tP} < V_{in} < V_{DD}$	Saturation	Linear	$V_{out} < \frac{V_{DD}}{2}$
E	$V_{DD} - V_{tP} < V_{in} < V_{DD}$	Cutoff	Linear	0



Region C: V_t (Switching threshold) is V_{tg} at which transition occurs

$$B_n = B_p$$

At switching threshold ($V_{in} = V_{out} = V_t$)

From the plot,

$$B_n (V_{tg} - V_{in})^2 = \frac{B_p}{2} (V_{tg} - V_{tP})^2$$

$$B_n (V_{in} - V_{tN})^2 = B_p (V_{in} - V_{DD} - V_{tP})^2$$

$$V_{in} - V_{tN} = \pm \sqrt{\frac{B_p}{B_n} (V_{in} - V_{DD} - V_{tP})}$$

$$V_{in} - V_{tN} = -\sqrt{\frac{B_p}{B_n} (V_{in} - V_{DD} - V_{tP})}$$

$$V_{in} \left(1 + \frac{B_p}{B_n}\right) = \frac{B_p}{B_n} (V_{DD} + V_{tP} + V_{tN})$$

we get correct off with -ve sign

$$\therefore B_p = B_n$$

$$\Delta V_{in} = V_{DD} + V_{tp} + V_{tr}$$

$$\text{WKT, } V_{tp} = -V_{tr}$$

$V_{in} =$	$\frac{V_{DD}}{2}$
------------	--------------------

$$\beta_p = \mu_p C_{ox} \frac{w}{L}$$

$$\beta_n = \mu_n C_{ox} \frac{w}{L}$$

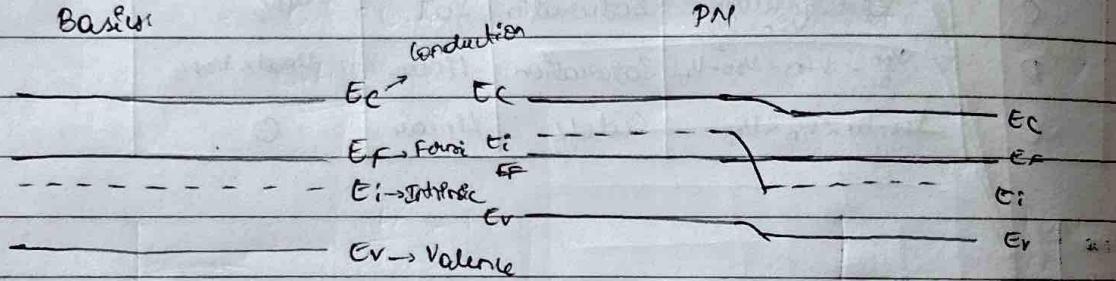
But $\mu_n \approx \mu_p$

Practically

∴ DC graph is shifted slightly to the left

Energy band gap:

Basics:



Syllabus:-

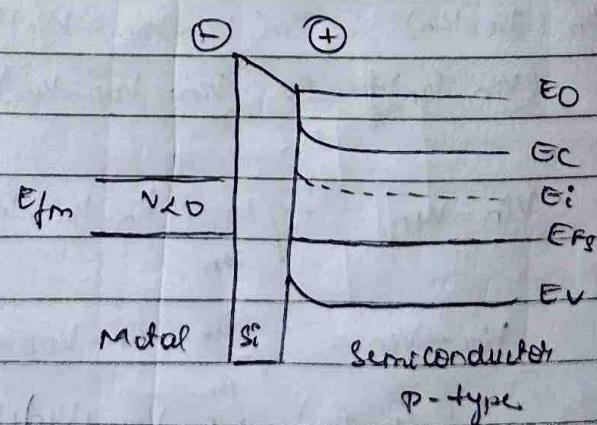
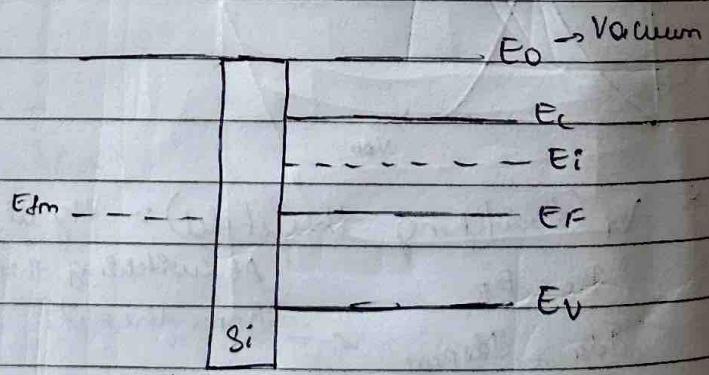
NMOS

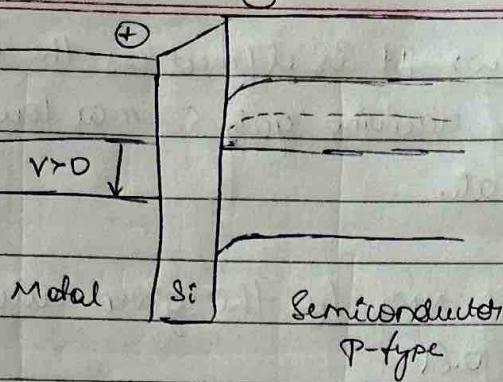
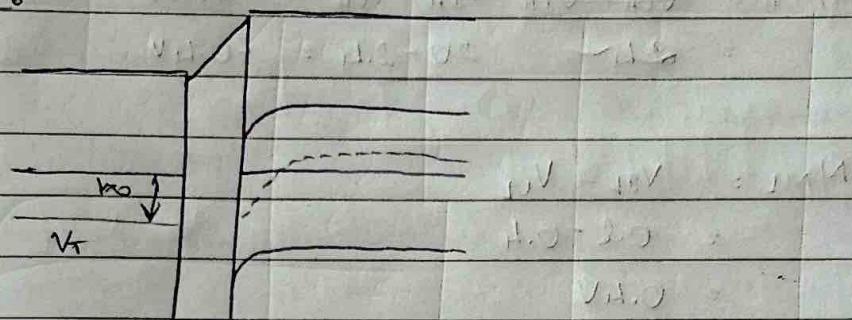
1. Accumulation

2. Depletion

3. Inversion

Metal
Insulator
Si



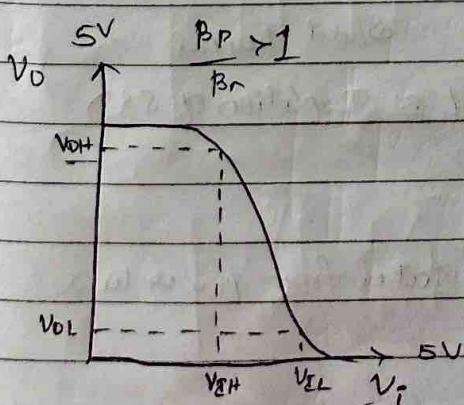
DepletionInversion-

$$\Psi_S = 2\Psi_B$$

Noise Margin

Output logic high	V_{DD}	V_{TH}	V_{OL}	V_{UL}	$i/p \text{ logic high}$	$NM_H = V_{IH} - V_{OL}$
Output logic low					$i/p \text{ logic low}$	$NM_L = V_{IL} - V_{UL}$

$V_{IH} = \text{Min high i/p vtg}$
 $V_{OL} = \text{Min high o/l vtg}$
 $V_{UL} = \text{Max low o/l vtg}$
 $V_{IL} = \text{Max low i/p vtg}$



- To determine allowable noise voltage on the input of the gate so that the O/P of the gate is not corrupted

Noise margin (M): M is defined as the difference b/w the min η O/P vtg of the driving gate & min high i/p vtg recognizd by receiving gate.

Noise margin Low: It is defined as the difference in max & min V_{DS} recognized by receiving gate & max low output voltage produced by the driving gate.

1. Calculate NM_H & NM_L for the given values V_{OH} = 2.4V V_{OL} = 0.4V

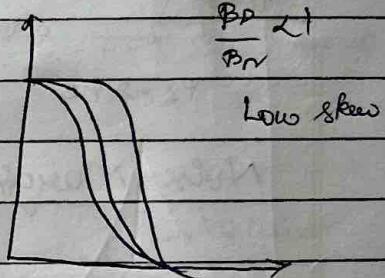
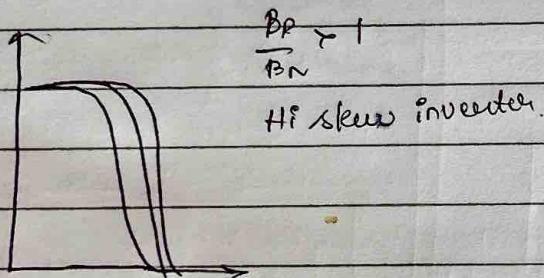
$$V_{DH} = 2.0V \quad V_{DL} = 0.8V$$

$$\rightarrow NM_H = V_{OH} - V_{DH} = 2.4V - 1.2V = 1.2V$$

$$NM_L = V_{DL} - V_{OL}$$

$$= 0.8V - 0.4V$$

$$= \underline{0.4V}$$



$$B = \frac{\mu C_o W}{L}$$

Non ideal I-V characteristics / Second Order effects / Short channel effects :-

Long channel

- Length of the channel is more than the depletion S & D

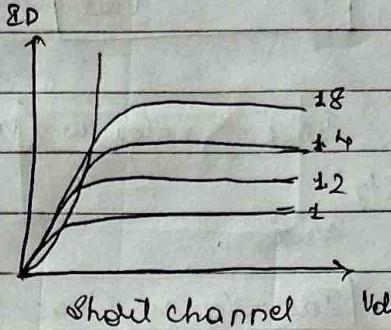
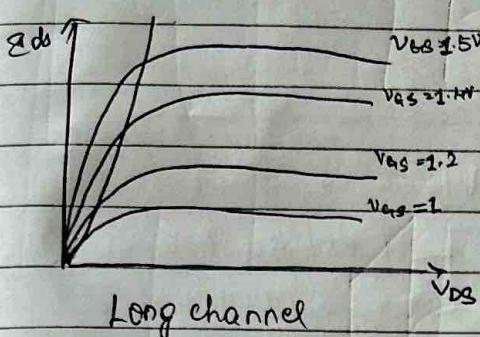
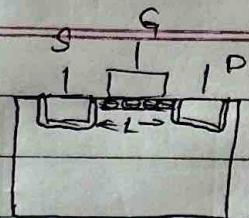
- Follows power law

$$I_D = \frac{B}{2} (V_{GS} - V_t)^2$$

Short channel

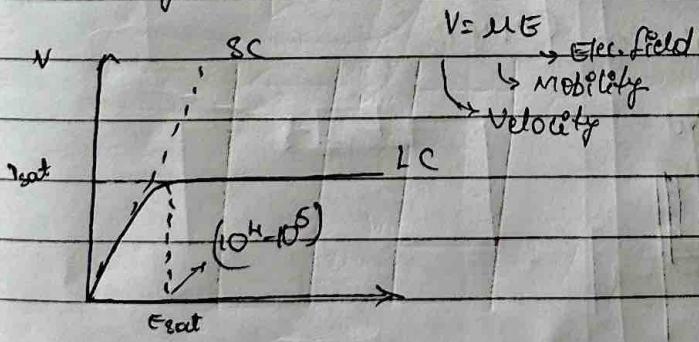
- $L \approx$ Depletion of S & D

- Deviates from power law



1. Velocity saturation & mobility degradation
2. Channel length modulation (CLM)
3. Threshold voltage \rightarrow Body effect, DTBL \rightarrow Drain Induced Barrier Lowering
4. Leakage - Gate leakage, Tunnel leakage
5. Temperature dependence
6. Geometric dependence

Velocity Saturation:-



In short channel,
when V_{ds} is increased to greater than E_{sat} (Critical electric field), carriers
starts colliding with each other which reduces the drift
velocity & in turn reduces E_{sat}

\rightarrow Mobility degradation

when we keep on applying gate voltage, scattering of carriers
happens which in turn decreases E_{sat}

$$V_{sat} = m E_{sat}$$

$$\boxed{V = \frac{m E_{sat}}{1 + \frac{E_{sat}}{E_{sat}}}}$$

$$I_{dsat} = m C_o x w \frac{(V_{GS} - V_t)^2}{L}$$

Velocity

$$V_{sat}$$

$$\boxed{I_{ds} = C_o x w (V_{GS} - V_t) V_{sat}}$$

$$I_{ds} = 0 \text{ cutoff } V_{GS} < V_t$$

$$I_{dsat} \propto I_{ds} \frac{V_d}{V_{sat}} \rightarrow \text{linear } V_{GS} > V_t$$

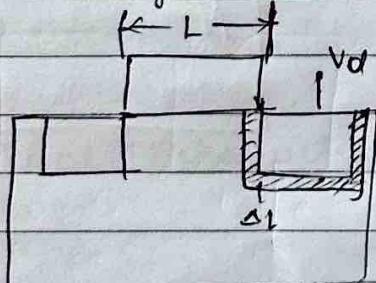
$$I_{dsat} = I_{ds} \text{ saturation } V_{GS} > V_t$$

$$I_{dsat} = P_c \frac{B}{2} (V_{GS} - V_t)^2$$

$$V_{dsat} = P_v (V_{GS} - V_t)^{1/2}$$

\times → Velocity Saturation Index

2 Channel Length modulation (CLM)



$$L_{eff} = L - \Delta L$$

$$V_{dsb} \approx V_{ds}$$

1.0.2.2.

$$I_{ds} = \frac{B}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{ds})$$

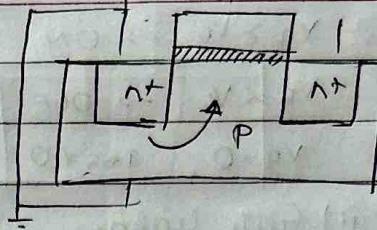
$I_{ds} \uparrow L \downarrow$

$$= 20mA$$

$\lambda \rightarrow$ Channel Length modⁿ factor

3. Threshold voltage effects:

(i) Body effect



$$V_t = V_{to} + \gamma (\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$$

where

V_{sb} → Source to body voltage

ϕ_s → Surface potential

γ → body effect co-efficient $0.4e - 1/V^{1/2}$

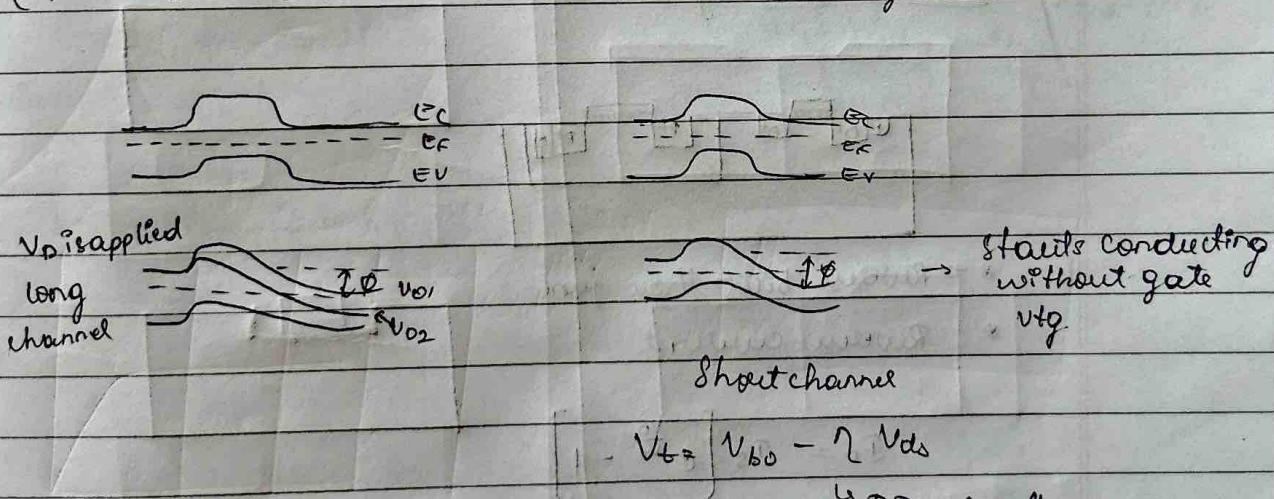
V_{to} → Threshold voltage with body effect

$$\phi_s = \frac{2VT \ln \frac{N_A}{n_i}}{n_i} \quad | \quad N_A \rightarrow \text{Doping conc.}$$

$n_i \rightarrow \text{Intrinsic conc.}$

$$\gamma = \frac{4\pi \sqrt{2\epsilon_s \epsilon_0 N_A}}{E_{on}}$$

(ii) DIBBL: Drain Induced Barrier Lowering



4.

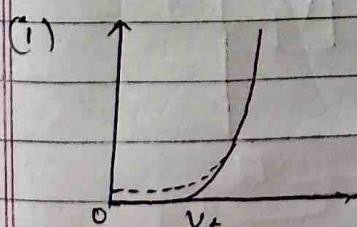
Leakage:-

(i) Subthreshold leakage → D & S

(ii) Gate leakage → gate & body

(iii) Junction leakage → D & S

↳ DIBBL co-off



Advantage

* DRAM

It happens due to

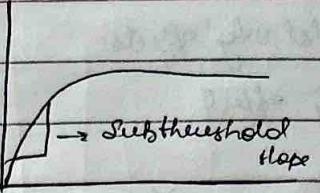
DIBBL & GIDL

DESI:-

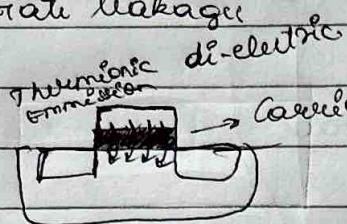
$$V_g > V_t \rightarrow ON$$

$$V_g < V_t \rightarrow OFF$$

$$V_g = 0, I_{DS} \neq 0$$



(ii) Gate leakage



Gate punch through
&
substrate

V_g Fowler-Nordheim

- FN punch through \rightarrow High & Moderate V_g
- Direct punch through \rightarrow Low V_g

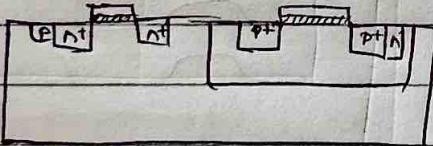
How to improve!

$$V_t = t_{ox} r - [9\text{ Å}]$$

$\text{SiO}_2 \xrightarrow{3.9} \uparrow \epsilon_{ox}$

1. High k materials
2. Silicon nitride

(iii) Junction leakage :-



- * \rightarrow Reverse bias these junc
- * Reverse current

$$I_D = I_S \left[e^{\frac{V_D}{V_T}} - 1 \right]$$

$I_S \rightarrow$ Depends on doping

$V_D \rightarrow$ Diode V_{tg}

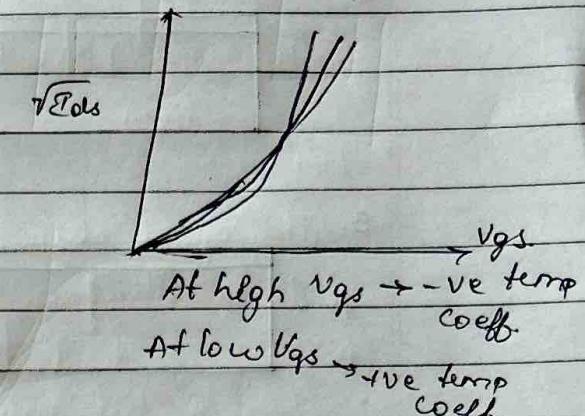
Temperature dependence :-

$$n(t) = n(T_0) \left[\frac{T}{T_0} \right]^{-k_f}$$

T - absolute temperature

T_0 → Room temp

k_f → Fitting parameter



$$V_t(T) = V_t(T_0) - k_{vt} (T - T_0)$$

$$k_{vt} \approx 0.5 \text{ to } 3 \text{ mV/K}$$

X } OFF → high current
ON → low current

Geometry dependence :-

• Happens during fabrication.

Pentavalent gas



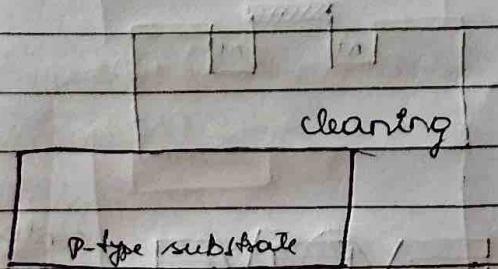
$$L_{eff} = L_{drawn} + x_L - 2L_D - \text{diffusion}$$

through bulk

$$W_{eff} = w_{drawn} + x_w - 2w_D - \text{diffusion}$$

through bulk

Unit-1 → Fabrication



clear Room:

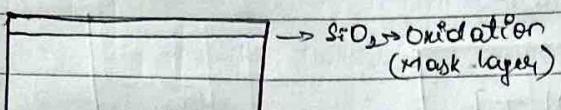
- class 100 → No. of particles per unit area
- class 10
- class 1

RCA1 → remove oxides

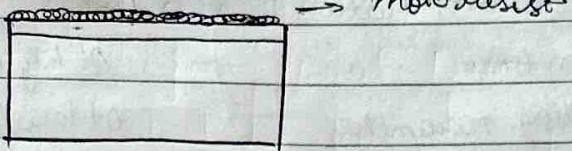
RCA2 → remove polymers

Pighana → $H_2O_2 + H_2SO_4$

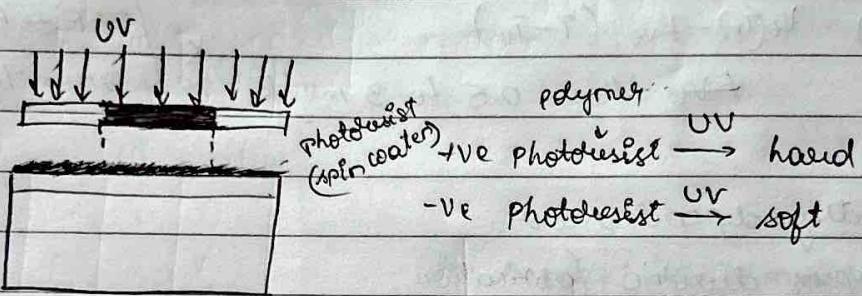
2.



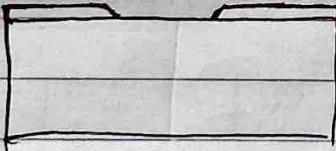
3.



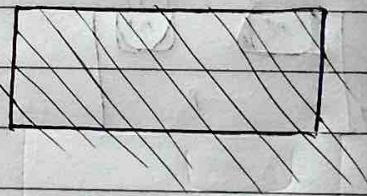
4.



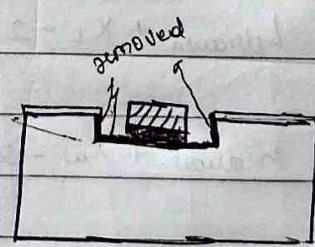
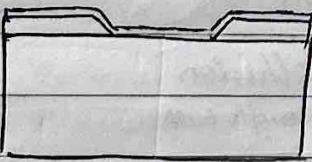
5. Developer soln :- HF



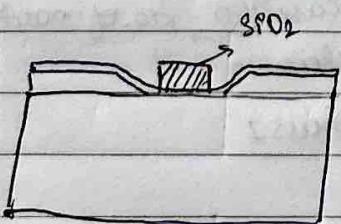
8.



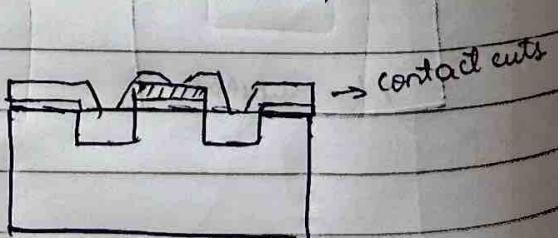
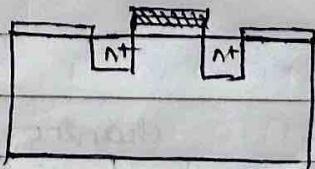
6.



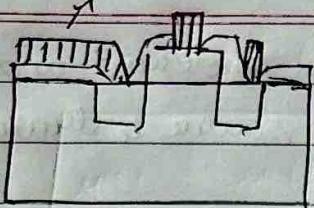
7. Pattern the gate



9.



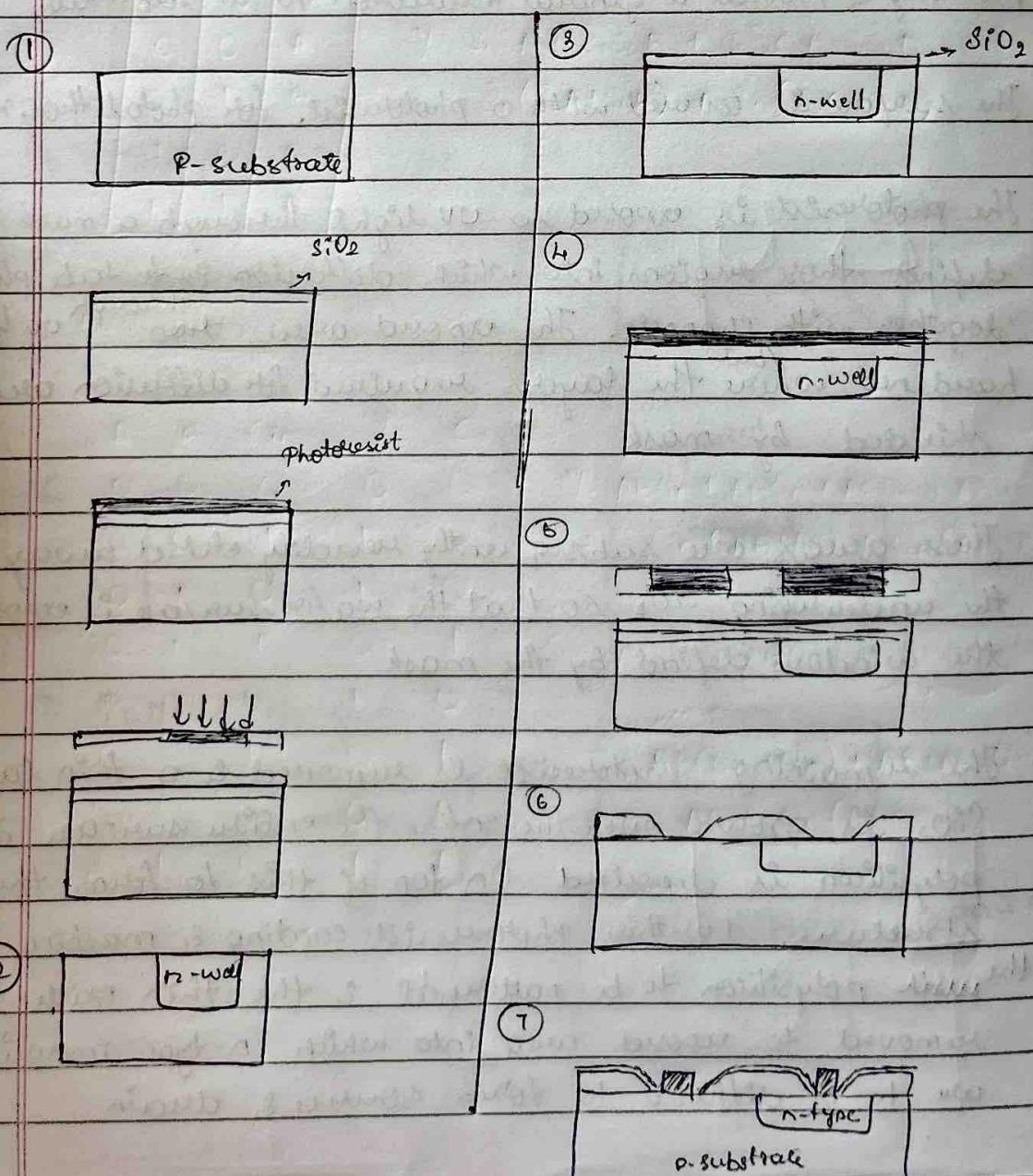
Metal



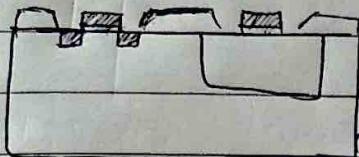
- Processing is carried out in thin wafers cut from a single crystal of silicon of high purity into which the required are introduced as the crystal is grown. The wafer is cleaned with RCA1, RCA2 and piranha soln.
- A layer of SiO_2 is grown all over the surface of the wafer to protect the surface, which acts as a barrier b/w during processing & provide a general insulation to the substrate.
- The surface is covered with a photoresist, for photolithography
- The photoresist is exposed to UV light through a mask which defines those regions into which diffusion is to take place together with channels. The exposed areas ^{through} _{but} UV light are hardened where the layers required for diffusion are shielded by mask
- These areas are subsequently readily etched away with the underlying SiO_2 so that the wafer surface is exposed in the windows defined by the mask
- The remaining photoresist is removed & a thin layer of SiO_2 is grown over the entire the entire surface. Then polysilicon is deposited on top of this to form the gate structure. Further, photoresist coating & masking along allows the polysilicon to be patterned & the thin oxide is removed to exposed area into which n-type impurities are to be diffused to form source & drain

- SiO_2 is grown & is masked with photoresist and then etched to expose selected areas of gate, source & drain where connections
- The whole chip then has metal deposited over its surface to a thickness typical 1μm.
- This metal layer is then masked & etched to form the μm^2 interconnection pattern.

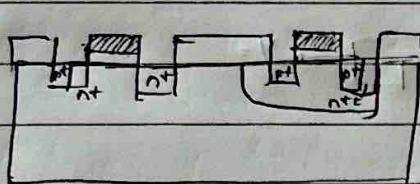
CMOS Fabrication:



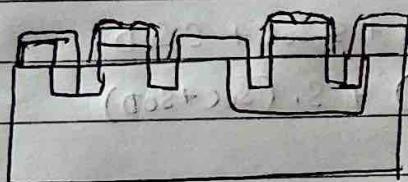
(8)

 N^+ diffusion

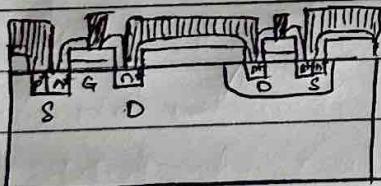
(9)



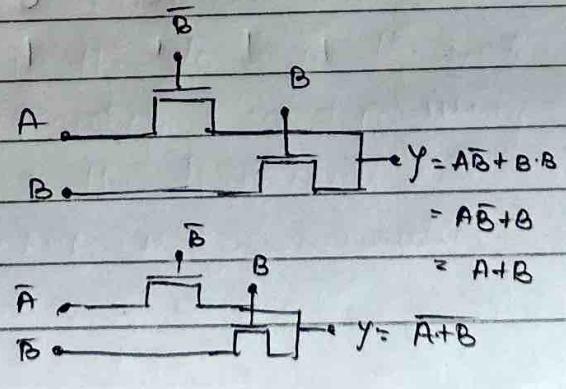
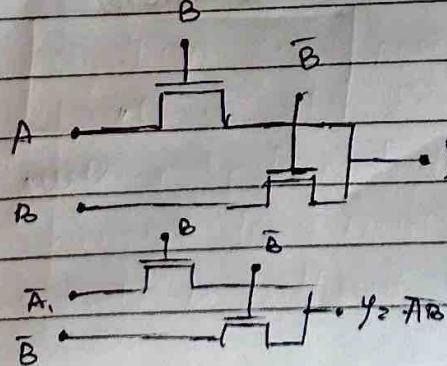
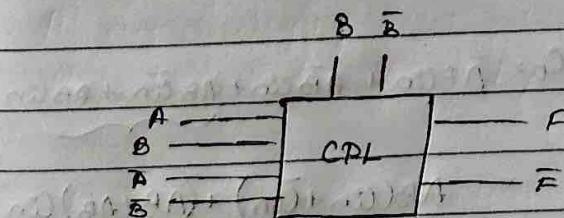
(10) Contact cuts.



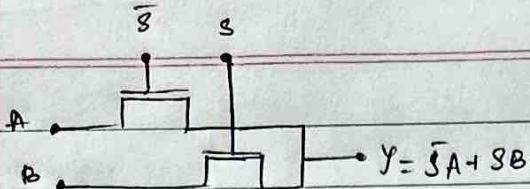
(11) Metallization



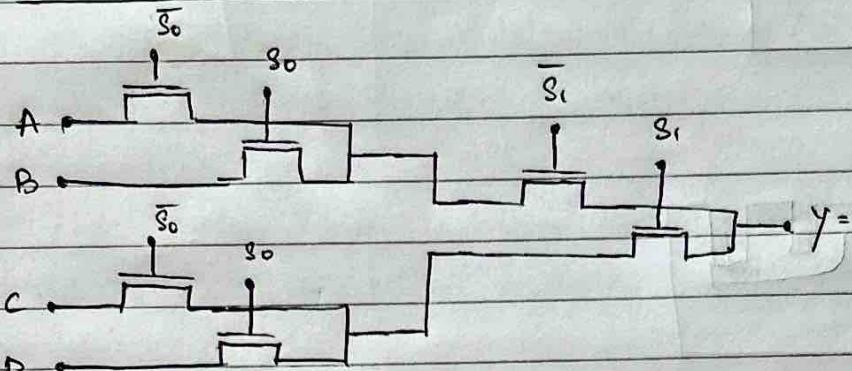
CPL : Complementary Pass Transistor logic

 $B \bar{B}$ 

2:1 MUX



4:1 MUX :-



S ₁	S ₀	Y
0	0	A
0	1	B
1	0	C
1	1	D

$$Y_1 = \bar{S}_1 \bar{S}_0 A + \bar{S}_1 S_0 B + S_1 \bar{S}_0 C + S_1 S_0 D$$

$$= \bar{S}_1 (\bar{S}_0 A + S_0 B) + S_1 (\bar{S}_0 C + S_0 D)$$

Full adder :-

A	B	Cin	Y	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$Y = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + AB\bar{C}_{in}$$

$$= C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

$$C_0 = \bar{A}\bar{B}C_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + \underbrace{ABC_{in}}$$

$$= AB(C_{in} + \bar{C}_{in}) + (\bar{A}B + A\bar{B})C_{in}$$

$$= AB + C_{in}(A \oplus B)$$

