

### Experiment-5

**Aim:** a) Implement master slave based negative edge triggered flip flop using 2x1 MUX as an element designed using transmission gate.

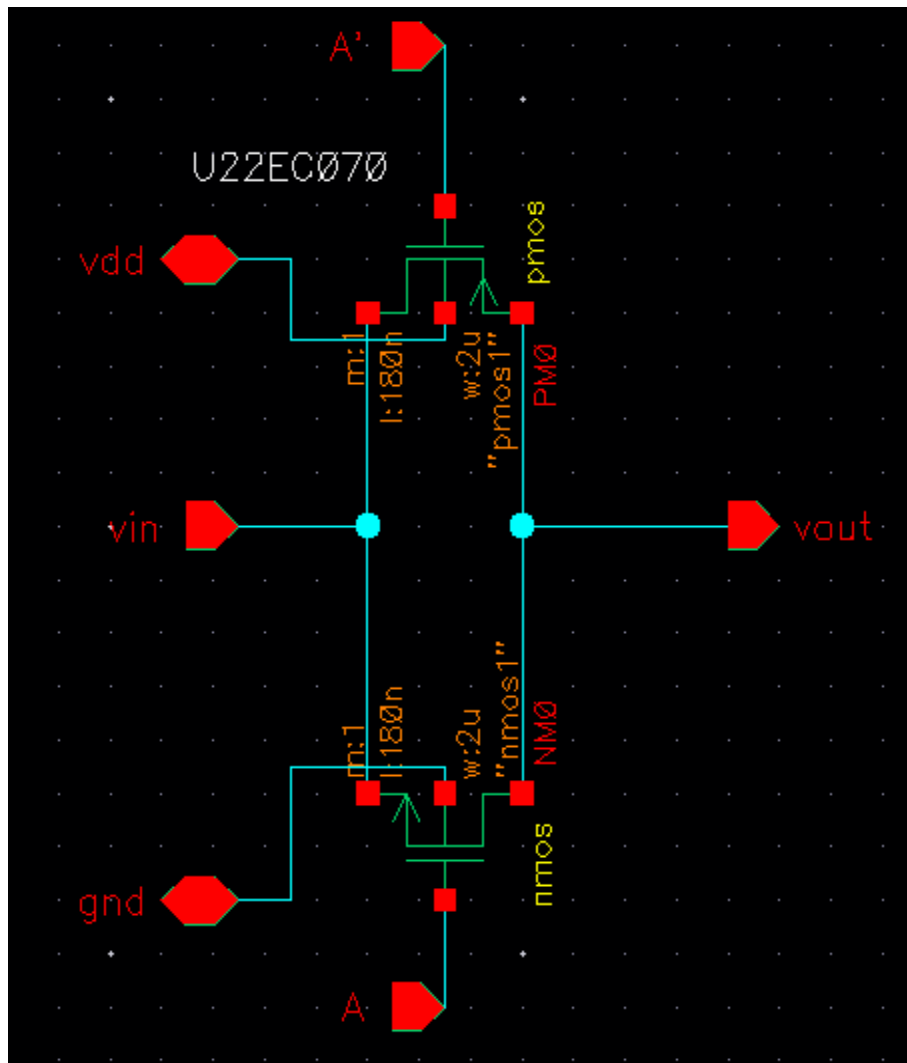
b) Implement dynamic positive edge triggered flip flop using transmission gate.

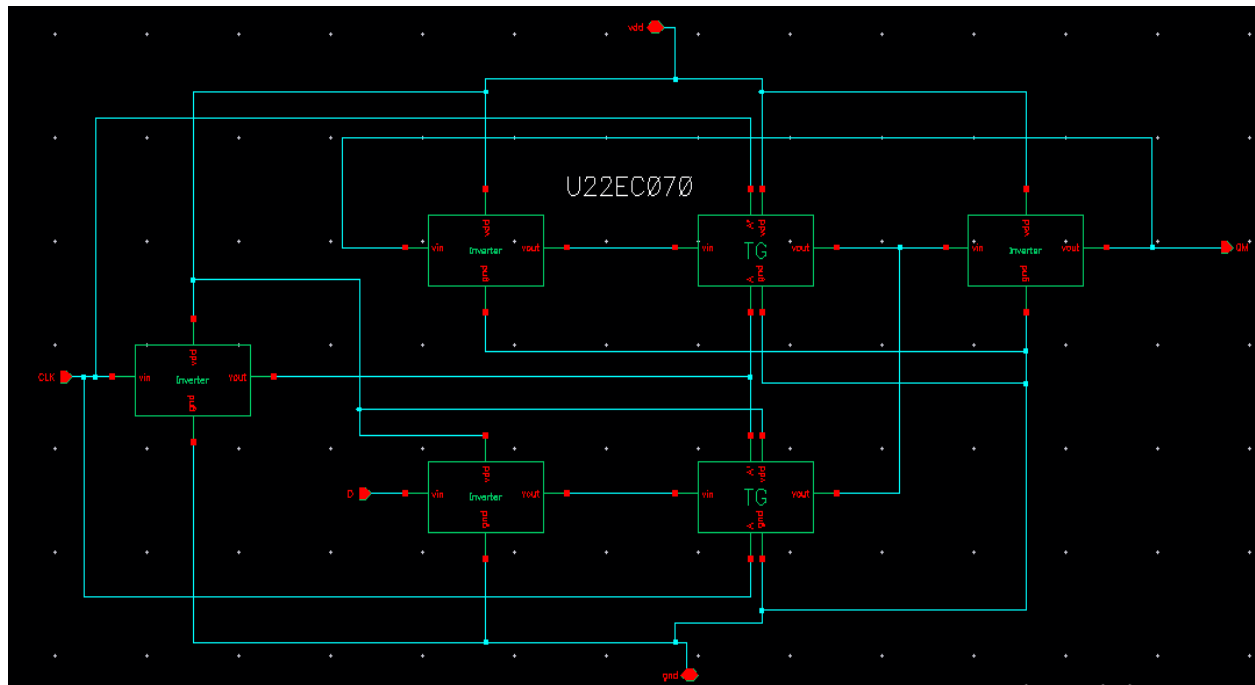
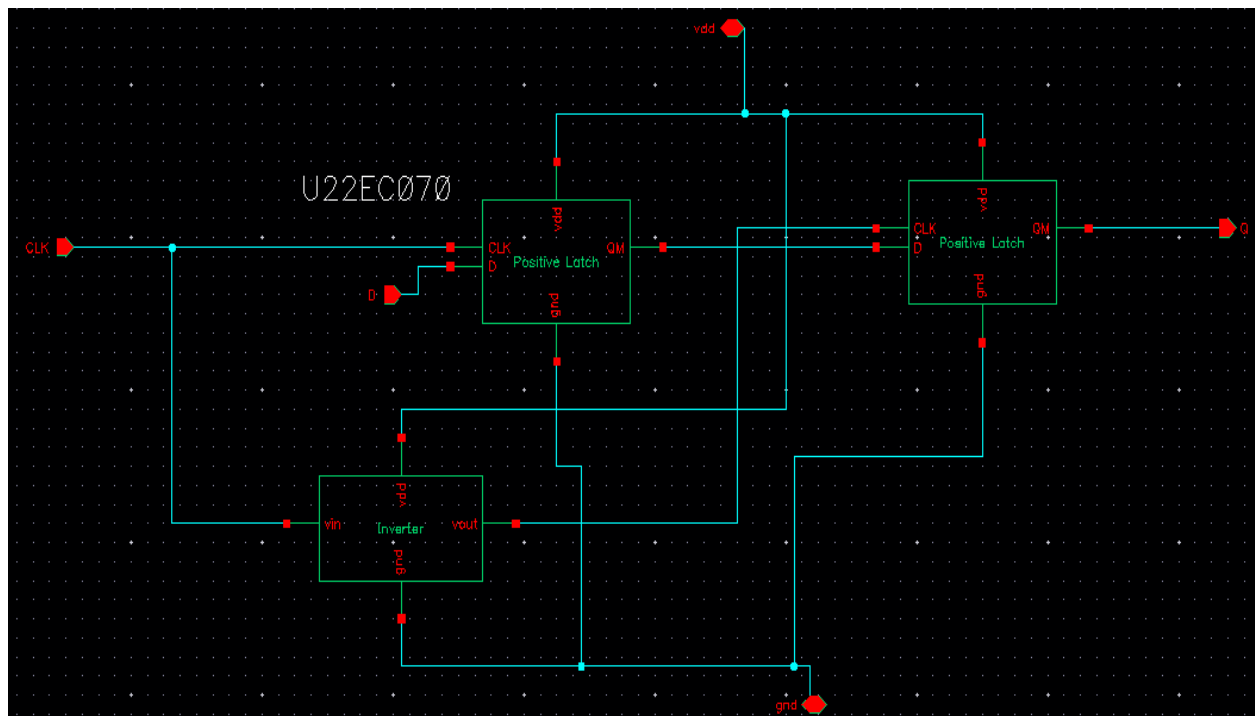
Also, do above by using two phase clock generator and compare both.

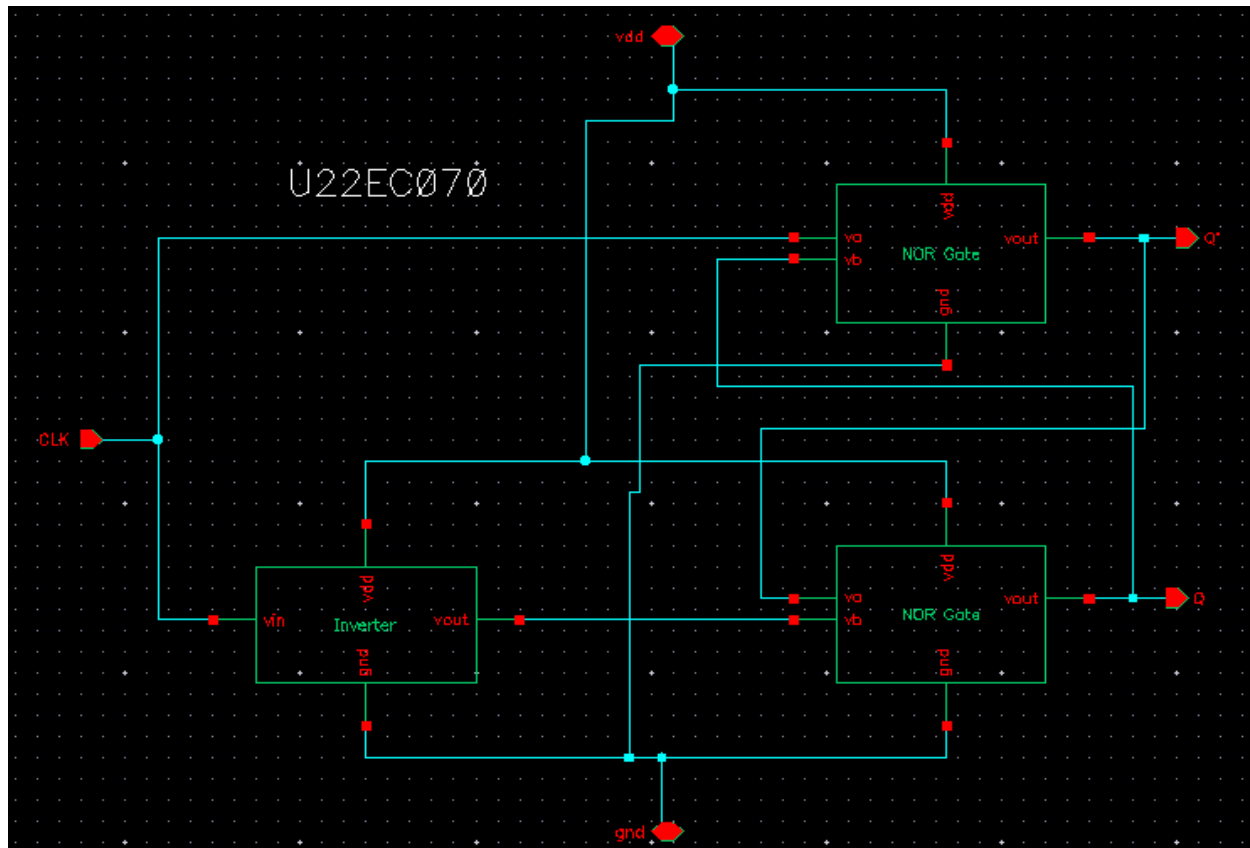
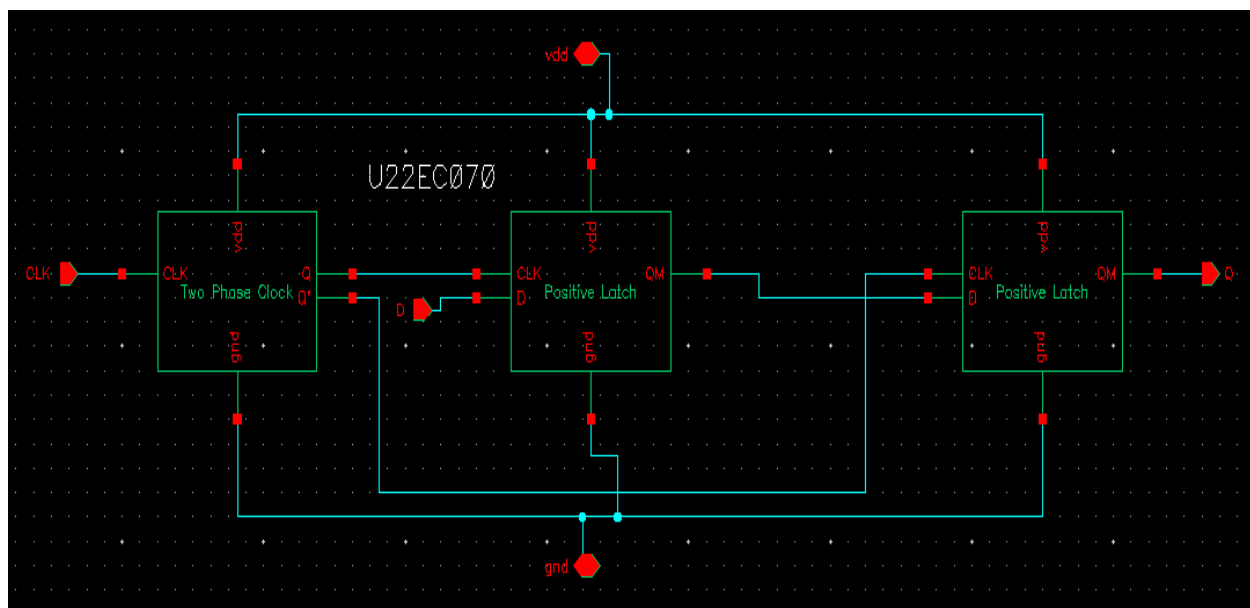
**Apparatus:** Cadence Virtuoso Software

**Schematic:**

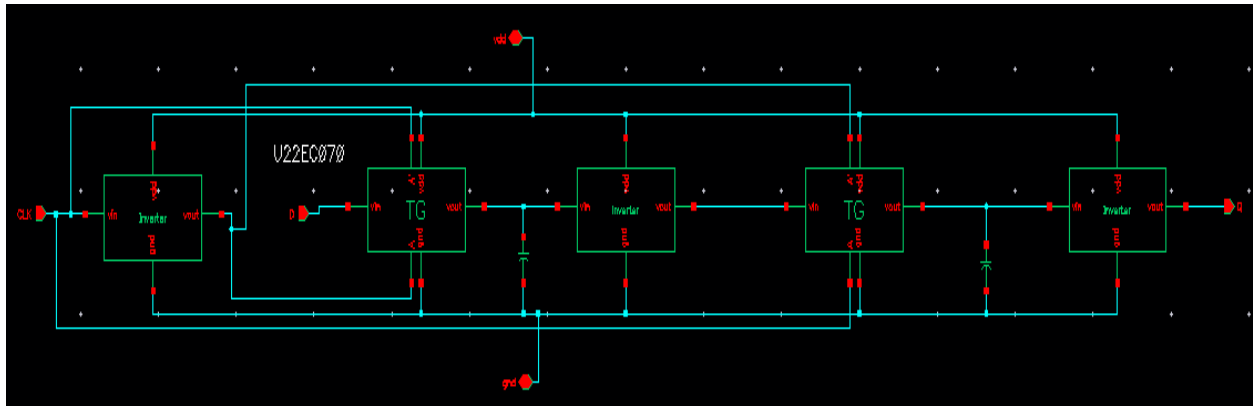
**Transmission gate schematic:**



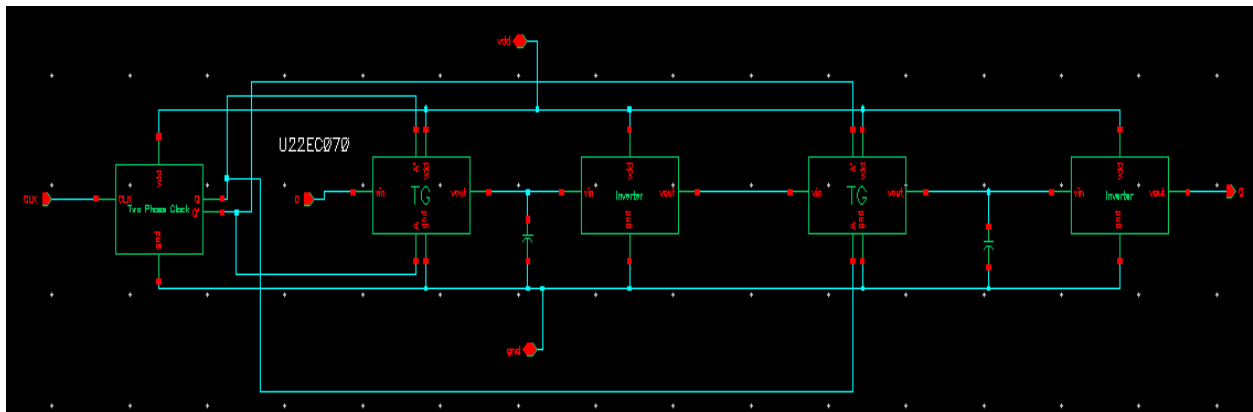
**Positive latch:****Master slave based edge triggered flip flop without using two phase clock generator:**

**Two phase clock generator:****Master slave based edge triggered flip flop using two phase clock generator:**

**Dynamic edge triggered flip flop without using two phase clock generator:**

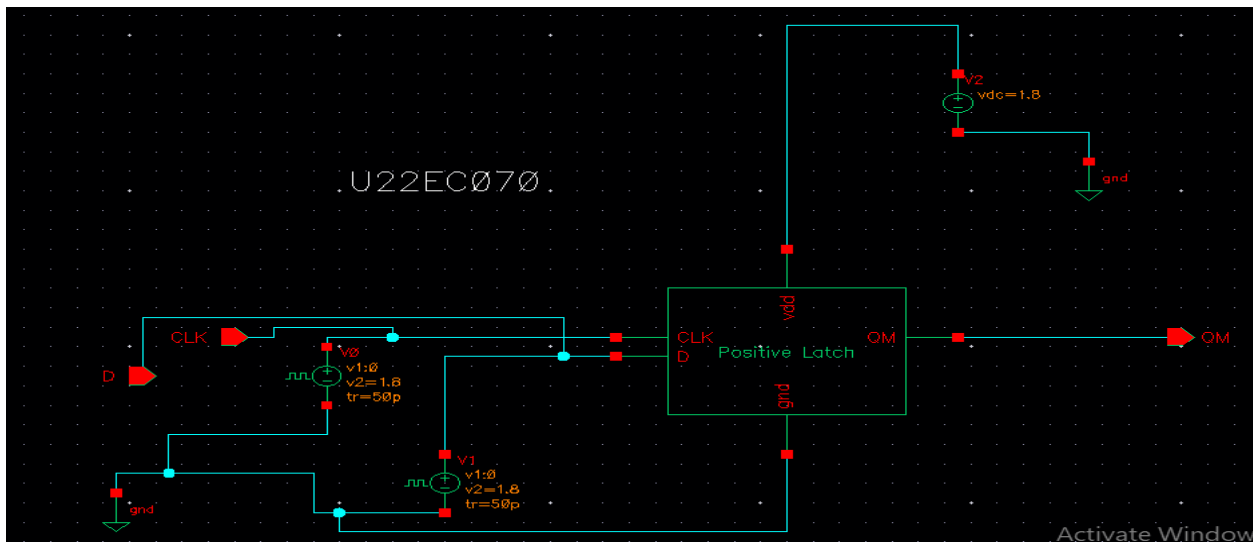


**Dynamic edge triggered flip flop using two phase clock generator:**

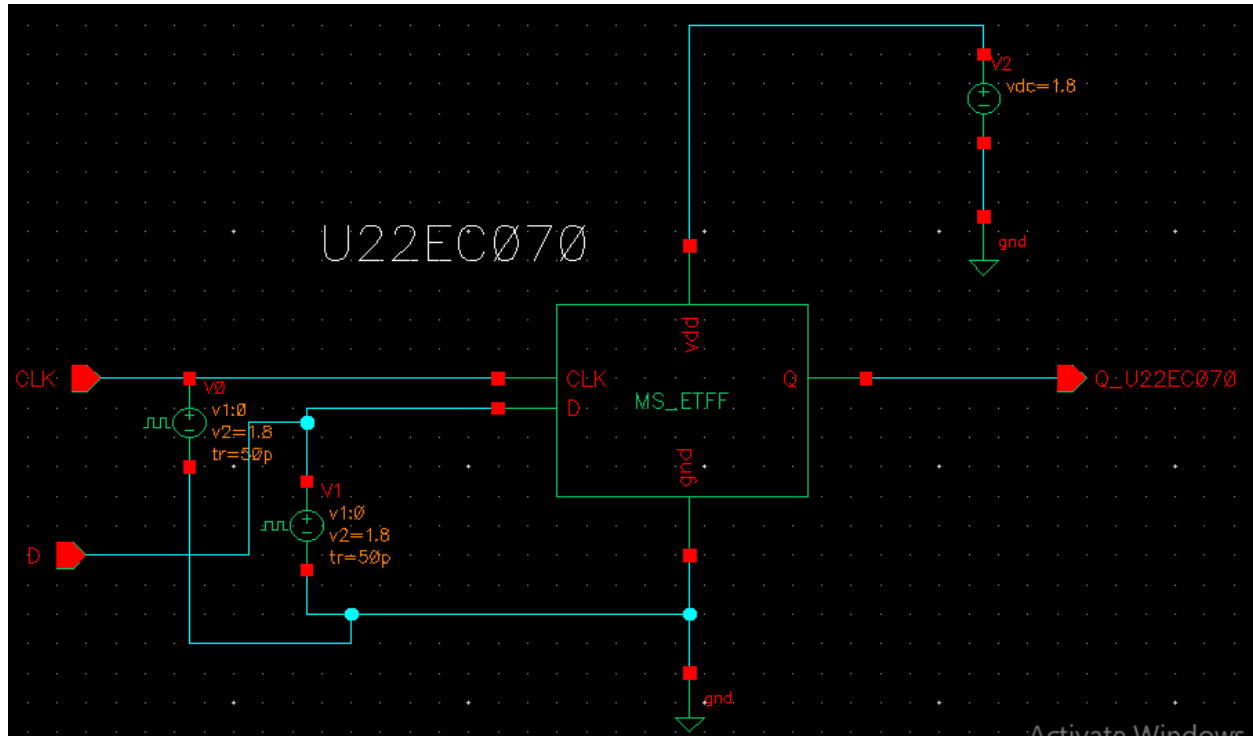


**Testbench:**

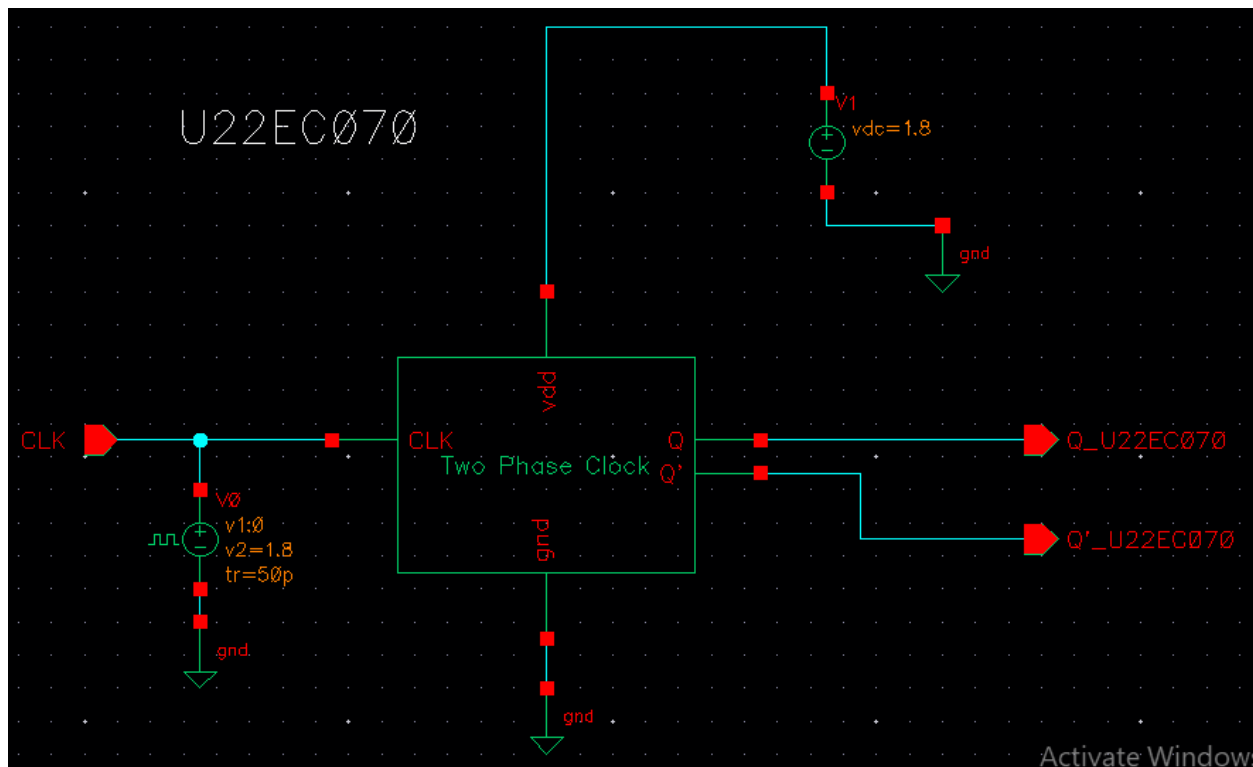
**Positive latch:**

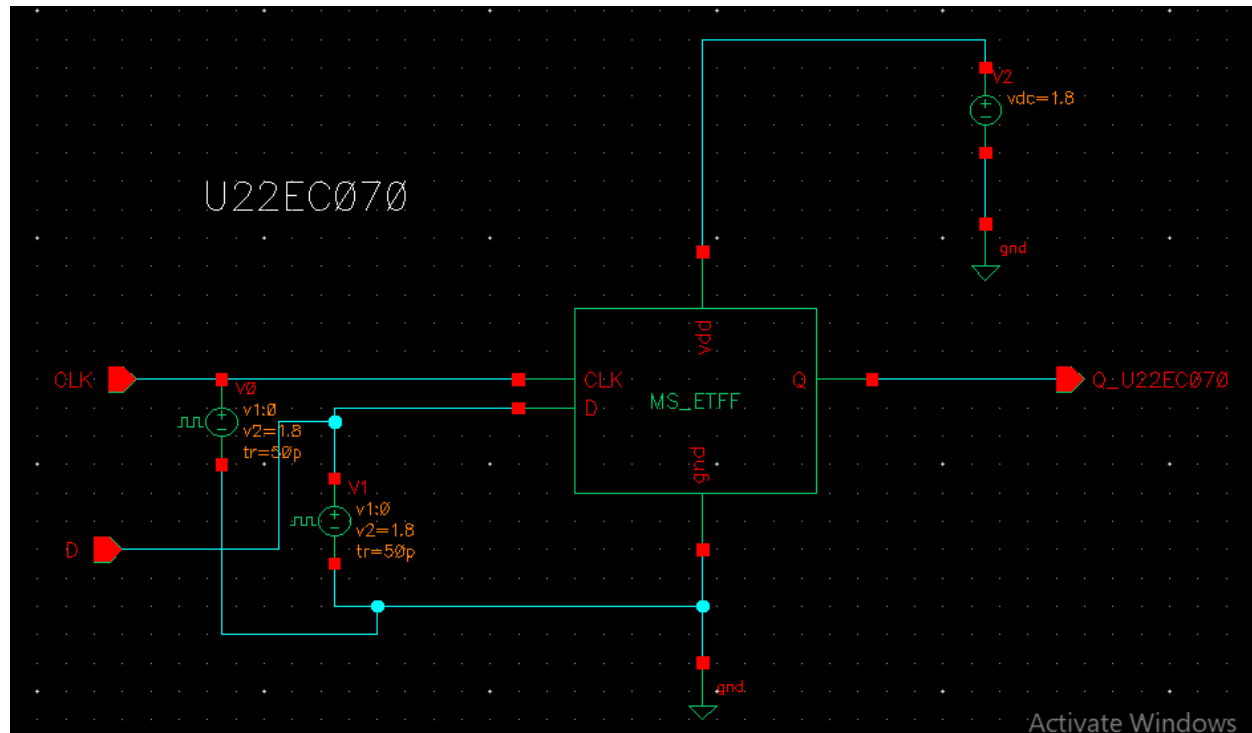
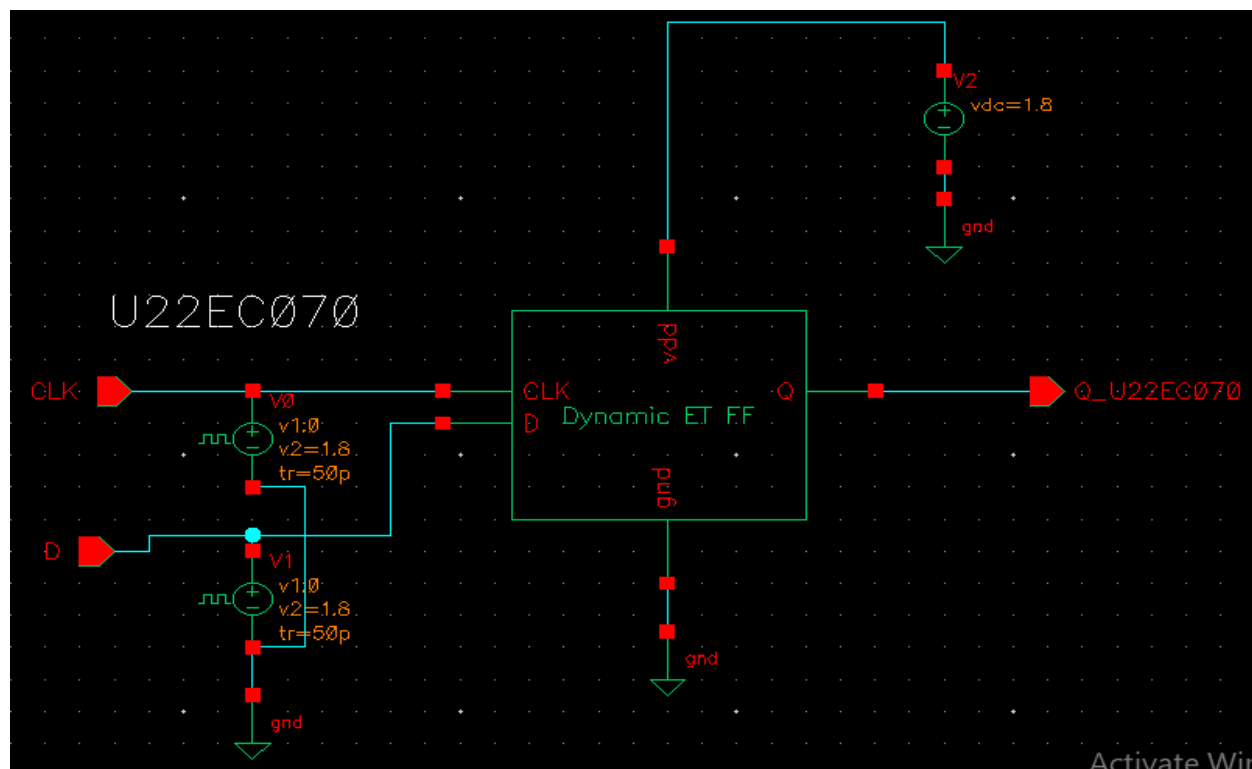


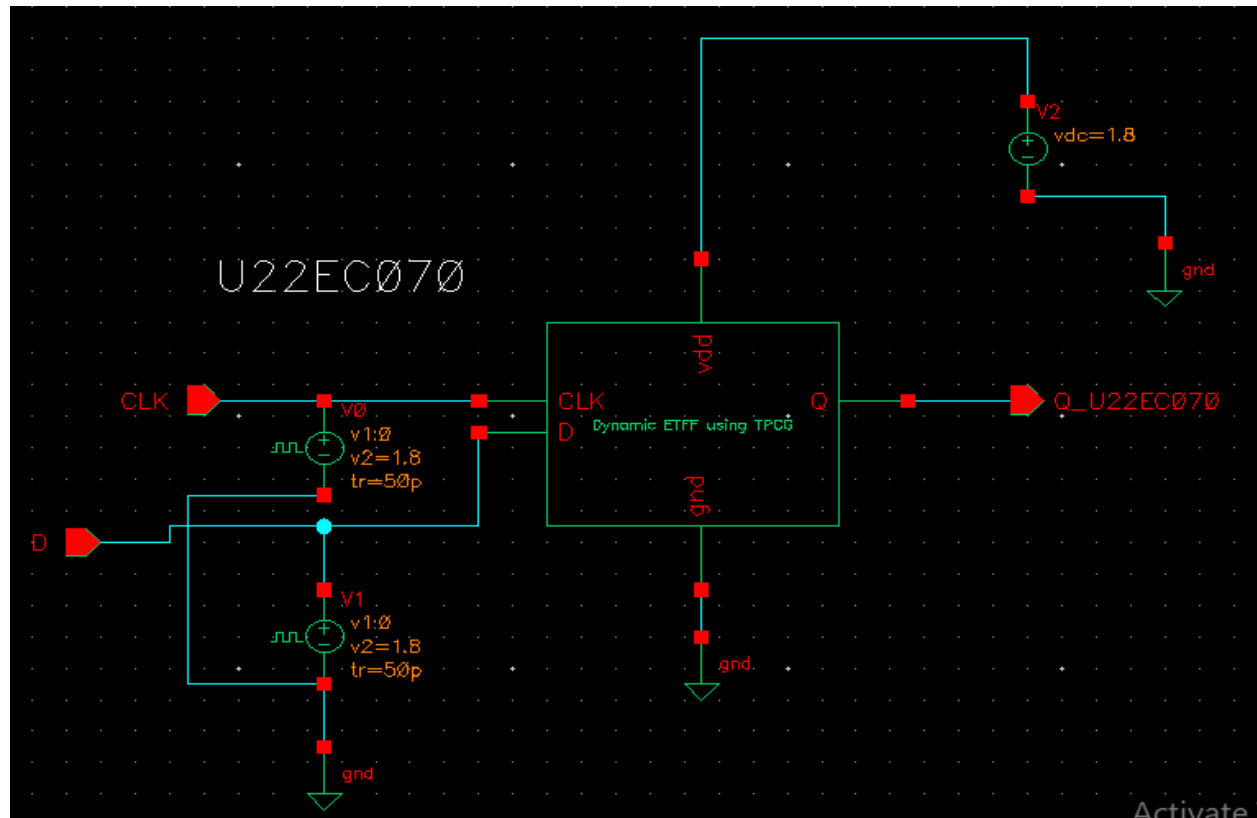
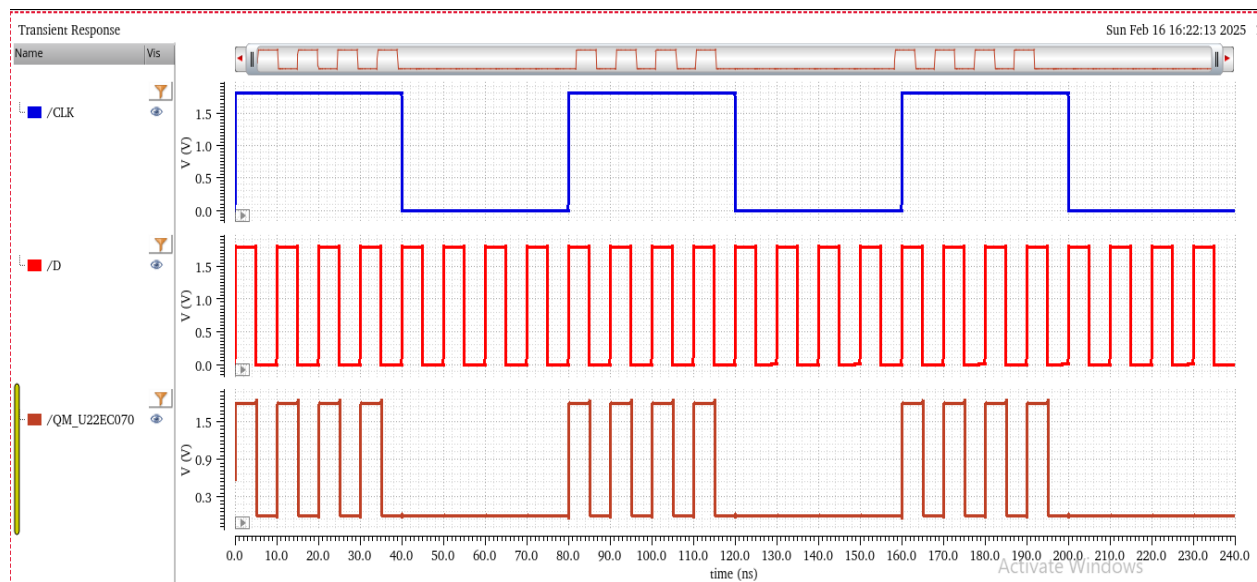
### Master slave based edge triggered flip flop without using two phase clock generator:



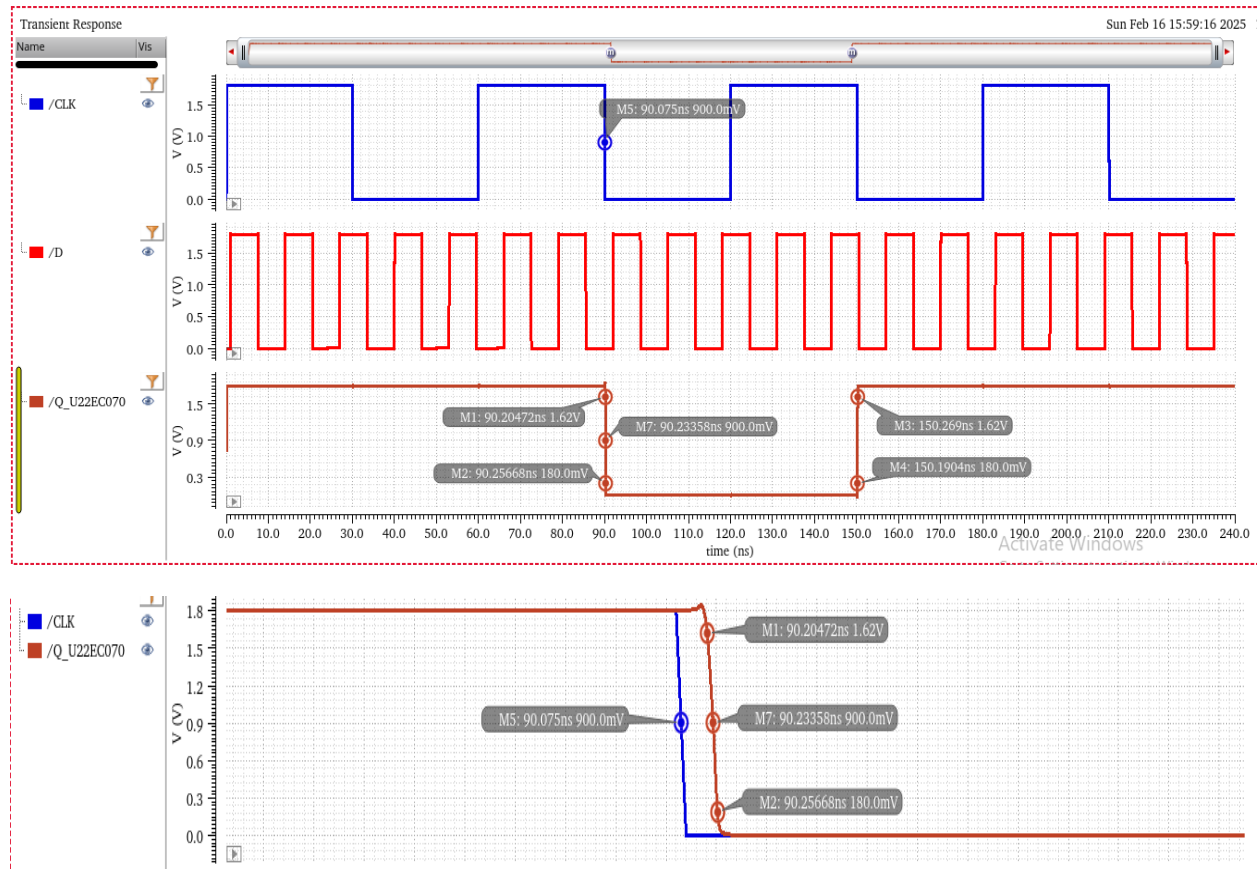
### Two phase clock generator:



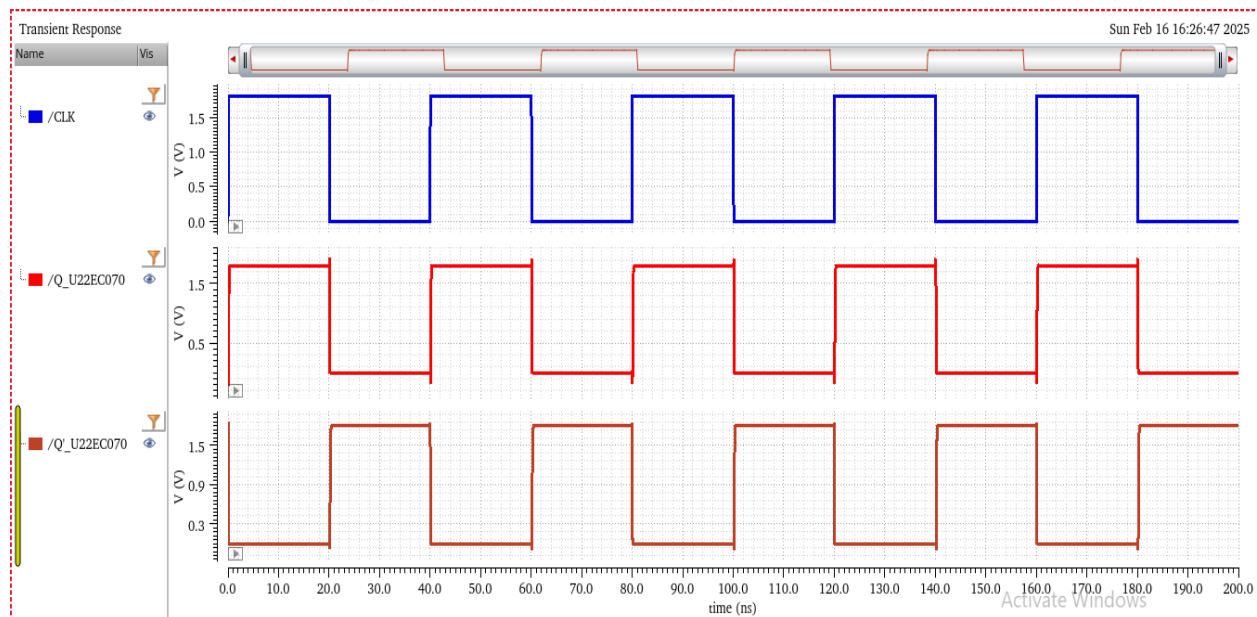
**Master slave based edge triggered flip flop using two phase clock generator:****Dynamic edge triggered flip flop without using two phase clock generator:**

**Dynamic edge triggered flip flop using two phase clock generator:****Outputs:****Positive latch:**

# Master slave based edge triggered flip flop without using two phase clock generator:

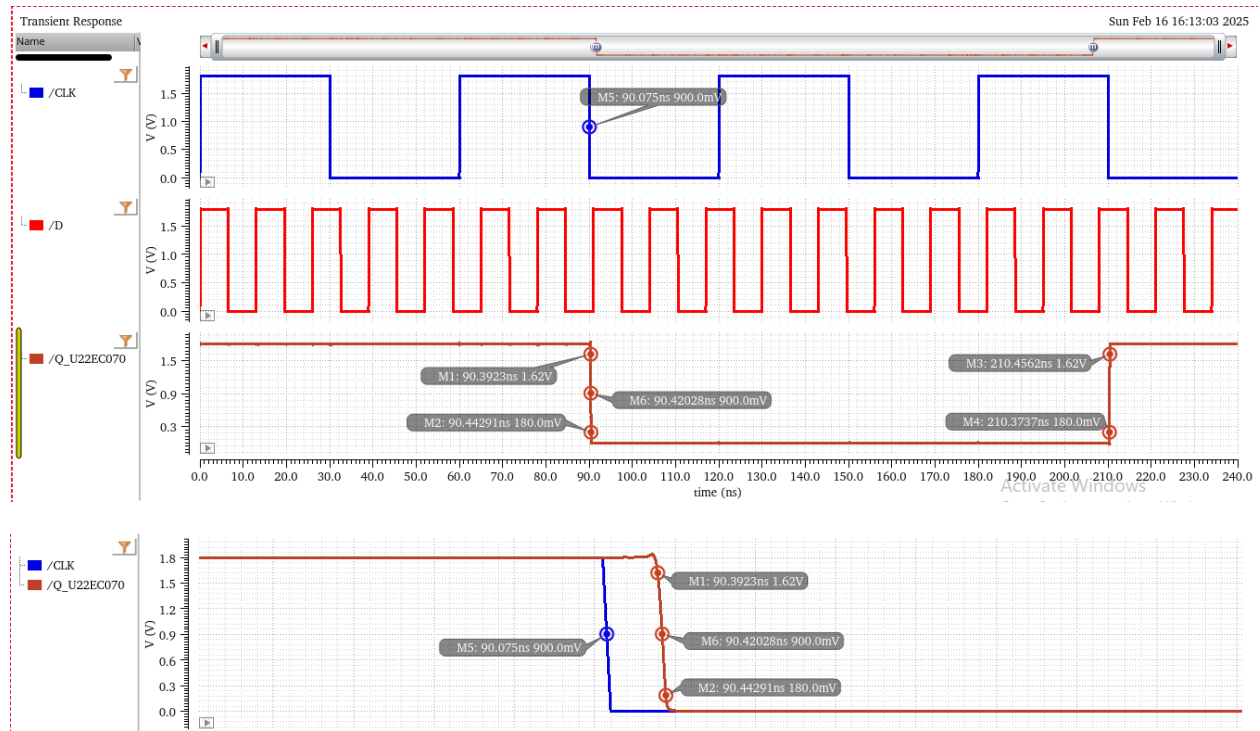


# Two phase clock generator:

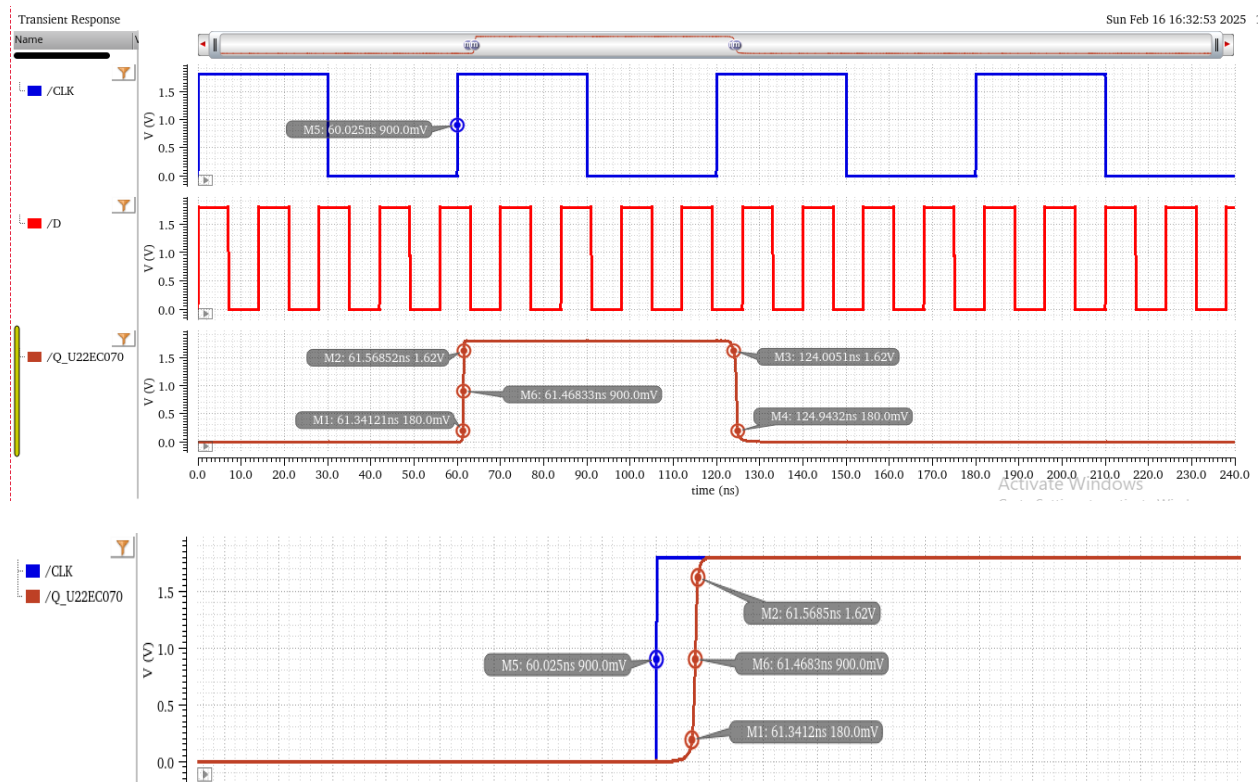




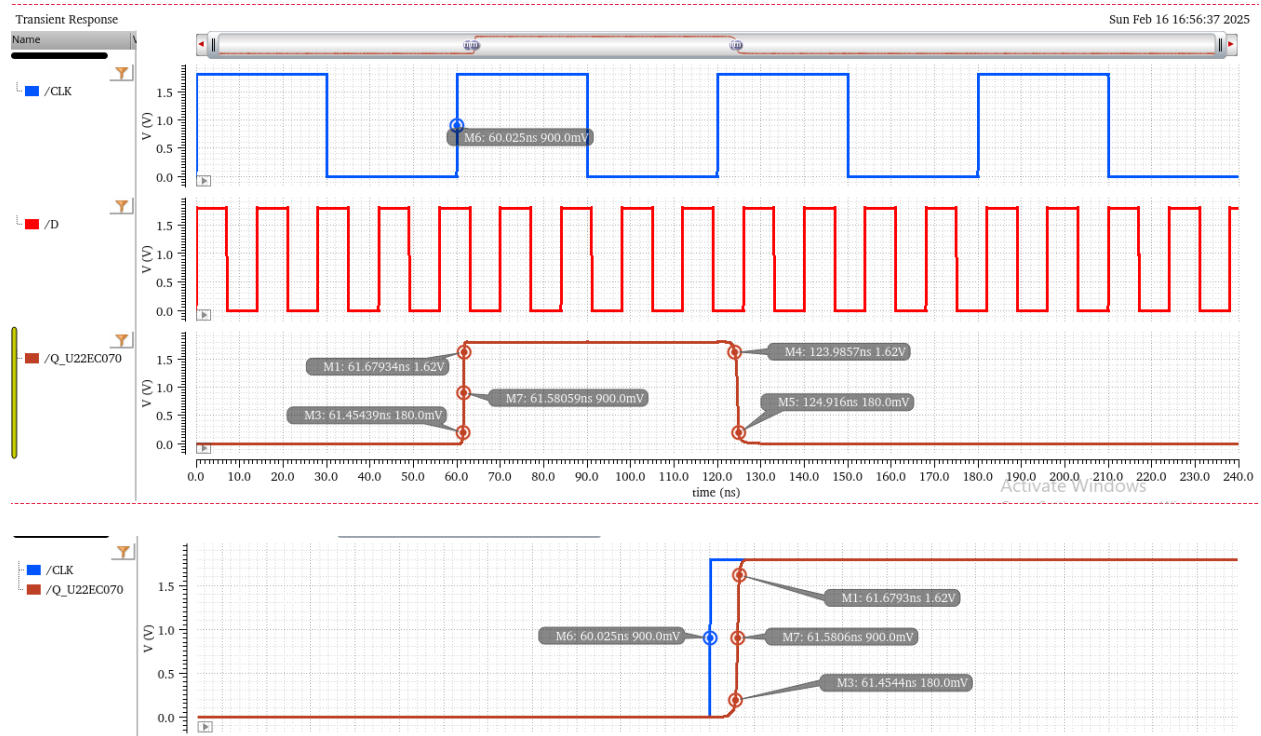
### Master slave based edge triggered flip flop using two phase clock generator:



### Dynamic edge triggered flip flop without using two phase clock generator:



# Dynamic edge triggered flip flop using two phase clock generator:



## Calculations:

## Conclusion:

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## Assignment-5

### Part-A

**Aim:** a) Implement layout of master slave based negative edge triggered flip flop using 2x1 MUX as an element designed using transmission gate.

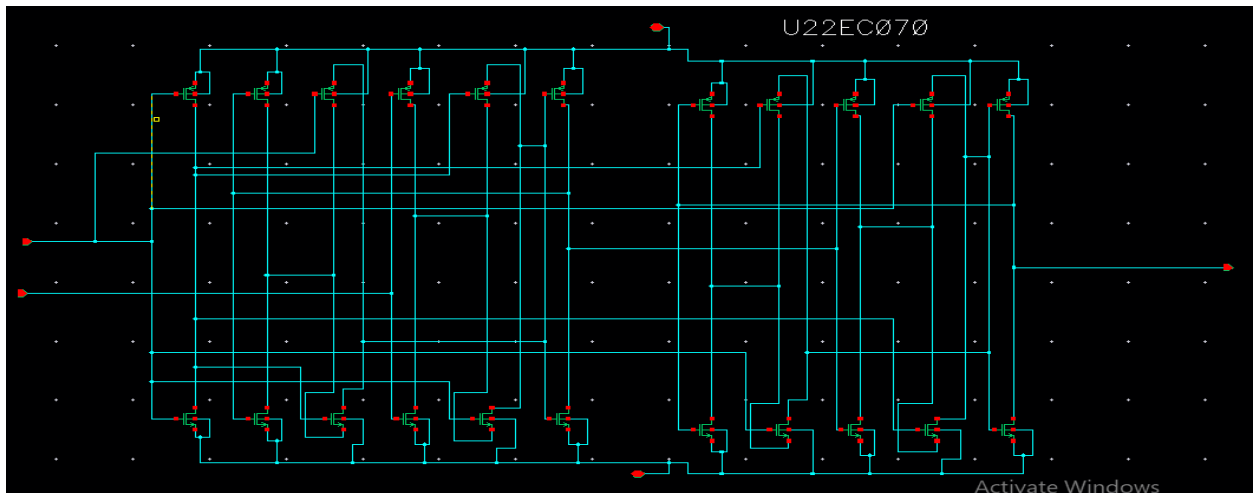
b) Implement layout of dynamic positive edge triggered flip flop using transmission gate.

Consider sea of gate structure in both part a) and b).

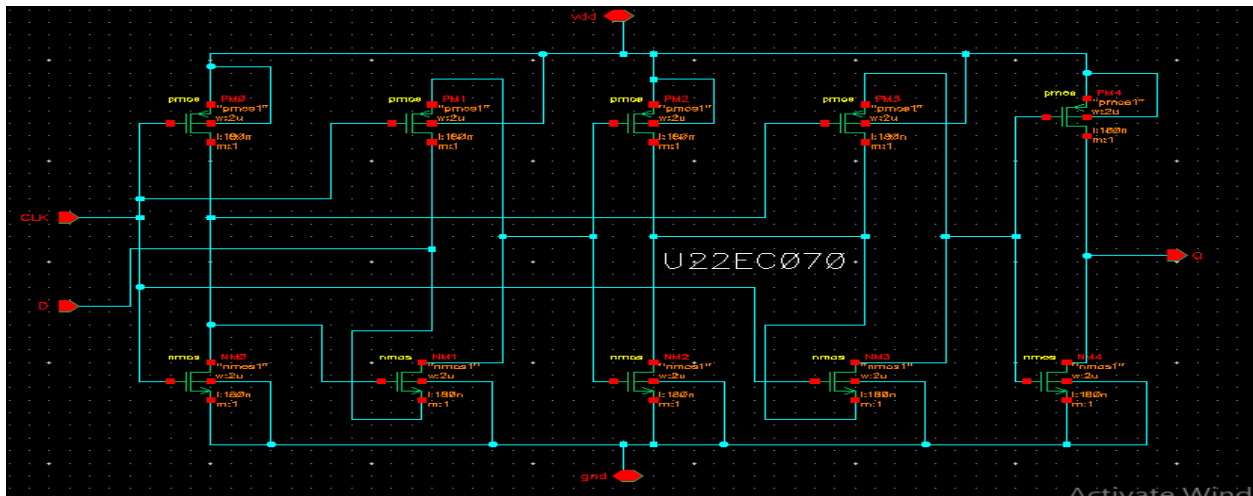
**Apparatus:** Cadence Virtuoso Software

**Schematic:**

**Master slave based negative edge triggered flip flop:**

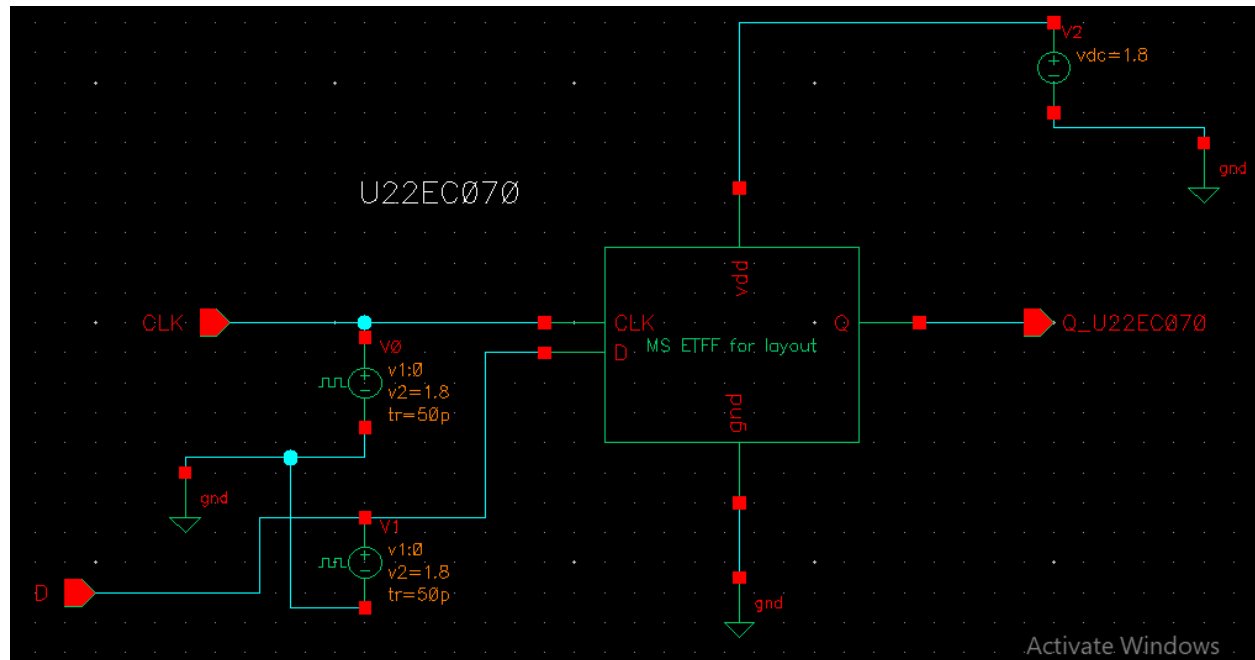


**Dynamic positive edge triggered flip flop:**

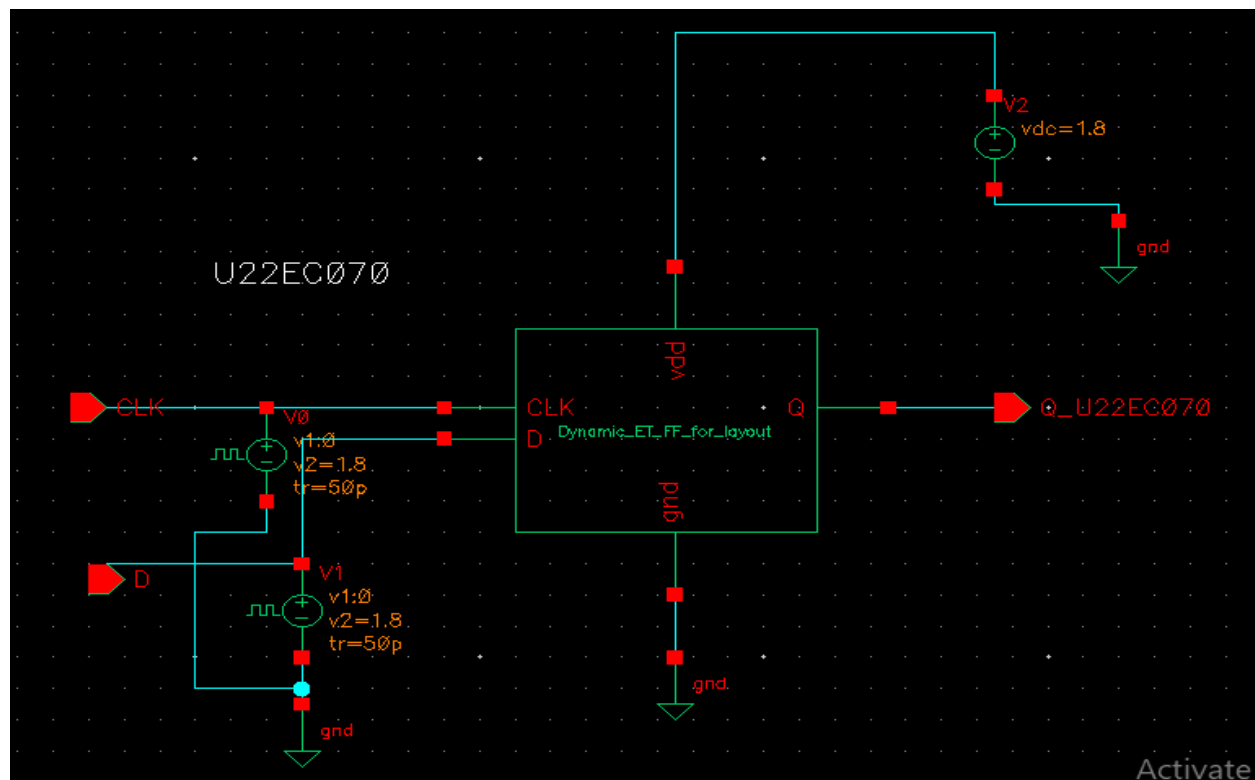


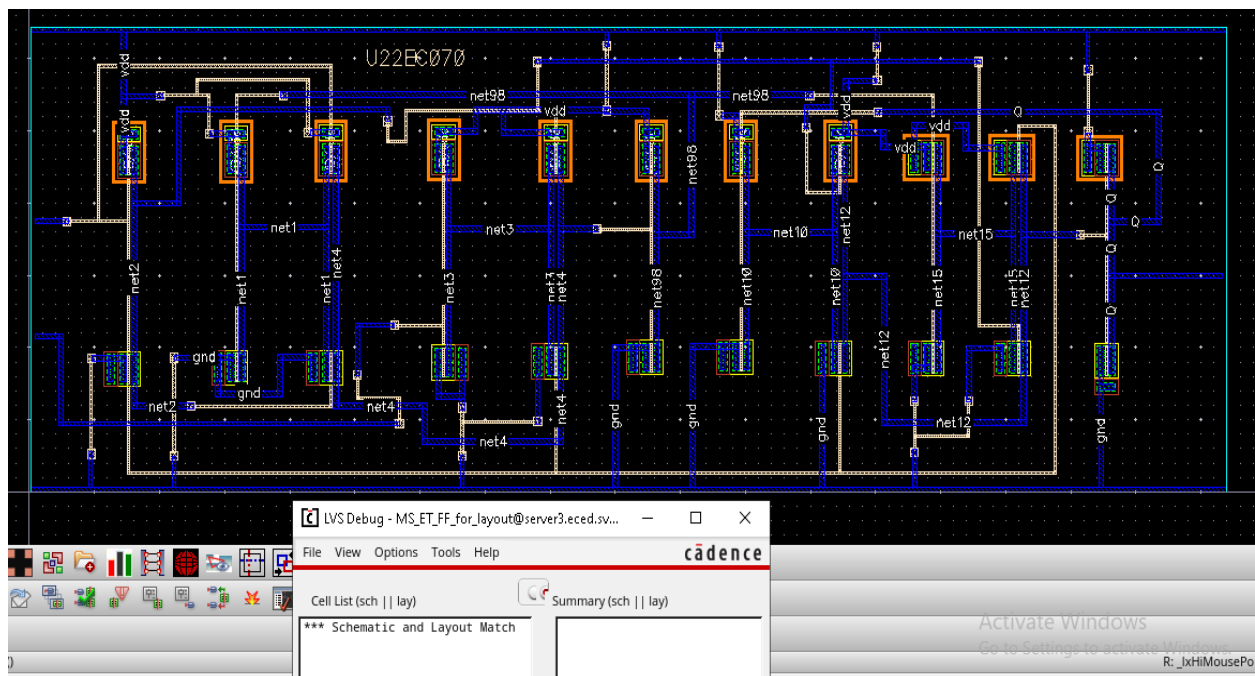
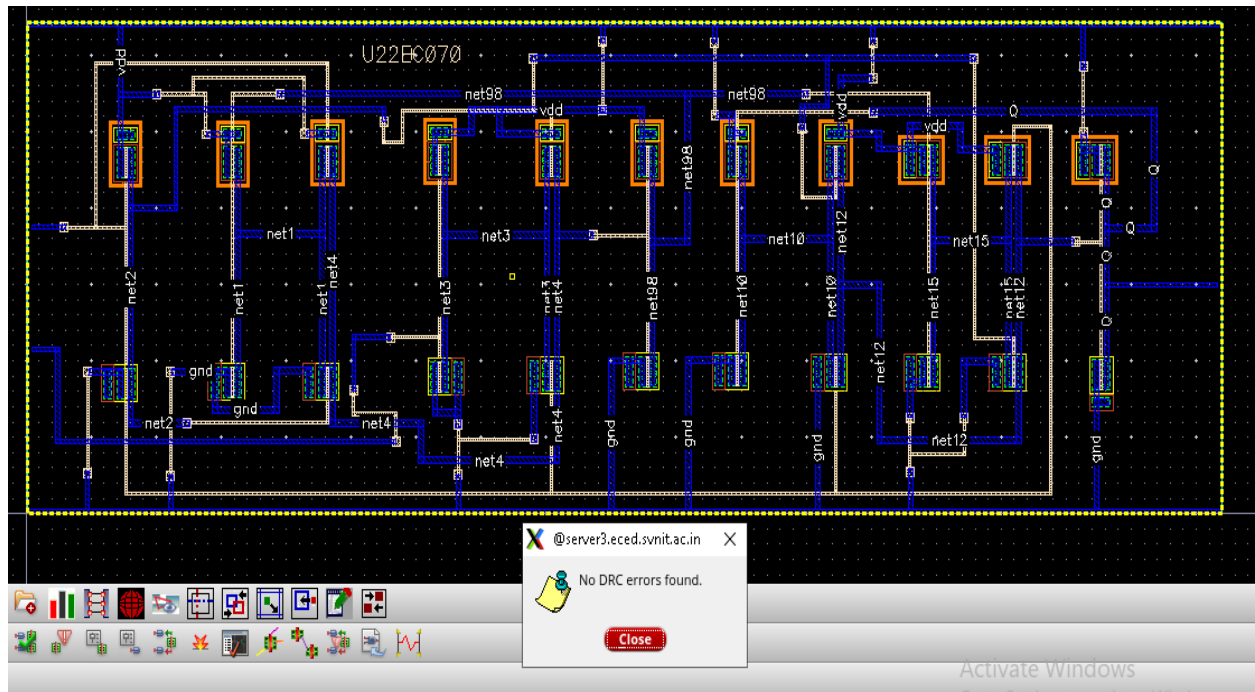
**Testbench:**

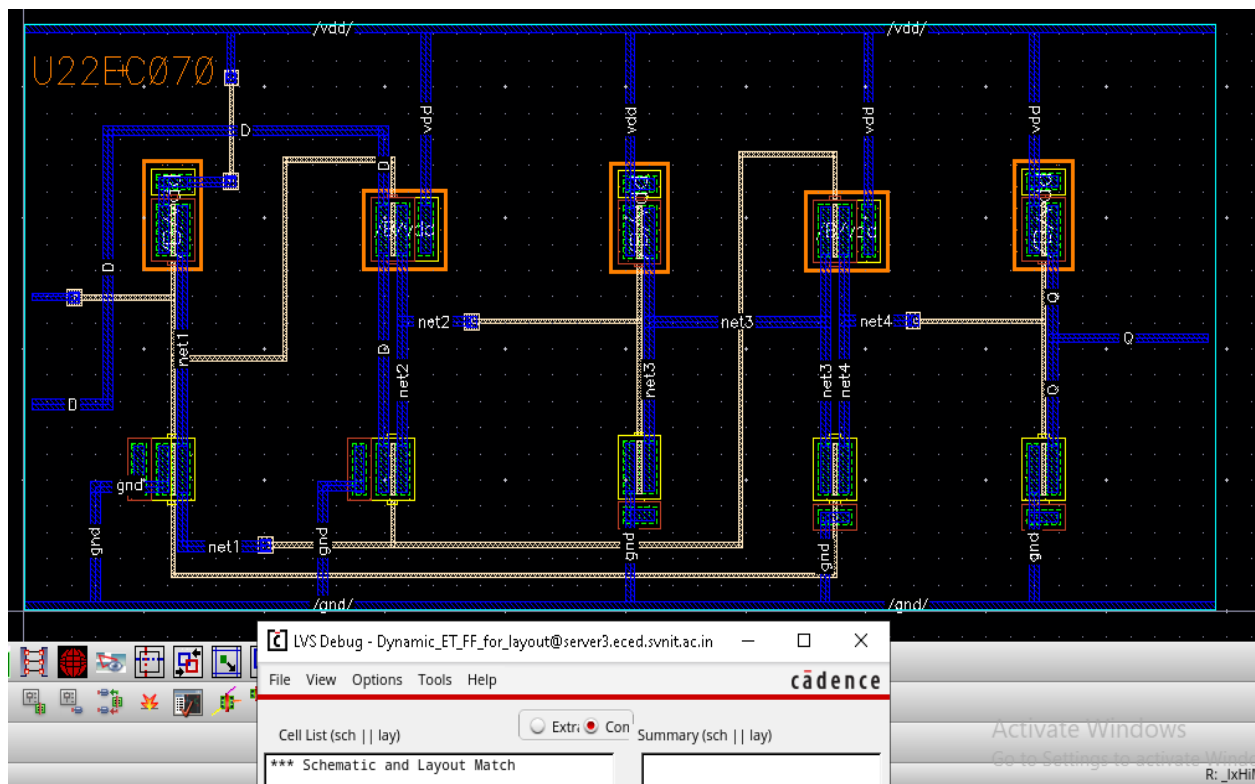
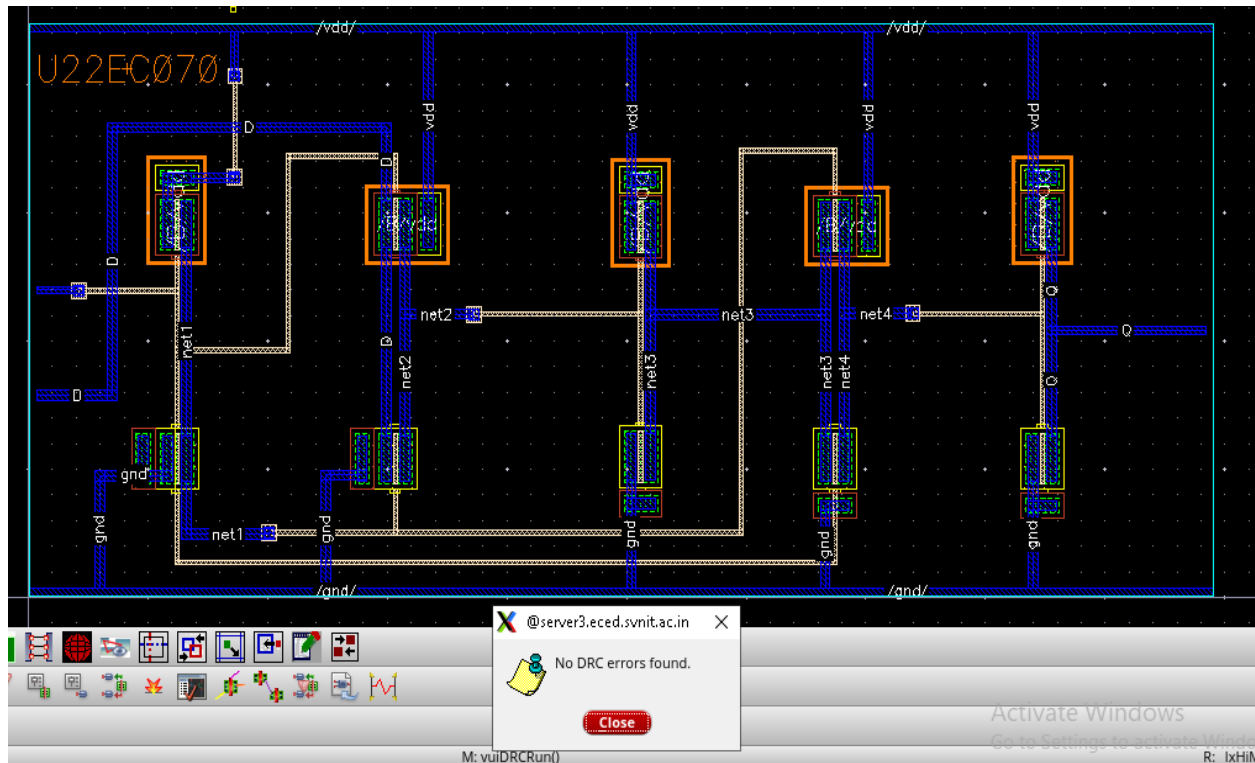
**Master slave based negative edge triggered flip flop:**

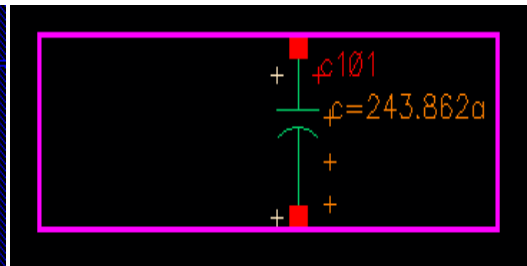
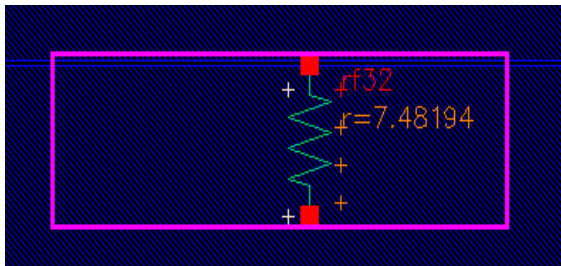
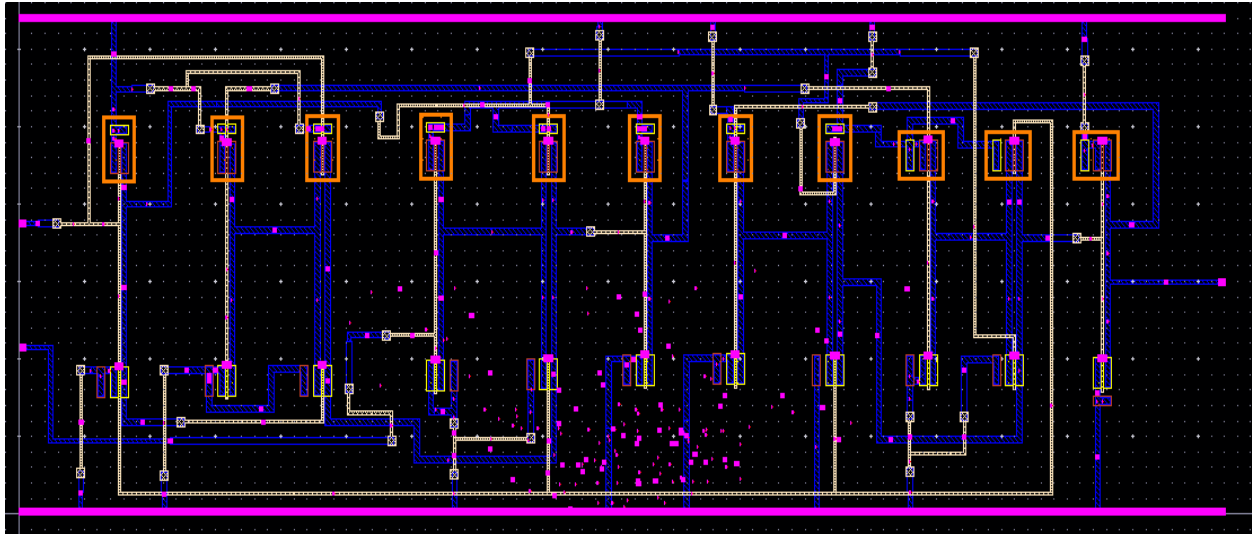


**Dynamic positive edge triggered flip flop:**



**Layouts:****Master slave based negative edge triggered flip flop:**

**Dynamic positive edge triggered flip flop:**

**RC Extraction:****Master slave based negative edge triggered flip flop:**

Library: Master\_Slave\_Based\_ET\_FlipFlop  
Cell: MS\_ET\_FF\_for\_layout\_tb  
View: schematic

Open Edit ADE L ADE Explorer

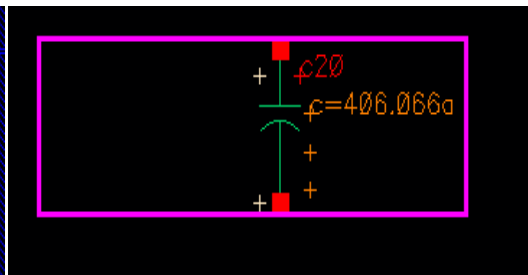
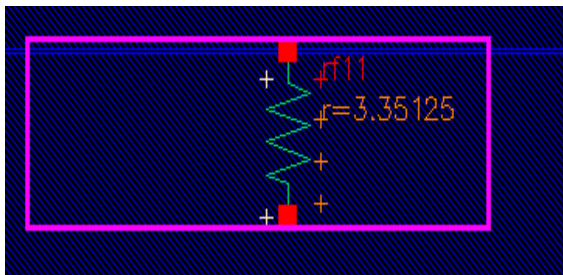
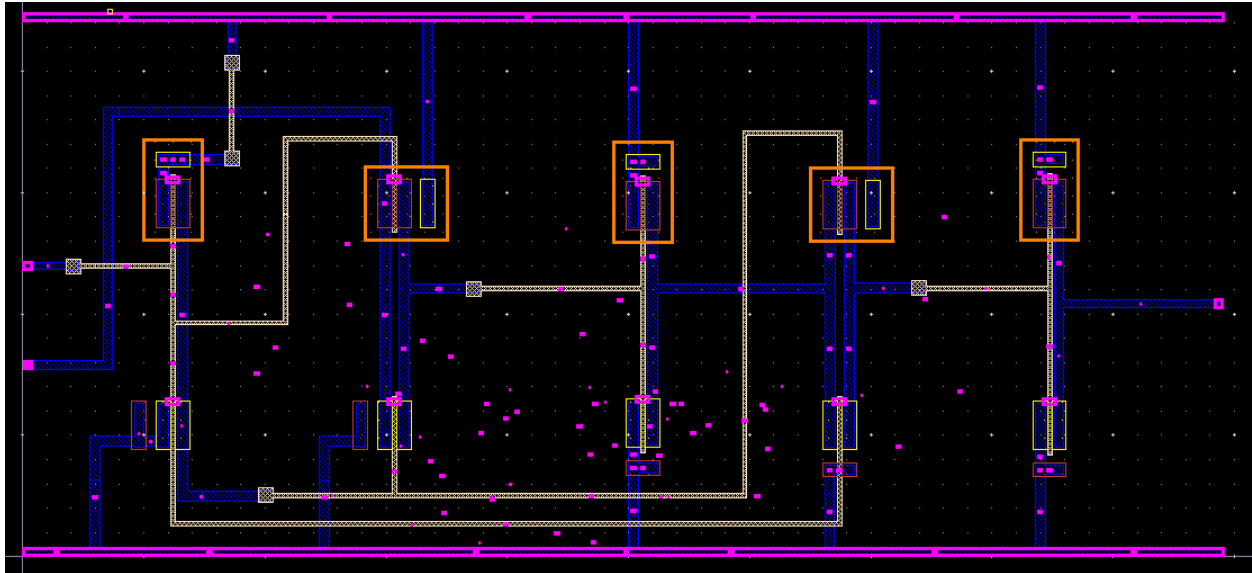
Library List: myLib  
View List: tic verilogahdl pspice dspf  
Stop List: spectre  
Constraint List:

Table View Tree View

Target: Instance

Instance	View To Use	Inherited View List
c130 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c131 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c132 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c133 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c134 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c135 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c136 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c137 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c138 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c139 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
c140 (analogLib pcapa...		spectre cmos_sch cmos.sch schematic...
rf1 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf2 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf3 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf4 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf5 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf6 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf7 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf8 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf9 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf10 (analogLib presist...		spectre cmos_sch cmos.sch schematic...
rf11 (analogLib presist...		spectre cmos_sch cmos.sch schematic...



**Dynamic positive edge triggered flip flop:**

Library: Dynamic\_ET\_FlipFlop  
 Cell: Dynamic\_ET\_FF\_for\_layout\_tb  
 View: schematic

Open Edit ADE L ADE Explorer

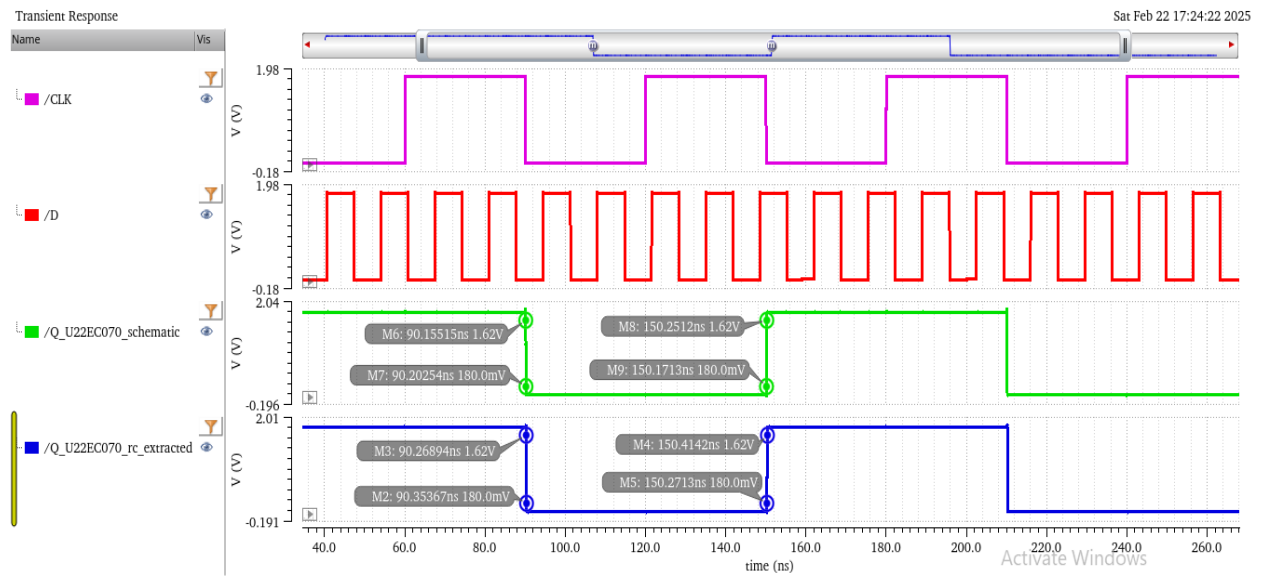
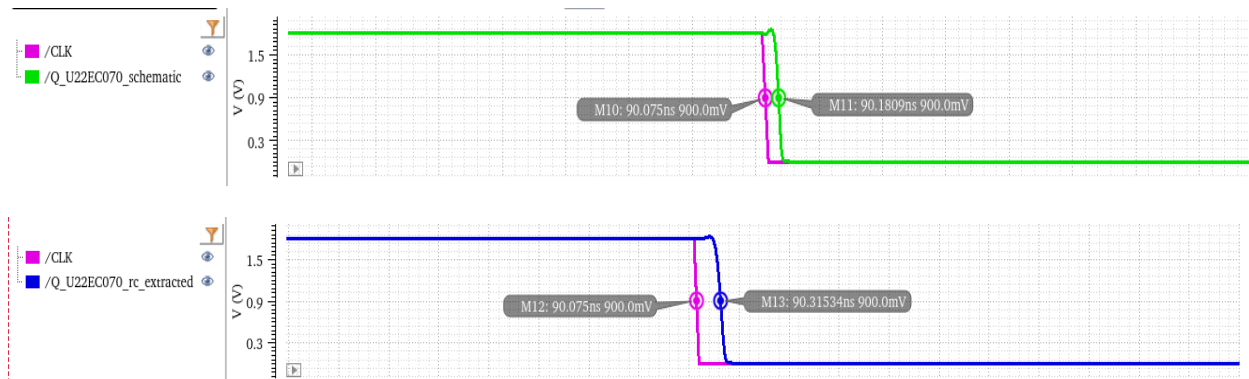
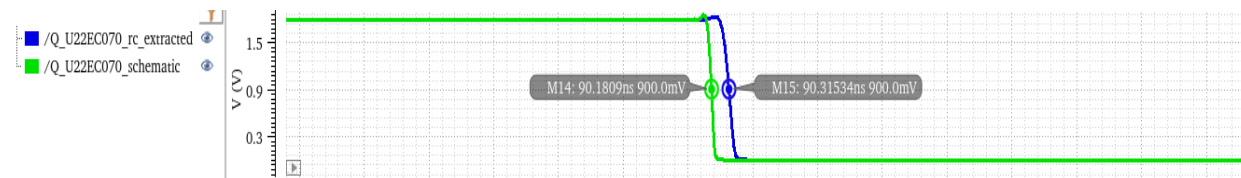
Library List: myLib  
 View List: tic verilog ahdl pspice dspf  
 Stop List: spectre  
 Constraint List:

Table View Tree View

Target: Instance

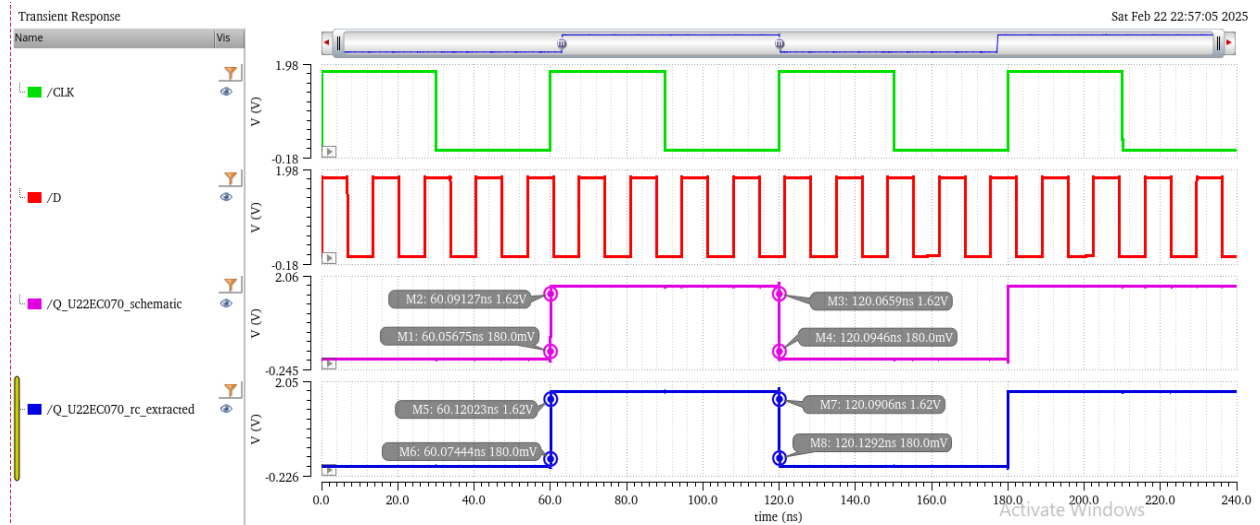
Instance	View To Use	Inherited View List
c49 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c50 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c51 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c52 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c53 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c54 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c55 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c56 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c57 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c58 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
c59 (analogLib pcapaci...		spectre cmos_sch cmos.sch schematic...
rf1 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf2 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf3 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf4 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf5 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf6 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf7 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf8 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf9 (analogLib presisto...		spectre cmos_sch cmos.sch schematic...
rf10 (analogLib presist...		spectre cmos_sch cmos.sch schematic...
rf11 (analogLib presist...		spectre cmos_sch cmos.sch schematic...



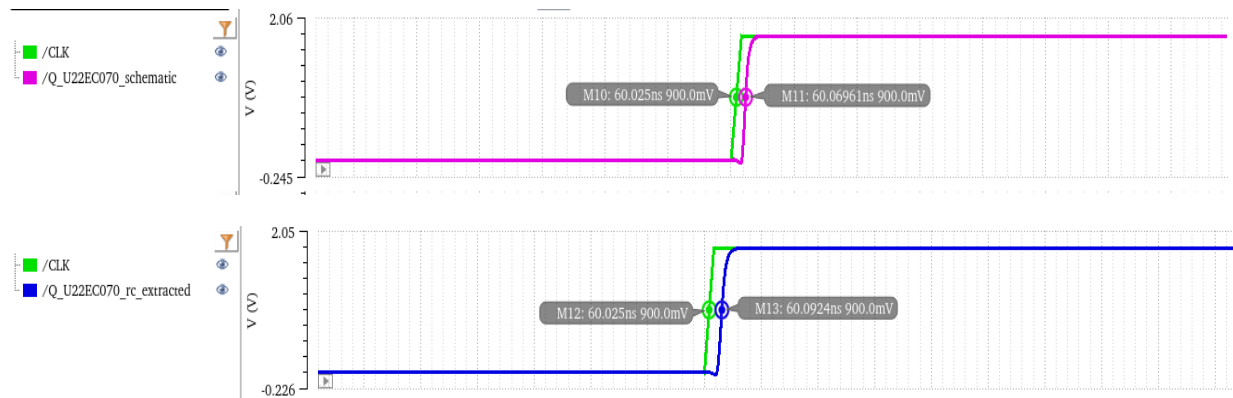
**Outputs:****Master slave based negative edge triggered flip flop:****a) Rise time and fall time:****b) CLK to Q delay:****c) Post layout simulation:**

## Dynamic positive edge triggered flip flop:

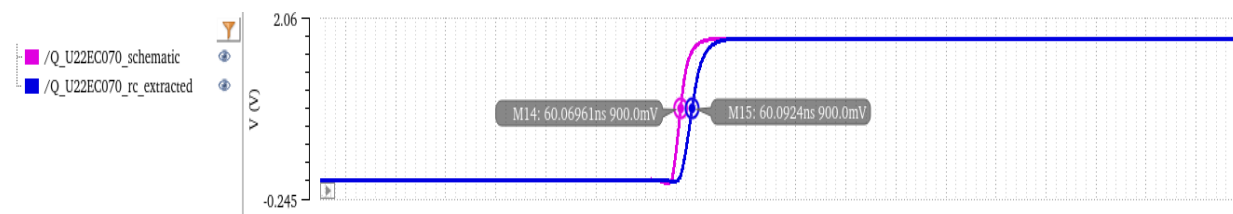
### a) Rise time and fall time:



### b) CLK to Q delay:



### c) Post layout simulation:



**Calculations:**

**Conclusion:**

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