DLCA MASTER QUESTION BANK

Theory

Q.1] Draw Detailed Von- Neumann architecture and explain in brief. Explain the advantages and disadvantages of the Von Neumann architecture.	**05**
Q.2] Explain bus arbitration and the different methods of centralized bus arbitration.	**10**
Q.3] Explain the various addressing modes.	**05**
Q.4] Explain how NAND is a universal logic gate with examples.	**10**
Q.5] Explain classic instruction pipeline stages. What are pipeline hazards?	**10**
Q.6] List methods used for designing a Hardwired Control Unit.	**03**
Q.7] List the levels of memory hierarchy.	**05**
Q.8] Draw and explain MIMD architecture under Flynn's classification.	**10**
Q.9] Explain D, T, S-R and J-K flip-flops with truth tables.	**05**
Q.10] Explain Register Organization of a processor.	**05**
Q.11] Describe Half Adder and Full Adder circuit with block and logical diagram & truth table. Design full adder using Half Adder.	**05**
Q.12] Explain IEEE-754 floating point representation.	**05**
Q.13] Explain the instruction cycle with state diagram.	**10**
Q.14] Write a short note on Encoder and Decoder.	**05**
Q.15] Explain Master-Slave JK Flip-Flop with PRESET & CLEAR.	**10**
Q.16] Explain different memory Mapping Techniques.	**05**
Q.17] List and Explain Characteristics Of Memory.	**05**
Q.18] What do you mean by cache coherence.	**05**
Q.19] Explain Concept of Locality of Reference.	**05**

Difference/Compare

Q.1] Explain the difference between a Multiplexer and Demultiplexer with suitable parameters.	**10**
Q.2] Explain microprogrammed control unit and hardwired control units, Compare microprogrammed and hardwired control units, List advantages/disadvantages.	**10**

Q.3] Differentiate computer organization vs. computer architecture. **10**

Q.4] Differentiate Interleaved and Associative Memory. **10**

Q.5] Compare SRAM vs DRAM with parameters. **10**

Q.6] Distributed vs Centralized Bus Arbitration. **10**

Numericals & Diagrams

Q1] Booth's Algorithm. **10**

Q2] Non-Restoring Algorithm. **10**

Q3] Restoring Algorithm. **10**