CS220A: COMPUTER ORGANIZATION

ASSIGNMENT - 2

Question - 1

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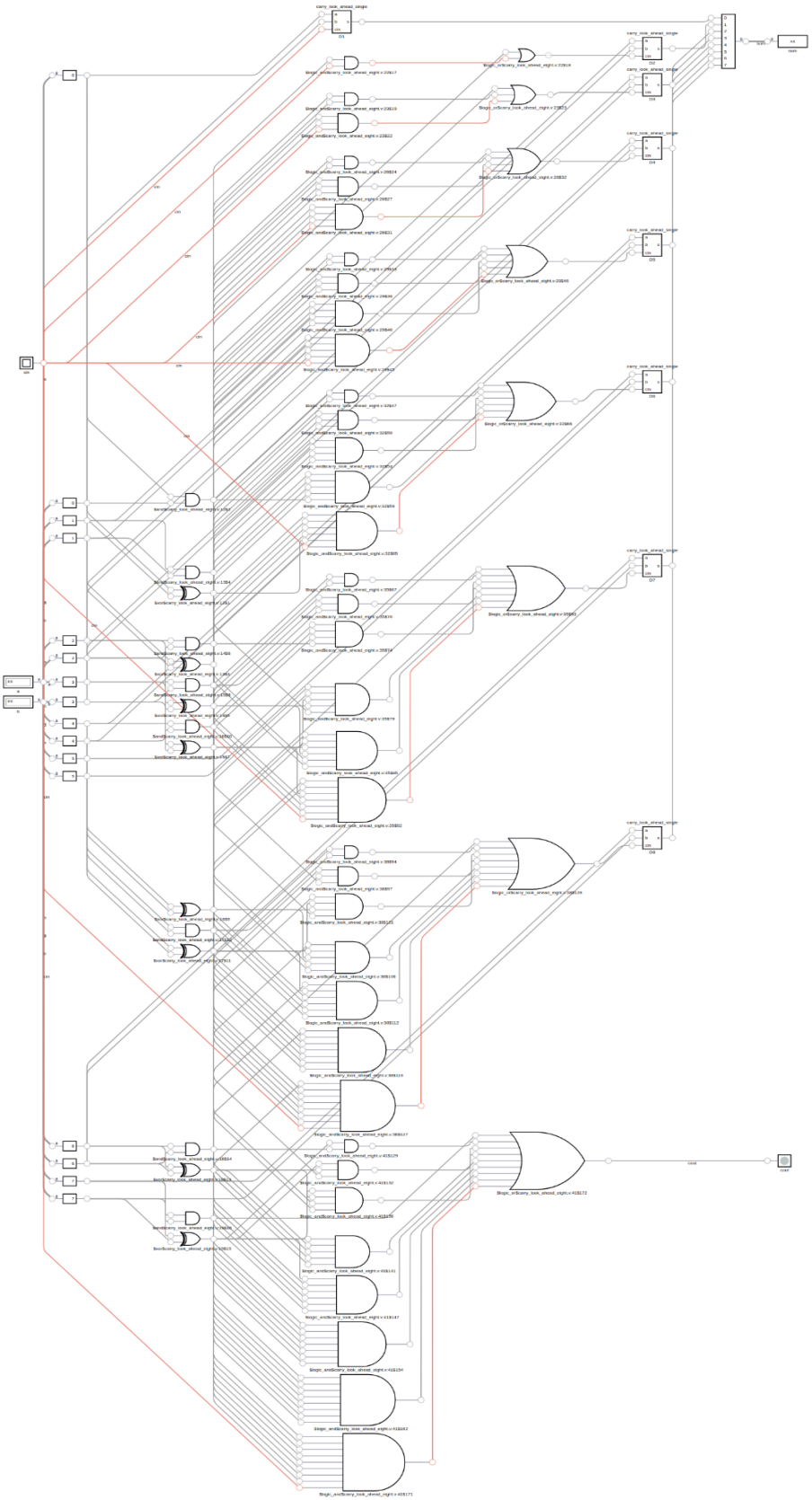
Circuit Diagram



Motivation

In the conventional 8 bit ripple carry adder the output gets delayed because each successive bit has to wait for the carry of the previous bit to get evaluated. This is called propagation delay.
This problem is solved by Carry look ahead adder. It uses more hardware than the regular adder but produces output faster.

WORKING

We define two variables for “Carry Generation” g and “Carry Propagation” p.
P[i] = XOR(A[i] , B[i])
G[i] = AND(A[i] , B[i])

The Carry output of each bitwise sum can be generated using P[i] and G[i].
C[1] = OR(G[0] , AND(P[0] , CIN))

In each successive step, we define
C[i] = OR(G[i-1] , AND(P[i-1] , C[i-1]))

But here we don’t use the variable C[i-1]. Instead of this, we use the whole expression of C[i-1]. This, therefore, reduces the delay since the evaluation of each carry element is calculated simultaneously.

After we get C[i], we pass the (A[i] , B[i] , C[i]) to adder and then we receive the output in Sum[i] get the final output.