Adib Rezaei Shahmirzadi

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Education

College of Electric and Computer Engineering, University of Tehran *Tehran, Iran*

Undergraduate student of B.Sc. in Software Engineering Sep. 2019 - Present

- **GPA of Last Year: 18.53 (Cum. GPA: 17.98/20)**
- Courses: Advanced Programming(20/20) - Data Structure(20/20) - Distributed Systems(20/20) - Electric Circuits(19.2/20) - Artificial Intelligence(18.75/20) - Neural Networks(18.5/20) - Discrete Mathematics(18.5/20)

Shahid Beheshti High School *Qaemshahr, Iran*

Affiliated with the National Organization for the Development of Exceptional Talents (NODET) Sep. 2013 - Jun. 2019

Research Interests

- **Cloud & Edge Computing**
- **Machine Learning**
- **Distributed Systems**
- **Computer Networks**

Professional Experience

Software Engineer at Yektanet *Tehran, Iran*

Yektanet is Iran's leading online ad network, reaching 25 million users monthly with 5 billion impressions Oct. 2021 - Mar. 2023

- System owner overseeing critical services, accountable for code reviews and ensuring system availability, scalability, and maintainability.
- Responsible for interviewing new software engineer candidates and improvement of the technical interview process.
- Running technical knowledge-sharing conferences among domain members.

Co-Founder at Gymtime *Sharif University of Technology*

Gymtime is a startup tech company associated with Sharif Accelerator providing an online reservation service and management solutions to gym owners and athletes Jan. 2022 - Jan. 2023

- Co-founder and team coordinator of 7 people in this group.
- Responsible for designing a clean technical architecture of the project.
- As a software engineer, responsible for developing features, improving services, and addressing technical challenges.
- As a site reliability engineer, responsible for automated operations like continuous deployment, building high available, fault-tolerant, scalable services capable of efficiently handling hundreds of requests per second.

Research Experience

Undergraduate Research Assistant *Remote/York University, Canada*

Under Supervision of Prof. P. Wang May. 2023 - Present

I am currently engaged in advancing deep reinforcement learning-based caching strategies tailored for IoT networks that handle transient data at the edge nodes. My current focus involves identifying and rectifying any existing flaws, as well as benchmarking the performance of these strategies in comparison to other models.

Undergraduate Research Assistant at High-Performance Network Laboratory *University of Tehran*

Under Supervision of Prof. A. Khonsari Jul. 2023 - Present

Given our limited resources and vulnerability to damage due to our small infrastructure in edge networks, we are exploring innovative solutions. We aim to strike a balance between the number of unique container image layers for improved response to requests and the number of duplicate layers to mitigate downtime in a node. To achieve this, we are leveraging layer-aware containerized service orchestration and machine learning algorithms.

Technical Skills

Computer Networking	WireShark, GNS3, TCL, PuTTY, Telnet, SSH
Technologies	Docker, Kubernetes, Apache Kafka, Redis Cluster, PostgreSQL, MongoDB, Prometheus, Grafana
Programming	Go, Python, Matlab, C/C++, Java, TypeScript, Verilog HDL, C#, HTML, CSS, Shell Script
Web Development	Django, React, Vue, Spring, JUnit

Awards and Honors

2019	**Ranked 216 (Top 0.2%)** in Konkur (Iranian University Entrance Exam) out of 164,000 participants.	*Iran*
2013	**Awarded** as an exceptional talent student in elementary school	*Iran*

Teaching Experience

University of Tehran *Tehran, Iran*

- **Teaching Assistant** Artificial Intelligence, H. Fadaei — Spring 2023
- **Teaching Assistant** Algorithm Design, MJ. Dousti — Spring 2022, Fall 2022
- **Teaching Assistant** Data Structure, H. Faili — Spring 2021, Fall 2021, Spring 2023
- **Teaching Assistant** Discrete Mathematics, S. Mohammadi — Spring 2023, Fall 2023
- **Teaching Assistant** Advanced Programming, R.Khosravi — Fall 2021, Spring 2022, Fall 2022

Academic Projects

Neural Network and Deep Learning: Implemented various model designs from multiple research papers, including Adaline, Madaline, Linear Regression, CNN, Faster-RCNN, Transfer Learning, LSTM, and GAN as part of my NNDL course projects.

Artificial Intelligence: Implemented seven projects of different artificial intelligence topics such as Search Algorithms, Genetic Algorithms, Classification, Multi-layer Neural Networks, and Regression as part of my AI course projects.

Hardware implementation of a Multi-Layer Perceptron Neural Network: Implemented Multi-Layer Perceptron model with Verilog HDL. To test the design, we used TensorFlow to generate neural network parameters from existing training data. This model is used to classify CIFAR-10 images.

Computer Networking: Developed an FTP server, utilizing low-level socket programming techniques. Additionally, conducted NS2 simulations and analyzed various parameters within a wireless network, including Throughput, Packet Transfer Ratio, and Average End-to-End Delay. Furthermore, I implemented TCP congestion control mechanisms using UDP network sockets. Lastly, designed both distance vector and link-state algorithms to determine the most efficient routing paths between routers in a specified network topology.

Operating System: Enhanced a cloned MIT xv6 kernel by introducing additional functionalities in the areas of CPU scheduling, memory management, and CPU synchronization. This customized kernel has undergone rigorous testing and can run in the Qemu simulator. Additionally, I developed a word counter using MapReduce to gain insights into process management and intercommunication techniques. Moreover, a multi-threaded image filtering system has been implemented, utilizing both multi-threading and serial programming approaches.

Simple Loop Compiler: Implemented a compiler for a new object-oriented programming language, called *Simple Loop* in 4 phases. These phases include lexer and parser analyzer, symbol table and AST tree, type checking, and code generation. This is done by compiling *Simple Loop* code to Java bytecode and then running the bytecode instructions.

ARM Implementation on FPGA: Designed and Implemented ARM CPU with four-stage pipeline and 13 instructions. Written in synthesizable Verilog HDL code and tested in an FPGA with Quartus II simulator.

Workshops

Introduction to ML Workshop *ACM, University of Tehran*

Directed by the Association for Computing Machinery (ACM) Student Chapter, University of Tehran — July. 2021

- Practiced base machine learning concepts with hands-on projects.
- Implemented k-nearest neighbors, linear and non-linear regressions, and normalization techniques on real datasets.

Teaching Assistance Training *University of Tehran*

A three-hour workshop held by the School of ECE, University of Tehran — Jan. 2021

Languages

English Professional proficiency

Persian Native