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The phase II ATLAS Pixel upgrade: the Inner Tracker (ITk)

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Abstract: The entire tracking system of the ATLAS experiment will be replaced during the LHC Phase II shutdown (foreseen to take place around 2025) by an all-silicon detector called the *ITk* (Inner Tracker). The pixel detector will comprise the five innermost layers, and will be instrumented with new sensor and readout electronics technologies to improve the tracking performance and cope with the HL-LHC environment, which will be severe in terms of occupancy and radiation. Several layout options are being investigated. All of these include a barrel part and ring-shaped supports in the endcap regions. All structures will be based on low mass, highly stable and highly thermally conductive carbon-based materials cooled by evaporative carbon dioxide. Different designs of planar, 3D, and CMOS sensors are being investigated to identify the optimal technology for the different pixel layers. While the RD53 Collaboration is developing the new readout chip, the pixel off-detector readout electronics will be implemented in the framework of the general ATLAS trigger and DAQ system. A readout speed of up to 5 Gbit/s per data link (FE-chip) will be needed in the innermost layers going down to 640 Mbit/s for the outermost. This paper presents an overview of the different components of the ITk and the current status of the developments.

Keywords: Hybrid detectors; Particle tracking detectors; Radiation-hard detectors

Contents

1   Introduction

In 2024–2026 the Large Hadron Collider (LHC) will be upgraded to the High Luminosity-LHC (HL-LHC). HL-LHC will operate at a five times higher luminosity (5–$7 \times 10^{34} \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$). As a consequence, the detectors will have to handle higher particle densities leading to higher occupancies in the detector components and higher radiation levels. The number of events per collision will increase from around 25 to up to 140–200 (depending on the luminosity) events per collision. As the tracking systems of the detectors at HL-LHC have to cope with this increased particle multiplicity, the ATLAS detector [1] will upgrade its inner detector during Phase II (2024–26) completely. The currently existing inner detector, providing the track information of crossing particles, will be replaced by an all-silicon tracking system consisting of a 5-layer Pixel detector as the innner part and a 4-layer Strip detector as the outer part. All components of the new Inner Tracker (ITk) are currently under development. In the next sections an overview of this R&D program for most of the different components needed for the ITk Pixel system is described.

2   ITk layout

The final layout of the ITk Pixel detector is not yet decided. Two important decisions are pending: forward angle coverage ($\eta \leq 3.2$ or $\eta \leq 4.0$) and use of flat or inclined structures in the barrel layers. While in the flat layout the modules of the barrel section would be located parallel to the beam axis,
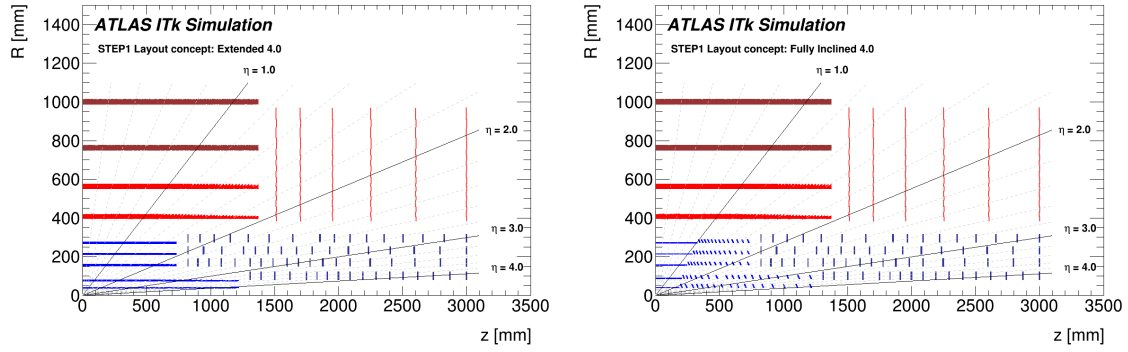
Figure 1. Simulated hit positions on the R-z plane for an ATLAS Inner Tracker layout with extended inner barrel layers (left) and inclined inner and outer barrel layer (right), optimized for measuring at least nine space points on tracks up to $|\eta| \leq 4.0$ for $|z_0| < 150$ mm. Pixels (blue), short strips (light red) and long strips (dark red) are shown [2].

in the inclined layout the outer modules of a stave would be inclined and therefore tracks originating from the interaction point would cross the modules at an angle close to normal. The latter option can potentially reduce the number of modules needed. An angular coverage up to $\eta = 4.0$ will provide measurements for particles being scattered under a very small angular. This would complement the calorimeter measurements for these particles with tracking information. This option would require more electronic modules and longer support structures. Ongoing simulation studies will show the best option which then will become the baseline layout for the ITk pixel system. Figure 1 shows the two different options for angle coverage of $\eta \leq 4.0$.

3   ITk Pixel modules

The basic electrical unit of the Pixel detector is a module. Depending on the finally chosen layout about 10,000 modules are needed for ITk. The baseline module concept is a hybrid module which uses a sensor and a readout chip bump bonded to each other at the pixel level. In addition, other concepts are being investigated like monolithic CMOS Pixel detectors especially for the outer layers (see section 3.3).

The type of modules will depend on the layer, the layout option (inclined or flat), and on the type of sensor to be used. 3D sensors (see section 3.1.2) will result in single chip modules, while planar sensors (see section 3.1.1) can be built in 2×2 or 1×2 chip modules. The inclined part of a stave would be equipped with 1×2 chip modules, while for the flat part for the outer layers and for the disks 2×2 chip modules will be used. A sketch of the different module layouts is shown in figure 2.

Because the new pixel readout chip is still in development the final size of this chip is not yet defined, its dimensions are assumed to be similar to the FE-I4 pixel chip [3] ($\sim 17 \times 20$ mm^2 for the active region and a periphery region of $\sim 2 \times 20$ mm^2). Accordingly, quad-chip modules would have dimensions of around 4×4 cm^2 and double chip modules around 2×4 cm^2.

3D sensor modules would be preferably used for the innermost layers, because of their advantages in power consumption and radiation tolerance. Planar sensors can be used for double-chip and quad-chip modules due to the large size sensor production feasibility.
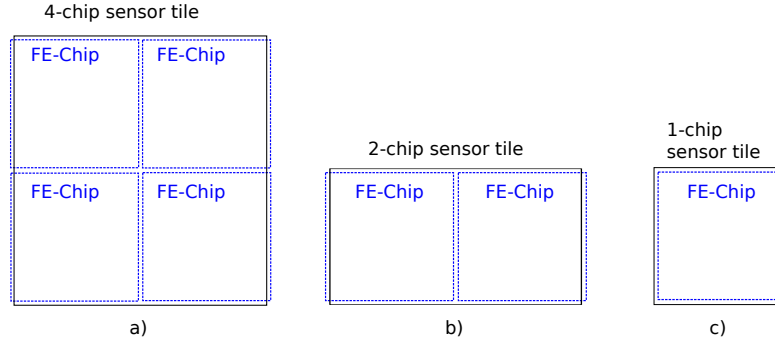
Figure 2. Sketch of the different module geometry options for ITk, a quad-chip module (a), a double-chip (b) module, and a single-chip module (c) is shown. The black solid line is for the sensor edge while the blue dashed lines indicate the front-end ASIC.

To avoid inactive regions in between the chips longer pixels are foreseen in the sensor design as well as minimising the edge region while still preventing the voltage break down. The technique to be used depends on the sensor and module type choice. Chips and sensors will be as thin as possible. Sensors with thicknesses in the range of $100\,\mu m$ to $150\,\mu m$ and $150\,\mu m$ thick ASICs show good results in handling and performance. Nevertheless, handling and production yield (favouring thicker devices) have to be balanced against material reduction and radiation tolerance (favouring thinner devices). Finally, a flexible printed circuit to which the needed passive components are assembled is glued to the module and provides all connections to and within the module. The connections between the module and this printed circuit are done with standard wire bonds.

All chips within the module will be controlled in parallel (shared clock and command inputs), but the module may have one or several dedicated data outputs. In order to keep the amount of data cables as low as possible, data lines of read-out chips might be combined into a higher bandwidth signal wherever possible.

3.1 Sensors

Different sensor technologies are being investigated with several vendors for each technology, a new generation of planar sensors as well as 3D sensors, which build the basis for the well known hybrid module composition. The final pixel size is still under study. For the reduced pixel cell area of $2500\,\mu m^2$ two sets of dimensions are being investigated: $25 \times 100\,\mu m^2$ and $50 \times 50\,\mu m^2$. Pixel cell designs have been implemented for the different sensor technologies and are under investigation now. Once the final layout has been chosen these two options need to be compared concerning tracking performance to give an indication which option to choose. The final read-out chip providing the smaller pixel pitch will also be essential to study real assemblies with the different pixel geometries.

3.1.1 Planar sensors

A new generation of planar pixel sensors using n-in-p technology (current sensor are built in n-in-n technology) is under development for ITk. The final thickness of the devices has to be defined still. Currently, investigations for thin devices, $100\,\mu m$ to $150\,\mu m$, are ongoing. The aim is to provide a sensor which is thinner compared to the sensors used in the Insertable B-Layer (IBL) [5]

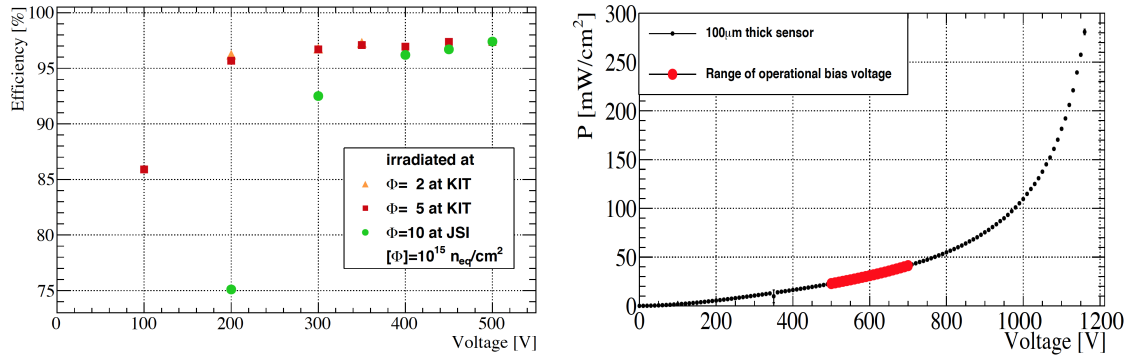**Figure 3**. Left: comparison of hit efficiencies of FE-I4 modules with $100\,\mu$m thin planar sensors irradiated at a fluence of $2 \times 10^{15}\mathrm{n_{eq}/cm^2}$ to $10^{16}\mathrm{n_{eq}/cm^2}$. The expected efficiency of around $97\,\%$ is reached always, but the applied voltage differs. The higher the irradiation level, the higher the needed bias voltage. For the measurement at $2 \times 10^{15}\mathrm{n_{eq}/cm^2}$ the point at $100\,$V is missing, unfortunately, but it would be higher than the one for the measurement at $5 \times 10^{15}\mathrm{n_{eq}/cm^2}$. The shape of the curves is not changing with irradiation. Right: power dissipation estimated for $100\,\mu$m thin sensors at a temperature of $-25\,°$C irradiated at a fluence of $10^{16}\mathrm{n_{eq}/cm^2}$, where the range of possible operational bias voltages is based on the results shown in the left plot. The values of the leakage currents used in the calculation are for a sensor after 11 days of annealing at room temperature [4].

($200\,\mu$m) or the outer layers of the current Pixel detector ($250\,\mu$m), which nevertheless provides a sufficient hit signal to be read out by the FE-chip. An advantage of the n-in-p technology is single side processing and reduced handling complexity. The guard ring structure is implemented on the front side, leaving the edges of the sensor at a potential close to the one of the backside. To avoid sparking between the sensor periphery and the FE-chip, isolation techniques have been investigated successfully. Either deposition of Benzocyclobutene (BCB) or parylene would be possible [6].

The cell structure design has been optimised with respect to the smaller pitch of the ITk readout chip based on beam test results obtained with FE-I4 chips. Preliminary electrical characterisation of these devices can be found in ref. [7].

Thin planar sensors have been irradiated up to a fluence of $10^{16}\mathrm{n_{eq}/cm^2}$ to investigate the feasibility of employing them in the innermost pixel layers. A hit efficiency up to 97% with FE-I4 modules has been reached in test-beam measurements by $100\,\mu$m thin sensors at a bias voltage of $350\,$V for a fluence of $5 \times 10^{15}\mathrm{n_{eq}/cm^2}$. The left part of figure 3 shows the efficiency obtained with $100\,\mu$m thin sensors versus the applied bias voltage for different fluences. The shape of the curves is not depending on the irradiation level, but the bias voltage needed to reach the 97% efficiency level increases with fluence, as expected (note that there is no measurement for $100\,$V at $2 \times 10^{15}\mathrm{n_{eq}/cm^2}$). Comparing this performance with those of thicker sensors it can be stated that $100\,\mu$m thin sensors can provide the same tracking efficiency at lower bias voltages. At a fluence of $10^{16}\mathrm{n_{eq}/cm^2}$ $500\,$V are needed to reach a hit efficiency of 97% in test-beam measurements. Based on this result, the power dissipation has been estimated to be in the range of $25\,$mW/cm^2 to $45\,$mW/cm^2 at a temperature of $-25\,°$C for a sensor after 11 days of annealing (see figure 3).

3.1.2 3D sensors

3D silicon detectors [8] are candidates to be used for the innermost layer(s) of the barrel pixel system and some of the inner end-cap rings due to their excellent radiation hardness at low operational voltages as well as moderate temperatures with low power dissipation compared to planar sensors. 3D silicon detectors have recently undergone a rapid development from R&D to industrialisation with their first operation in the IBL.

IBL-generation 3D pixel detectors coupled to FE-I4 pixel electronics have been found to have hit efficiencies in testbeam measurements larger than 97% at 170 V after irradiation to $10^{16} n_{eq}/cm^2$ for normally incident minimum ionizing particles with a power dissipation of $15\,mW/cm^2$ at a temperature of $-25\,°C$ [8], see figure 4. The 3D design under development for the ITk detector builds on the successful IBL 3D sensor. Columns of $5\,\mu m$ to $10\,\mu m$ diameter are alternately n- and p-type doped into the high resistivity p-type silicon bulk, defining the pixel configuration. The 3D sensor technology inherently allows for slim edges of $15\,\mu m$ to $150\,\mu m$ [8], or even active edges sensitive up to the physical sensor edge [9]. Productions of 3D devices with smaller pixel sizes of 25×100 and $50 \times 50\,\mu m^2$ compatible with the FE-I4 chip have already been carried out and the prototypes are currently being tested. Furthermore, specific productions of 3D sensors compatible with the RD53 chip have also been completed by various companies (CNM Barcelona, FBK Trento, SINTEF Oslo).

3.2 Front-end electronics

The new front-end ASIC is currently under development. The RD53 Collaboration [10] is developing a pixel readout chip for both ATLAS and CMS usage at the HL-LHC. The chip must cope with the HL-LHC requirements in terms of hit occupancy and radiation levels. Based on simulations the hit occupancy is expected to be around 0.007% for the outermost layer and 0.23% for the innermost layer (numbers are for the end of stave region) [11].

In ITk the chip will be used in all layers. Nevertheless, the most critical performance is driven by the innermost layer. Compared to the IBL pixel chip the new chip will be improved in sevaral
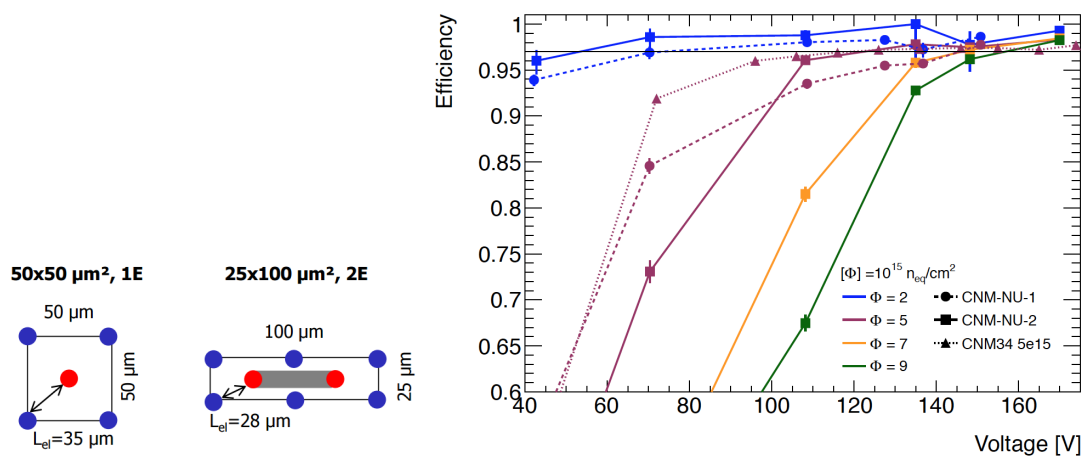

Figure 4. Left: design of 3D pixel cells with $50 \times 50\,\mu m^2$ and $25 \times 100\,\mu m^2$ size [8]. Right: hit efficiency vs. voltage for different fluences in various 3D sensor devices. The 97% benchmark efficiency is marked [8].

aspects. The pixel size will be reduced by a factor of five. The hit threshold will be around 600 electrons (compared to 2000 electrons) and triggers at a rate of 1 MHz can be handled. The transmission bandwidth is increased to 5 Gbit s^{-1} (compared to 160 Mbit s^{-1}). All this has been implemented without a significant increase of the power consumption of the chip. The ASIC is being designed in 65 nm CMOS technology (through a CERN frame contract).

The small feature size is critical to create the small pixel cells being needed for ITk. Radiation studies of 65 nm feature size process revealed an unexpected issue, the previously unknown effect called Radiation Induced Short Channel Effect (RISCE). Together with the already known Radiation Induced Narrow Channel Effect (RINCE), it is a CMOS damage mechanism, which leads to the fact, that small transistors, which are needed for high logic density designs, are bad for radiation tolerance [12]. Therefore, modest compromises have to be made on logic density. Taking this into account the RD53 chip still provides much higher logic density than the FE-I4 and can be qualified up to a dose of 5 MGy. Nevertheless, the innermost two layers have to be built removable to provide functionality over the full planned operation time of HL-LHC.

A first prototype ASIC (FE65-P2) [13] has been produced and is currently under test. FE65-P2 has the same pixel size and same CMOS process as the foreseen prototype chip RD53-A (submission in spring 2017). FE65-P2 also demonstrates the performance of the analog front-end part to be used in RD53-A and validates the superb analog-digital isolation needed for 600 electron threshold stable operation. The discriminator threshold of a bare FE65-P2 was tuned to values below 600 electrons. While a significant temperature variation of the threshold is observed on irradiated chips, pixels with a 'radiation hard' front-end variant show the smallest effect, at a level acceptable for operation. Generally, performance is still good even after 5 MGy. The threshold to detect a charge pulse within 25 ns was measured to be below 500 electrons for a discriminator threshold of 300 electrons. FE65-P2 bump bonded to sensors show a small increase in noise with nominal noise achieved at a bias voltage of -10 V (full depletion expected at -300 V) which confirms expectations that the noise performance is most sensitive to the inter-pixel capacitance. Data were successfully taken with a 50 MeV proton beam which shows pixel hit clusters the size of which matches the expected depletion depth. These excellent results with FE65-P2 give significant confidence in the RD53-A design.

3.3 Monolithic sensors

As an alternative to hybrid modules, HV-CMOS pixel detectors are being investigated. Originally designed for charge collection in an epitaxial layer (10 μm to 20 μm thick), new approaches have them coping with the rate and radiation environment expected at the HL-LHC. Options for allowing high depletion voltages and large depletion depths as well as radiation hardness improvements and device thinning are being studied.

Currently the studies on HV-CMOS devices aim for demonstrating the feasibility of its usage in the outer layers of ITk. For this several technologies have been explored and characterised as stand-alone sensors as well as bonded to the FE-I4 pixel chip (as a 'hybrid') either via bump bonds or via glue bonding (capacitively coupled pixel detector, CCPD). The promising results should lead to a large scale demonstrator chip in 2017 showing usability of the CMOS technology in ATLAS ITk. More information can be found in [14] and [15]

4 Powering and detector control

4.1 Serial powering

Powering each of the 10,000 ITk modules in parallel would lead to an unacceptable amount of material inside the detector volume. Therefore, powering options with active voltage regulators inside the detector volume have to be taken into account and as baseline serial powering has been chosen. In this concept a chain of modules is supplied by a constant current source and the modules themselves will perform the current to voltage conversion using built-in shunt regulators in the FE-chips. This way the current being transported is only the current of a single module, while the voltage is the sum of voltages needed by all modules. The modules in the powering chain will operate on different ground levels, so that the communication path has to be AC-coupled.

Tests with serially powered FE-I4 modules, which already include the shunt-regulator foreseen for ITk (an Low-Drop-Out (LDO) shunt regulator), show that the power scheme has no impact on the chip operation and functionality. Neither cross-talk nor noise increase could be observed and the minimum tunable threshold is also not influenced by the powering [16].

4.2 Detector control

To ensure safety, reliable control and information for debugging the ITk Pixel a **D**etector **C**ontrol **S**ystem (DCS) [17] is foreseen. It provides three independent control and information paths, which differ in granularity, availability, and reliability.

The safety path, which has the lowest granularity, consists of a hard-wired interlock system, which acts directly on power supplies or other equipment, if the safe operation of the detector cannot be guaranteed any more.

The control and feedback path acts on module level. It is the interface between operator and detector. This path enables steering of all components of the detector and provides monitoring information as feedback. It is made up by the DCS network, consisting of DCS chip and DCS controller, as described in section 4.2.1.

The diagnostics path is embedded into the module's data path and provides the operator with additional monitoring values in order to debug the behaviour of the detector or tune its performance. It delivers information on read-out chip level and is therefore the path with the finest granularity.

4.2.1 The DCS chip and controller

The main component of the control path is the DCS chip [18] which provides the monitoring and control capabilities on module level. Figure 5 shows how the DCS chip is integrated within the serial power chain. From the DCS computer the commands are sent to the DCS controller over a long term protocol. The CAN[1] protocol is currently envisioned for use.

The DCS chip is specially designed to work in a serial power chain. It is placed on the module flex of each pixel module. It includes bypass capability for the modules, realised by a shunt transistor. The bypass can be activated or deactivated by command. Furthermore, a hard-wired automatic activation of the bypass transistor in the case of over-voltage or over-temperature is included. The thresholds for the automatic activation are defined with external components on

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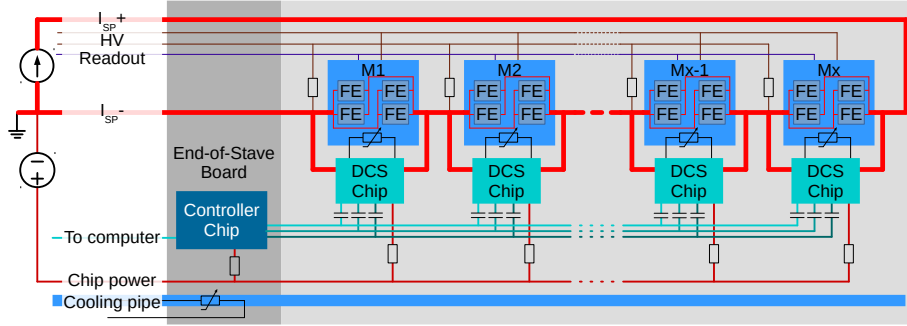
[1]CAN: Controller Area Network.

Figure 5. Diagram of how a Pixel Serial Powering Protection chip would be integrated into a serial powering chain.

the flex print. This bypass is off after power-up or in the case of power-loss. For feedback the DCS chip includes an ADC, which allows for monitoring of the module temperature and voltage. As the DCS chip is mounted in close vicinity to the detector modules, even in the innermost layer, it needs to fulfil the same radiation hardness as the read-out chips of the innermost pixel layer. The DCS chips are powered independently from the read-out chips. The DCS chips of one serial input current (I_{SP}) chain share the same power line (see figure 5). The power return of the DCS chips is merged with the serial supply current I_{SP}. The DCS power line is also used as an external reference for detecting drifts of the internal reference. There are three independent communication lines to the DCS chips of one I_{SP} chain. The DCS chips are AC coupled to the communication lines. Currently up to eight modules are foreseen to build one I_{SP} chain. The DCS controller realises the communication between the DCS computer and the DCS chip. It serves as a bridge between a long range communication from the computer to the short range communication used by the DCS chip.

5 Detector readout architecture

Due to the very high radiation levels expected in the innermost detector volume, placing the opto-elements at the end of staves or rings is not feasible. Therefore, the data transmission link will be split into an optical part, running from the counting caverns down to the Inner Detector (ID) end-plate region (final location still to be defined) and an electrical part, connecting the opto-components to the front-end electronics on the rings or staves. The off-detector components don't need to be radiation hard and therefore can be off-the-shelf commercial components. Optical plug-ins and FPGA based signal processing logic will be placed here. The optical signal will run via optical fibres, which need to be radiation hard to withstand the irradiation along the routing path up to the opto-converter boards. The electrical part needs to serve the data transmission between optical converters and front-end electronics at the needed bandwidth, which depends on the location inside the detector, and must not introduce too much material into the detector not to disturb the particle flight towards the outer subdetectors. As the innermost layers will run at the highest bandwidth, this is the driving factor for the development. Very thin cables serving a bandwidth of around 5 Gbit/s are under development and study.

The final read-out electronics is still under discussion [11]. As baseline the TTC[2] links should operate at a bandwidth of 160 Mbit/s, likely using 8b/10b encoding. This makes sending of more complex commands than a simple trigger signal possible. The TTC links are aggregated using the GBT[3] ASIC, which is currently under development at CERN. In contrast, the data links will use the encoding as provided by the read-out chip, such as 64b/66b, possibly after multiplexing of the links of read-out chips on one module in case the available bandwidth allows this. The data links will operate at an optical bandwidth of 5 Gbit/s having lower speed electrical links being aggregated into the faster optical one.

6 Conclusion

The development of the components for the ATLAS ITk Pixel detector is ongoing. R&D activities in the sensor and read-out chip area show already feasible solutions for a future module concept. Alternative approaches such as monolithic pixel chips are also being studied. Simulation studies on the layout options as well as the physics performance will indicate the best layout, the requirements to be put for the electronics and the read-out bandwidths. Intense investigations in meeting the known or assumed requirements for the ITk pixel operation are driving the R&D effort in all the collaborating labs. The Technical Design Report for the ITk Pixel detector is due by end of 2017. The collaboration is putting high priority on making baseline decisions where several options are still present.

Acknowledgments

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[2]TTC: Timing, Trigger, Control.

[3]GBT: Gigabit Transceiver.

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