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I Semester Diploma Examination, December-2023

DIGITAL ELECTRONICS

Time : 3 Hours]

[Max. Marks : 100

- Instructions :**
- (i) Answer one full question from each section.
 - (ii) One full question carries 20 marks.

SECTION - I

1. (a) (i) Compare analog signal and digital signal. **5**
 (ii) Convert decimal number $(27)_{10}$ into binary. **3**
 (iii) Convert the octal number $(1574)_8$ into binary. **2**
- (b) (i) Mention the features of ASCII Code. **5**
 (ii) Add $(5B6)_{16}$ and $(63A)_{16}$. **3**
 (iii) Subtract $(1010)_2$ from $(1101)_2$. **2**
2. (a) (i) Explain the procedure for binary to gray conversion with an example. **5**
 (ii) Subtract $(1001)_2$ from $(1011)_2$ using 1's complement method. **5**
- (b) (i) Explain distributive law. **5**
 (ii) State and prove any one De-Morgan's theorem. **5**

SECTION - II

3. (a) (i) Show realization of NOT, AND & OR gates using NOR gates. **5**
 (ii) List any five laws of Boolean algebra. **5**
- (b) Write NOT, AND, OR, NAND, NOR gates with symbol and truth table. **10**



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4. (a) (i) Simplify the below expression using Boolean laws and draw the logic diagram for the simplified expression. 5

$$Y = (A + B)(A + C)$$

- (ii) Simplify the following expression using K-map and draw the logic diagram for the simplified expression : 5

$$F(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC$$

- (b) (i) Describe SOP and POS forms with an example. 4

- (ii) Convert the following : 6

- (1) SOP to POS

$$F(A, B, C) = \Sigma(0, 2, 3, 5)$$

- (2) POS to SOP

$$F(A, B, C) = \pi(0, 1, 6, 7)$$

SECTION - III

5. (a) (i) Define combinational logic circuit and list its applications. 5

- (ii) Explain half adder with truth table and logic expressions. 5

- (b) Explain the working of full adder with block diagram, truth table, logic expression and logic diagram. 10

6. (a) (i) List any five differences between serial adder and parallel adder. 5

- (ii) Explain half subtractor with truth table and logic expressions. 5

- (b) Explain the working of 3-bit parallel adder. 10

SECTION - IV

7. (a) (i) Explain 2 : 1 multiplexer with logic expression and truth table. 5

- (ii) Design 4 : 1 multiplexer using 2 : 1 multiplexer. 5

- (b) Explain the working of 4 : 1 multiplexer with block diagram, truth table, Boolean expression and logic diagram. 10

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8. (a) (i) Explain the working of 1 : 2 demultiplexer. 5
 (ii) List any five applications of multiplexer. 5
- (b) (i) Implement the equation $Y = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$ using a suitable multiplexer. 6
 (ii) Realize AND and OR gate using 2 : 1 multiplexer. 4

SECTION - V

9. (a) (i) List the applications of decoder. 5
 (ii) Explain priority encoder. 5
- (b) Explain BCD to 7-segment decoder. 10
10. (a) (i) List the advantages of IC. 5
 (ii) List any five differences between TTL and CMOS. 5
- (b) Define the following : 10
- (i) Fan in
 - (ii) Fan out
 - (iii) Propagation delay
 - (iv) Power dissipation
 - (v) Noise margin
-

Diploma examinations December-2023
Digital Electronics (20EC11T)
Scheme of Evaluation

Subject: Digital Electronics

Subject code: 20EC11T

Special Note: (i) Answer one full question from each section.
(ii) One full question carries 20 marks.

Section-I

- | | |
|--|--------------------|
| Q.1. (a) (i) Any 5 differences each difference carry 1 mark. | 5x1=5 marks |
| (ii) Decimal to binary conversion | 3 marks |
| (iii) Octal to binary conversion | 2 marks |
| Q.1.(b) (i) Any 5 features each feature carry 1 mark. | 5x1=5 marks |
| (ii) Addition operation each step - 01 marks | 3x1=3 marks |
| (iii) Subtraction operation correct answer | 2 marks |
| Q.2.(a) (i) Writing procedure 4 marks+example 1mark | 4+1=5 marks |
| (ii) 1's complement 1M, addition 2M, answer-2M | -----1+2+2 =5marks |
| Q.2.(b) (i) Statement-2 marks+Explanation-3 marks | 2+3=5 marks |
| (ii) Statement - 2 marks + proof- 3 marks (Any one theorem) | 2+3=5 marks |

Section-II

- | | |
|---|------------------------------|
| Q.3.(a) (i) NOT-1 mark+AND-2 marks+OR-2 marks
(ii) List any 5 laws each carries 1 mark | 1+2+2=5 marks
5x1=5 marks |
| Q.3.(b) Definition, Symbol, Truth table of each gate- 2 marks | 5x2=10 marks |
| Q.4.(a) (i) Simplification-3 marks+ Logic diagram-2 marks
(ii) Simplification-3 marks+ Logic diagram-2 marks | 3+2=5 marks
3+2=5 marks |
| Q.4.(b) (i) Definition +example of each-(SOP & POS)
(ii) (1)SOP to POS- 3marks+ (2) POS to SOP-3 marks | 2+2 =4marks
6 marks |

Section-III

- Q.5.(a) (i) Definition -2 marks+ Writing any 3 applications-3 marks 2+3=5 marks**
(ii) Definition-1 mark, Truth table-1 mark, Logic expression-1 mark,logic diagram-2 marks 1+1+1+=5 marks

- Q.5.(b) Full adder explanation-3, Truth table-2, Logic expression-2, Logic diagram-3
3+2+2+3=10 marks

- Q.6.(a) (i) List any 5 differences each carry 1 mark $5 \times 1 = 5$ marks
(ii) Definition-1 mark, Truth table-1 mark, Logic expression-1 mark, logic diagram-2 marks $1+1+1=3$ marks

Q.6.(b) Block diagram-4marks, Explanation with example-6 marks, $4+6=10$ marks

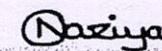
Section-IV

- Q.7.(a) (i) Definition -1 mark, Truth table-1 mark, Logic expression-1 mark, Logic diagram-2 marks $1+1+1+2=5$ marks
(ii) Construction diagram-3 marks +Explanation-2 marks $3+2=5$ marks
- Q.7.(b) Block diagram & explanation -4, Truth table-2, Logic expression-2 marks, Logic diagram-2 marks $4+2+2+2=10$ marks
- Q.8.(a) (i) Definition -1 mark, Truth table-1 mark, Logic expression-1 mark, Logic diagram-2 marks $1+1+1+2=5$ marks
(ii) Listing any 5 applications each carry 1 mark $5 \times 1 = 5$ marks
- Q.8.(b) (i) Writing truth table-2 marks Implementation using 8:1 mux-4 marks $2+4=6$ marks
(ii) Realization of each gate-2 marks $2 \times 2 = 4$ marks

Section-V

- Q.9.(a) (i) Listing any 5 applications each carry 1 mark $5 \times 1 = 5$ marks
(ii) Block diagram & explanation priority encoder-3 marks, Truth table-2 marks $3+2=5$ marks
- Q.9.(b) Block diagram- 3 marks, Explaination-3 marks, Truth table-4 marks $3+3+4=10$ marks
- Q.10.(a) (i) Listing any 5 advantages each carry 1 mark $5 \times 1 = 5$ marks
(ii) Listing any 5 differences each carry 1 mark $5 \times 1 = 5$ marks
- Q.10.(b) Each definition carry 2 marks $5 \times 2 = 10$ marks

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Model AnswersSection-I

1(a). (i) Compare analog signal and digital signal.

5x1=5 marks

Sl.No	Analog signal	Digital signal
1	Analog signal is continuous and time varying.	It is a discrete signal
2	It is denoted by sine waves.	It is denoted by square waves.
3	Easily affected by the noise.	These are stable and less prone to noise
4	Analog signals use continuous values to represent the data	Digital signals use discrete values to represent the data.
5	Accuracy of the analog signals may be affected by noise.	Accuracy of the digital signals are immune from the noise.
6	Analog signals may be affected during data transmission.	Digital signals are not affected during data transmission.
7	Analog signals use more power.	Digital signals use less power.
8	Analog signal bandwidth is low.	Digital signal bandwidth is high.
9	Examples: Temperature sensors, FM radio signals, photo cells etc	Examples: Computers, CDs, DVDs etc

1(a). (ii) Convert decimal number $(27)_{10}$ into binary.

03 marks

$$\begin{array}{r}
 2 \quad | \quad 27 \\
 2 \quad | \quad 13 \quad -1 \\
 2 \quad | \quad 6 \quad -1 \\
 2 \quad | \quad 3 \quad -0 \\
 2 \quad | \quad 1 \quad -1 \\
 0 \quad -1
 \end{array}$$

Therefore, $(25)_{10} = (11011)_2$ 1(a). (iii) Represent octal number $(1574)_8$ in binary.

02 marks

$$\begin{array}{r}
 1 \quad 5 \quad 7 \quad 4 \\
 001 \quad 101 \quad 111 \quad 100
 \end{array}$$

Therefore, $(1574)_8 = (001101111100)_2$

1(b). (i) Mention the features of ASCII code.

5x1=5 marks

- ✓ ASCII is the abbreviation for American Standard Code for Information Interchange.
- ✓ ASCII is a universally accepted alphanumeric code used in most computers and other electronic equipment.
- ✓ Most computer keyboards are standardized with the ASCII.
- ✓ When you enter a letter, a number, or control command, the corresponding ASCII code goes into the computer.
- ✓ ASCII has 128 characters and symbols represented by a 7-bit binary code.
- ✓ The code is divided into two groups of 3 and 4 bits. The first three bits in the code are used to identify whether the remaining four bits represent letters, numerals, or punctuation marks.
- ✓ Actually, ASCII can be considered an 8-bit code with the MSB always 0.
- ✓ This 8-bit code is 00 through 7F in hexadecimal.

- ✓ The first thirty-two ASCII characters are non graphic commands that are never printed or displayed and are used only for control purposes.

1(b). (ii) Add $(5B6)_{16}$ and $(63A)_{16}$.

03 marks

Column 1: $(6)_{16} + (A)_{16} = (10)_{16} = (0)_{16} + \text{carry } 1$ Column 2: $(B)_{16} + (3)_{16} + \text{CY } 1 = (0F)_{16} = (F)_{16} + \text{carry } 0$ Column 3: $(5)_{16} + (6)_{16} + \text{CY } 0 = (0B)_{16} = (B)_{16} + \text{carry } 0$ Therefore, $(5B6)_{16} + (63A)_{16} = (BF0)_{16}$

Note: Any alternative method may be considered , final answer should be in Hexadecimal

1(b). (iii) Subtract $(1010)_2$ from $(1101)_2$.

02 marks

$$\begin{array}{r} 1101 \\ -1010 \\ \hline 0011 \end{array}$$

Therefore, $(1101)_2 - (1010)_2 = (0011)_2$

2(a). (i) Explain the procedure for binary to gray conversion with an example. 05 marks

To perform binary to gray conversion, follow the below mentioned steps

- (1) The MSB of gray code is always equal to the MSB bit of binary code.
- (2) To get the next gray code bit perform the XOR operation between the adjacent pair of binary bits going from left to right.
- (3) Let the binary number be $B_3B_2B_1B_0$ with B_3 being the MSB and B_0 the LSB.
- (4) Let the corresponding Gray code be $G_3G_2G_1G_0$ with G_3 being the MSB and G_0 the LSB.
- (5) G_3 in the Gray code is the same as the corresponding digit B_3 in the binary number.

That is, $G_3 = B_3$

The other bits in the Gray code are given by the following logical expressions:

$$G_2 = B_3 \oplus B_2$$

$$G_1 = B_2 \oplus B_1$$

$$G_0 = B_1 \oplus B_0$$

Example: Convert the binary number $(1001)_2$ into gray code

$$G_3 = 1;$$

$$G_2 = 1 \oplus 0 = 1$$

$$G_1 = 0 \oplus 0 = 0$$

$$G_0 = 0 \oplus 1 = 1$$

Therefore gray equivalent of binary number $(1001)_2 = (1101)_2$

2(a). (ii) Subtract $(1001)_2$ from $(1011)_2$ by using 1's complement method.

05 marks

(a) Find the 1's complement of subtrahend $(1001)_2 = (0110)_2$

(b) Add 1's complement of subtrahend with minuend

$$\begin{array}{r} 1011 \\ + 0110 \\ \hline 10001 \end{array}$$

(c) Add the carry to the LSB result of the result

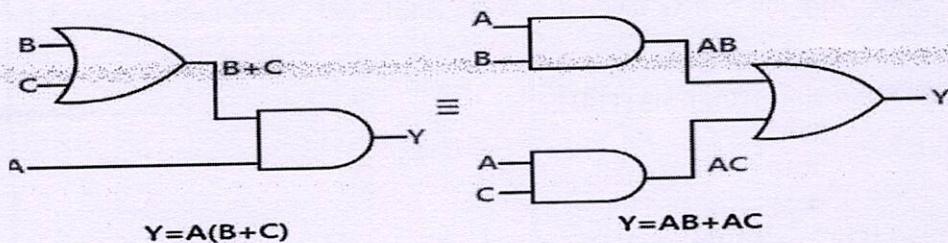
$$\begin{array}{r} 0001 \\ + 1 \\ \hline 0010 \end{array}$$

Therefore, $(1011)_2 - (1001)_2 = (0010)_2$

2(b) (i) Explain distributive law.

The Distributive Law says that multiplying a number by a group of numbers added together is the same as doing each multiplication separately.

$$A(B+C) = AB+AC$$

**Truth table:**

A	B	C	$B+C$	$A(B+C)$	AB	AC	$AB+AC$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

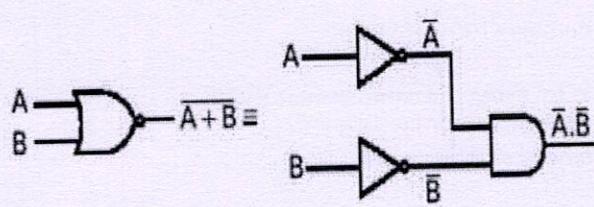
2(b). (ii) State and prove De Morgan's theorem.

(Any one)

05 marks

De Morgan's First Theorem:

"The complement of sum of two variables is equal to the product of the complements of individual variables."



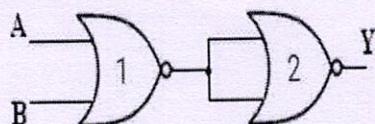
A	B	$\bar{A}+\bar{B}$	$\bar{A}\bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

DeMorgan's first theorem is stated as follows in equation form:

$$\overline{A+B} = \bar{A}\bar{B}$$

3. OR using NOR:

Connect a NOT using NOR, at the output of the NOR to invert it and get AND logic.



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3(a). (ii) List any five laws of Boolean algebra.

05 marks

- 1) Commutative Law: $(A \cdot B) = (B \cdot A)$ or $(A+B) = (B+A)$
- 2) Associative Law: $((A \cdot B) \cdot C) = (A \cdot (B \cdot C))$ or $((A+B)+C) = (A+(B+C))$
- 3) Distributive Law: $(A+(B \cdot C)) = ((A+B) \cdot (A+C))$ or $(A \cdot (B+C)) = ((A \cdot B)+(A \cdot C))$
- 4) Absorption Law: $(B+(B \cdot A)) = (B)$ or $(B \cdot (B+A)) = (B)$
- 5) Identity Law: $(A \cdot 1) = (A)$ or $(A+0) = (A)$
- 6) Null (Annulment) Law: $(B \cdot 0) = (0)$ or $(B+1) = (1)$
- 7) Complement Law: $(B \cdot B') = (0)$ or $(B+B') = (1)$
- 8) Inversion Law: $((A)')' = (A)$

3(b). Write NOT, AND, OR, NAND and NOR gates along with symbol, expression and truth table.

10 marks

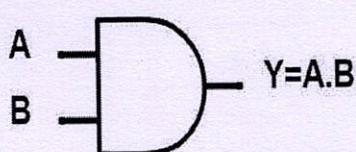
1. NOT Gate

Truth Table

Input		Output
A		Y
0		1
1		0

2. AND Gate

$$Y = A \cdot B$$



Truth table

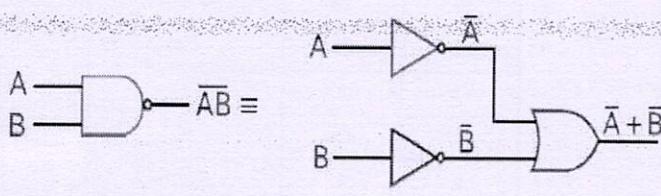
Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

3 OR Gate

$$Y = A + B$$

De Morgan's second theorem:

"The complement of product of two variables is equal to the sum of the complement of individual variables."



A	B	$\bar{A}\bar{B}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

DeMorgan's second theorem is stated as follows in equation form

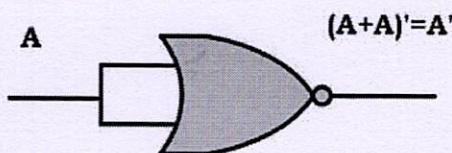
$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

Section-II

- 3(a). (i) Show realization of NOT,AND & OR gates using NOR gates. 05 marks

1. NOT using NOR

It's simple. Just connect both the inputs together.

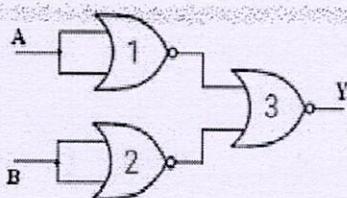


Truth table

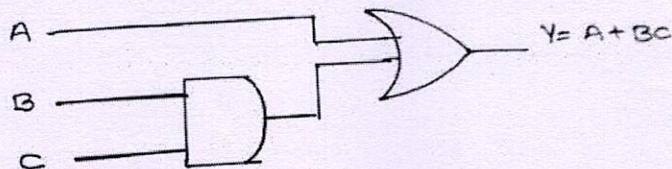
Input	Output
A	Y
0	1
1	0

2. AND using NOR:

Connect two NOT using NORs at the inputs of a NOR gate to get OR logic.



Input		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1



4(a). (ii) Simplify the following Boolean expression using k-map and draw the logic diagram for the simplified expression.

$$F(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC$$

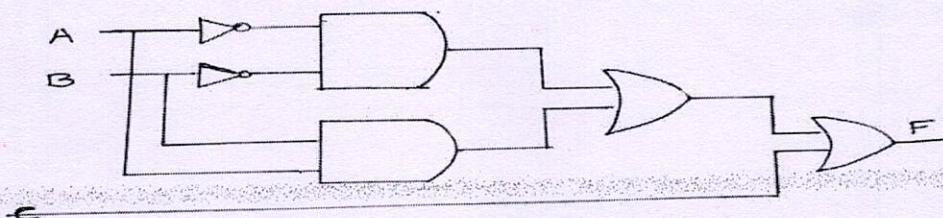
05 marks

K-map:

$\bar{B}\bar{C}$	00	01	11	10
\bar{A}	0	1	1	1
1	1	1	1	1

$$F(A, B, C) = \bar{A}\bar{B} + AB + C$$

Logic diagram:



4(b).(i) Describe SOP and POS forms with an example. 04 marks

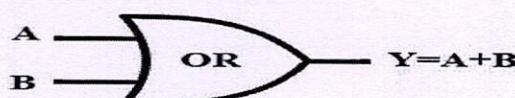
SOP(Sum Of Product)

- It is one of the ways of writing a boolean expression.
- It is formed by adding the product terms.
- The product terms are also called as 'min terms'.
- Min terms are represented with 'm', they are the product(AND operation) of Boolean variables either in normal form or complemented form.

Example: $Y = A'B'C' + A'BC' + ABC$

POS(Product Of Sum)

- It is also one of the ways of writing Boolean expression.
- It is formed by multiplying the sum terms
- The sum terms are also called as max terms.



Inputs		Output
A	B	$\bar{Y} = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

4. NAND Gate

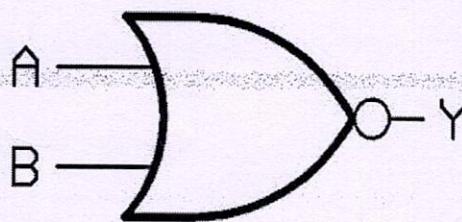
$$Y = (A \cdot B)'$$



Inputs		Output
A	B	$(AB)'$
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate

$$\triangleright Y = A \text{ NOR } B = (A + B)'$$



Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

4(a). (i) Simplify the below expression using Boolean laws and draw the logic diagram for the simplified expression. 05 marks

$$Y = (A + B)(A + C)$$

$$Y = AA + AC + AB + BC$$

$$Y = A + AC + AB + BC$$

$$Y = A(1 + C) + AB + BC$$

$$Y = A + AB + BC$$

$$Y = A(1+B)+BC$$

$$Y = A+BC$$

Logic diagram:

- Max terms are represented with 'M', they are the sum(OR operation) of Boolean variables either in normal form or complemented form.

Example: $Y = (A' + B' + C) \cdot (A + B' + C) \cdot (A' + B + C)$

4(b). (ii) Convert the following

06 marks

(1) SOP to POS

$$F(A, B, C) = \sum(0, 2, 3, 5)$$

(2) POS to SOP

$$F(A, B, C) = \pi(0, 1, 6, 7)$$

(1) SOP to POS conversion $F(A, B, C) = \sum(0, 2, 3, 5)$

Step 1: Change the symbol \sum to $\pi \rightarrow F(A, B, C) = \pi(0, 2, 3, 5)$

Step 2: Write down the indices of missing variables $\rightarrow 1, 4, 6, 7$

$$F(A, B, C) = \pi(1, 4, 6, 7)$$

Step 3: Write the maxterms corresponding to missing variables in step 2

$$\begin{aligned} 1(001) &= A + B + \bar{C}, 4(100) = \bar{A} + B + C, 6(110) = \bar{A} + \bar{B} + C, 7(111) \\ &= \bar{A} + \bar{B} + \bar{C} \end{aligned}$$

Step 4: Final POS form is obtained by AND'ing all maxterms obtained in step 3

$$F(A, B, C) = \pi(1, 4, 6, 7) = (A + B + \bar{C})(\bar{A} + B + C)(\bar{A} + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})$$

(2) POS to SOP conversion $F(A, B, C) = \pi(0, 1, 6, 7)$

Step 1: Change the symbol π to $\sum \rightarrow F(A, B, C) = \sum(0, 1, 6, 7)$

Step 2: Write down the indices of missing variables $\rightarrow 2, 3, 4, 5$

$$F(A, B, C) = \sum(2, 3, 4, 5)$$

Step 3: Write the minterms corresponding to missing variables in step 2

$$2(010) = \bar{A}B\bar{C}, 3(011) = \bar{A}BC, 4(100) = A\bar{B}\bar{C}, 5(101) = A\bar{B}C$$

Step 4: Final POS form is obtained by ORing all minterms obtained in step 3

$$F(A, B, C) = \sum(2, 3, 4, 5) = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C$$

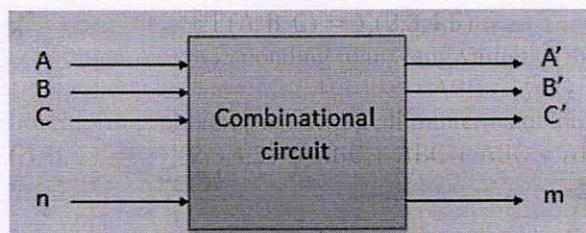
Section-III

5(a).(i) What is combinational logic circuit and list it's applications.

05 marks

Definition: "A combinational logic circuit is the digital logic circuit in which the output depends only on the current value of inputs."

- It does not require any memory.
- It can have an 'n' number of inputs and 'm' number of outputs.



Applications of combinational circuits are

(1) Data processing: Combinational circuits are used in various data processing applications such as data encoding, decoding, and multiplexing.

(2) Code conversion: Combinational circuits can be used to convert data from one code to another, such as binary to Gray code, or BCD to binary.

(3) Arithmetic operations: Combinational circuits can be used to perform arithmetic operations such as addition, subtraction, multiplication, and division.

(4) Logic gates: The basic building blocks of combinational circuits are logic gates such as AND, OR, and NOT gates. These gates are used to implement Boolean functions and perform logical operations.

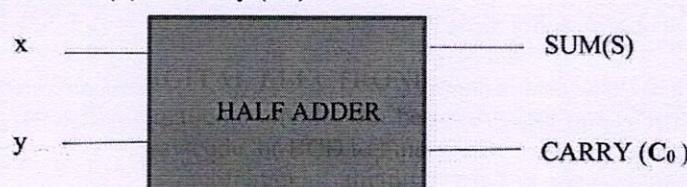
(5) Control systems: Combinational circuits are used in control systems to implement logic functions that control the behavior of the system.

Examples: Adders, Subtractors, Encoders, Decoders & Multiplexers etc...

5(a). (ii) Explain half adder with truth table and logic expressions.

05 marks

"Half Adder is a combinational circuit that adds two binary digits (addend and augend) to produce sum (S) and carry (C_0)."



Truth table:

INPUTS		OUTPUTS	
x	y	C_0	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Logic expression:

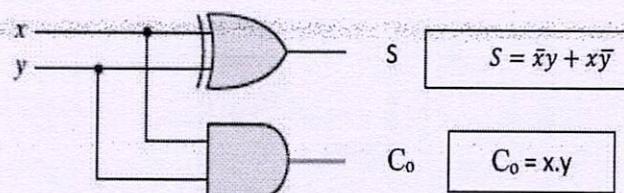
From the above truth table, the simplified Boolean functions

$$S = \bar{x}y + x\bar{y} = x \oplus y$$

$$C_0 = xy$$

Therefore, S can be implemented using an EX -OR and C_0 can be implemented using AND gate.

Logic diagram:



5(b). Explain the working of full adder with block diagram, truth table, logic expression, and logic diagram.

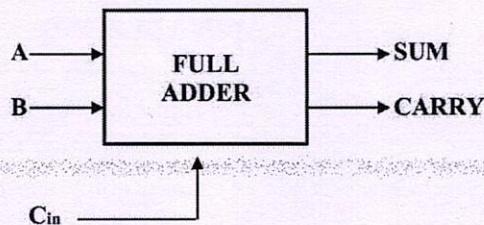
10 marks

"A Full Adder is a combinational arithmetic logic circuit that performs addition of three binary digits and generates two outputs. It is used for adding two input bits and an input carry and generates a sum and carry output."

➤ The two inputs are taken as A and B, they represent the two significant bits to be added.

The third input C_{in} , represents the carry from the previous Lower Significant Bit (LSB) position.

➤ Figure below shows the block diagram of full adder.



Truth Table:

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

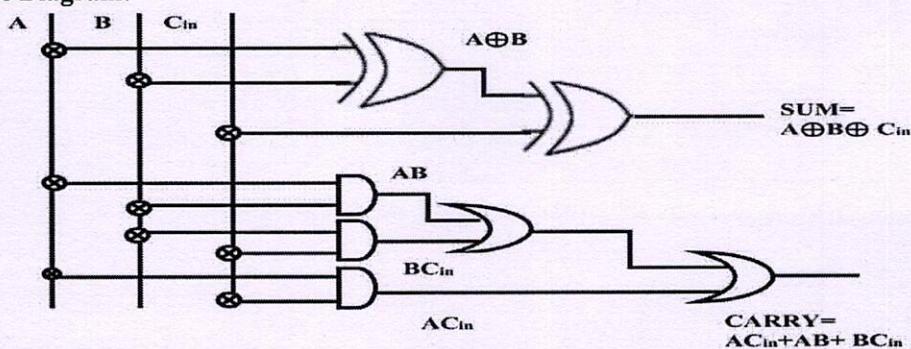
Logic Expression:

From the above truth table, the simplified Boolean functions

$$\text{SUM} = A \oplus B \oplus C_{in}$$

$$\text{CARRY} = AC_{in} + AB + BC_{in}$$

Logic Diagram:



Note: Any other relevant logic diagram may be considered

6(a). (i) List any five differences between serial adder and parallel adder. 05 marks

Sl.No	Serial Adder	Parallel Adder
1	It is used to add two binary numbers in serial form.	It is used to add two binary numbers in parallel form.
2	It uses shift registers.	It uses registers with parallel loads.
3	It requires single full adder.	It requires multiple full adders.
4	It is a sequential circuit.	It is a combinational circuit.
5	The propagation delay is more	The propagation delay is less.
6	It requires less components.	It requires more components.
7	It is slow in operation.	It is fast in operation.
8	The number of required full adders is fixed i.e. one.	The number of required full adders is equal to the number of bits in the binary number
9	Time required for addition depend on the number of bits.	Time required for addition does not depend on the number of bits.
10	Addition is performed bit by bit starting from the LSB.	All the bits are added simultaneously.

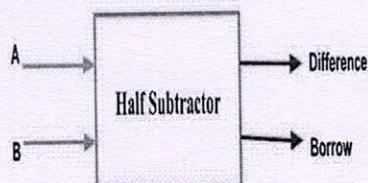
6(a). (ii) Explain half subtractor with truth table and logic expressions.

05 marks

“Half subtractor is a combinational circuit that can be used to subtract one binary digit from another to produce a DIFFERENCE output and a BORROW output.”

- The BORROW output here specifies whether a ‘1’ has been borrowed to perform the subtraction.

Block diagram



Truth table

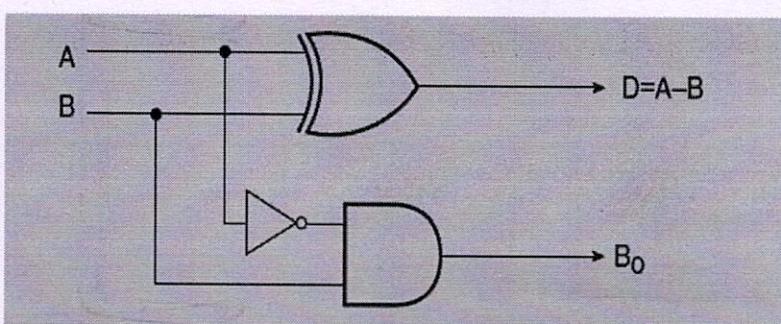
Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The Boolean expressions for the two outputs are given by the equations

$$D = \overline{A} \cdot B + A \cdot \overline{B}$$

$$B_o = \overline{A} \cdot B$$

Logic diagram

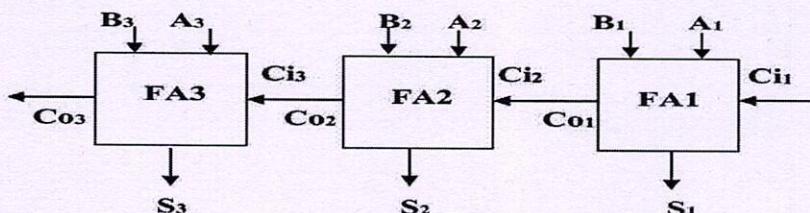


6(b). Explain the working of 3 bit parallel adder

10 marks

- (i) A binary parallel adder is a digital circuit that produces the arithmetic sum of two binary numbers in parallel.
- (ii) It consists of full adders connected in a chain, with the output carry from each full adder connected to the input carry of next full adder in the chain.
- (iii) Thus several full adders are connected to form adders that add several bits at one time.
- (iv) A three bit parallel adder consists of three full adders, with the output carry from each full adder connected to the input carry of next full adder in the chain.

Block diagram:



Working of 3-bit parallel Adder:

- As shown in the above figure, the first full adder FA1 adds A1 and B1 along with the carry Ci1 to generate the sum S1 (the first bit of the output sum) and the carry Co1 which is connected to the next adder in chain.
- The second full adder FA2 uses this carry bit as an input carry bit Ci2 to add with the input bits A2 and B2 to generate the sum S2(the second bit of the output sum) and the carry Co2 which is again further connected to the next adder in chain.
- The third full adder FA3 uses this carry bit as an input carry bit Ci3 to add with the input bits A3 and B3 to generate the sum S3(the third bit of the output sum) and the carry Co3 .

Truth Table:

Inputs							Outputs			
A3	A2	A1	B3	B2	B1	Ci1	Cout	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	1	0	1	1	0	0	1	1	0
1	0	0	1	0	0	1	1	0	0	1
1	0	1	1	0	1	1	1	0	1	1

1	1	0	1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1

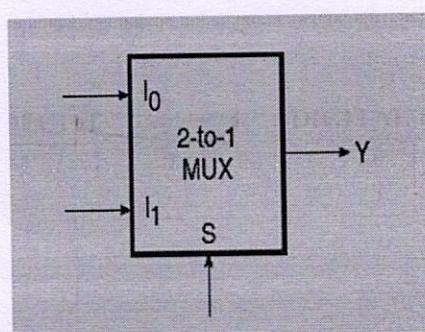
Section-IV

7(a). (i) Explain 2:1 multiplexer with logic expression and truth table. **05 marks**

“A 2:1 MUX is a combinational logic circuit with 2 input lines, one output line and one selection line.”

Depending on the input, the output is connected to either of the inputs.

Block diagram:



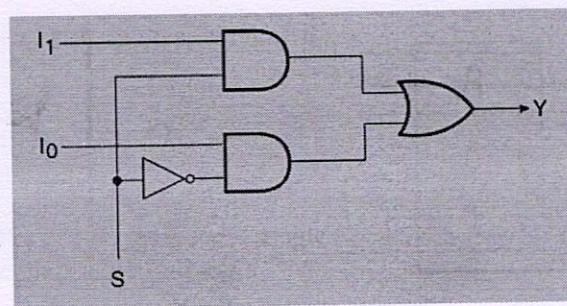
Truth table:

S	Y
0	I0
1	I1

expression:

$$Y = \bar{S} \cdot I_0 + S \cdot I_1$$

Logic diagram:

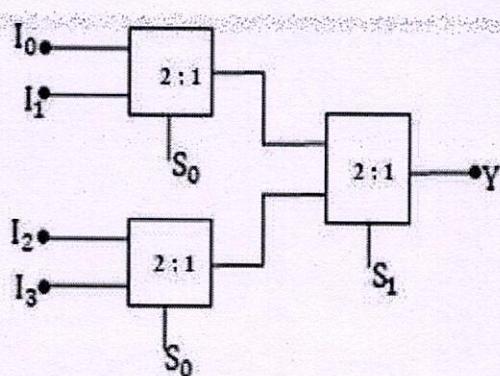


7(a)(ii). Design 4:1 multiplexer using 2:1 multiplexer. **05 marks**

(i) The 2x1 Multiplexer has 2 data inputs, 1 selection lines and one output. Whereas, 4x1 Multiplexer has 4 data inputs, 2 selection lines and one output.

(ii) So, we require two 2x1 Multiplexers in first stage to get the 4 data inputs. Since, each 2x1 Multiplexer produces one output, we require a 2x1 Multiplexer in second stage by considering the outputs of first stage as inputs and to produce the final output.

(iii) Let the 4x1 Multiplexer has four data inputs I0 to I3, two selection lines S1 & S0 and one output Y.



Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

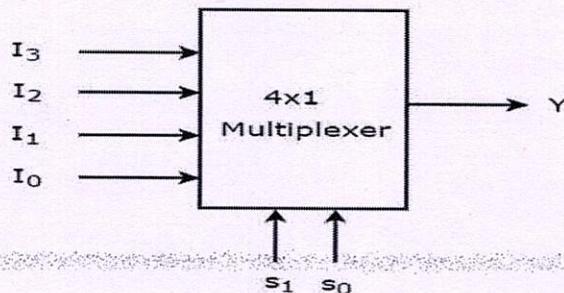
7(b). Explain the working of 4:1 multiplexer with block diagram, truth table, boolean expression and logic diagram.

10 marks

4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0 , two selection lines s_1 & s_0 and one output Y .

- One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines.
- If $S_1=0$ and $S_0=0$ then $Y=I_0$.
- If $S_1=0$ and $S_0=1$ then $Y=I_1$.
- If $S_1=1$ and $S_0=0$ then $Y=I_2$.
- If $S_1=1$ and $S_0=1$ then $Y=I_3$.

Block diagram:



Truth table:

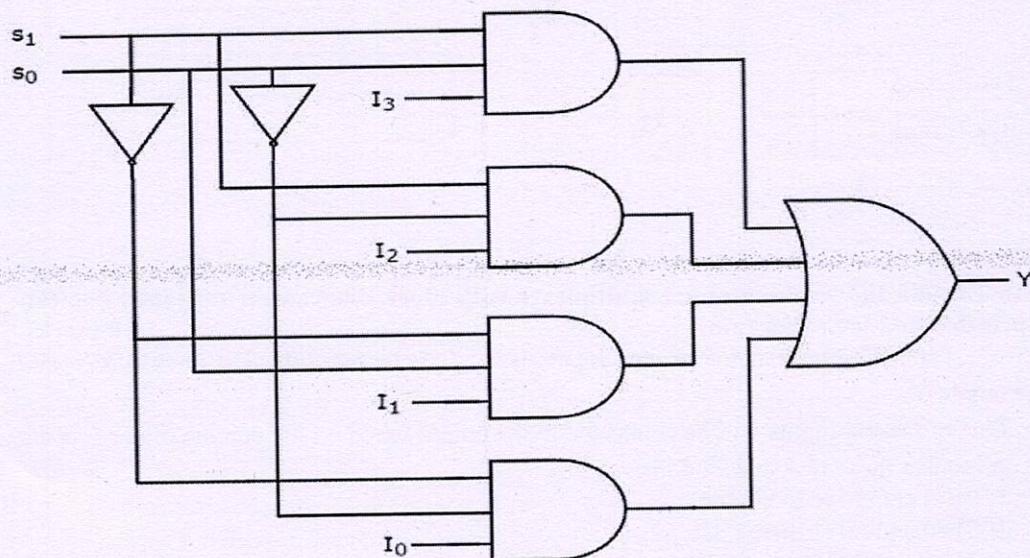
Inputs		Output
S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

From Truth table, we can directly write the Boolean function for output, Y as

$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

- We can implement this Boolean function using Inverters, AND gates & OR gate.

Logic diagram:

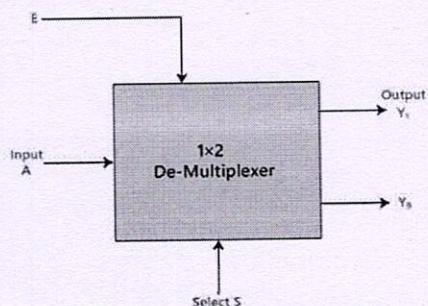


8(a)(i). Explain the working of 1:2 demultiplexer. 05 marks

Definition: It is a combinational logic circuit which has only 1 input line and 1 select line and 2 output lines..

- In the 1 to 2 De-multiplexer, there are only two outputs, i.e., Y_0 , and Y_1 , 1 selection lines, i.e., S_0 , and single input, i.e., A .
- On the basis of the selection value, the input will be connected to one of the outputs

Block Diagram:



Truth Table:

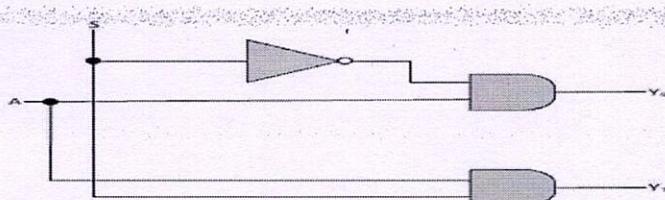
INPUTS		Output	
S_0		Y_1	Y_0
0		0	A
1		A	0

Logic expression:

$$Y_0 = S_0' \cdot A$$

$$Y_1 = S_0 \cdot A$$

Logic diagram:



8(a).(ii) List any five applications of multiplexer.

05 marks

Applications:

- Communication systems
- Computer memory
- Telephone Network
- Transmission from the Computer System of a Satellite
- Data Routing
- Logic Function Generator
- Parallel to Serial Conversion
- Operation sequencing

Note: Any other general application may be considered

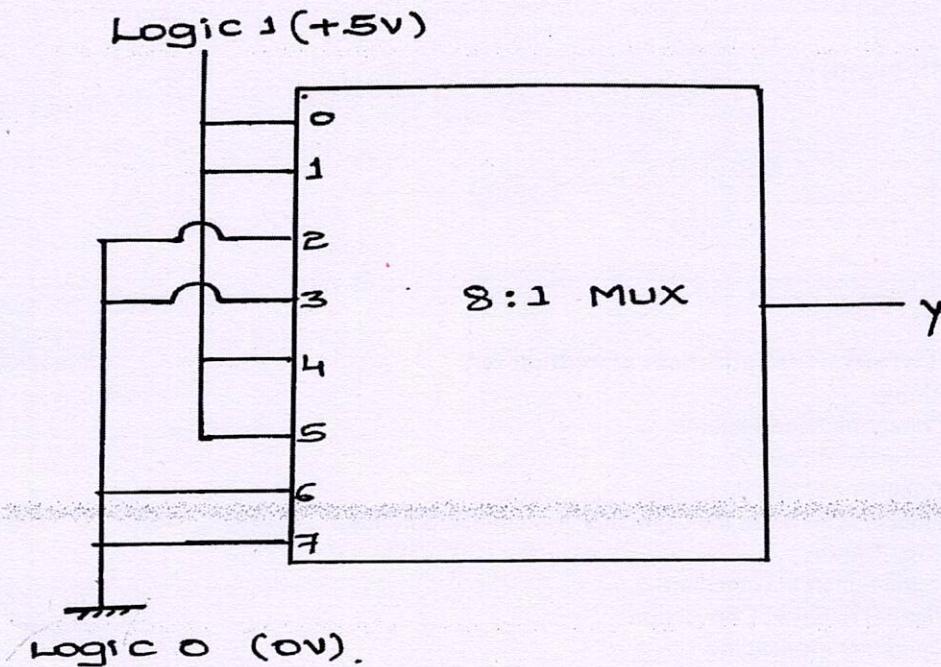
8(b)(i) Implement the equation $Y = A'B'C + A'B'C' + AB'C + AB'C'$ using a suitable multiplexer.

Using 8:1 Mux:

- There are 3 variables in the given expression, hence $2^n = 2^3 = 8 : 1$ multiplexer. So, the mux has 8 input lines, 3 selection lines, and one output.
- The inputs, corresponding to the minterms (0,1,4,5) are connected to logic 1 and the remaining terms to logic 0(grounded). The given input variables are connected as three selection lines.

Truth table

INPUTS			OUTPUT
S2	S1	S0	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



Section-V

9(a)(i). List the applications of decoder.

05 marks

Applications:

- (1) Decoders are used for code conversions.
- (2) Decoders are used in microprocessor memory systems for selecting different banks of memory.
- (3) Decoders are also used for de-multiplexing or data distribution.
- (4) Decoders are also used in data routing applications where very short propagation delay is required.
- (5) Decoder may also be used for timing or sequencing purposes.
- (6) Decoders are also utilized to turn on and off digital devices at a specific time.
- (7) Decoders are used in memory chips for enabling different rows of memory depending on address.

9(a).(ii) Explain priority encoder.

05 marks

- The priority encoder solves the drawback of normal encoder by allocating a priority level to each input.
- Its output corresponds to the currently active input which has the highest priority.
- When an input with a highest priority is present, all other inputs with a lower priority will be ignored.

Example: 4:2 priority encoder

- It has 4 inputs D0 to D3 and 2 outputs Y0 and Y1.

The IC is stand alone and requires no external components other than the LED current limiting resistors.

The display used here must be a common anode type because the IC has active low outputs.

Truth Table:

Decimal Digit	Input Lines				Output Lines								Display pattern
	D	C	B	A	a	b	c	d	e	f	g	dp	
0	0	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	0	1	1	0	0	1	1	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0	1	2
3	0	0	1	1	0	0	0	0	1	1	0	1	3
4	0	1	0	0	1	0	0	1	1	0	0	1	4
5	0	1	0	1	0	1	0	0	1	0	0	1	5
6	0	1	1	0	0	1	0	0	0	0	0	1	6
7	0	1	1	1	0	0	0	1	1	1	1	1	7
8	1	0	0	0	0	0	0	0	0	0	0	1	8
9	1	0	0	1	0	0	0	0	1	0	0	1	9

10(a). (i) List the advantages of IC.

05 marks

Some of the advantages of ICs are as follows

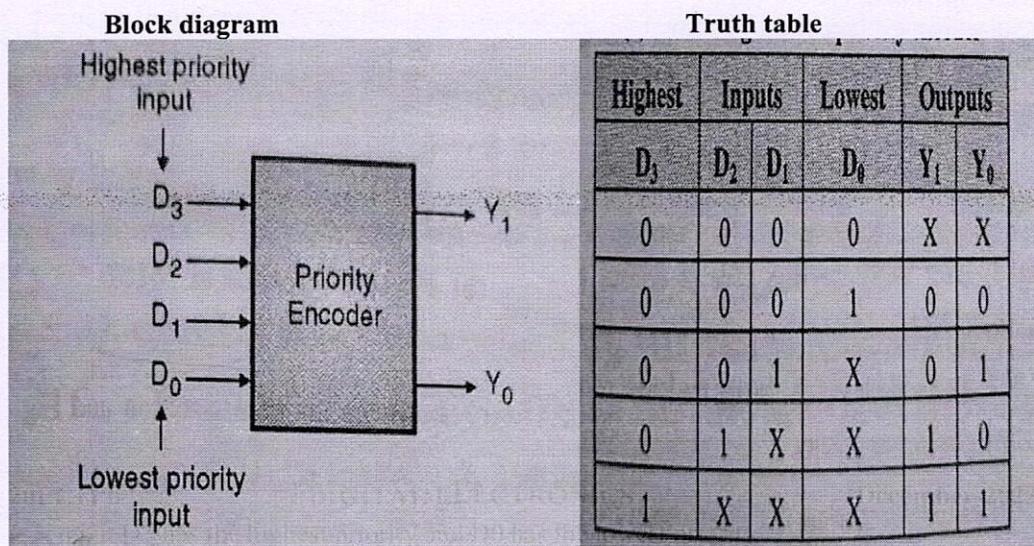
- (1) Extremely small in size.
- (2) Low power consumption.
- (3) High reliability and ruggedness
- (4) Improved performance.
- (5) Reduced cost.
- (6) Versatility.
- (7) Easy replacement.
- (8) Increased operating speed.
- (9) Less vulnerability to parameter variation.
- (10) Easy troubleshooting.
- (11) High integration density

10(a). (ii) List any 5 differences between TTL and CMOS.

05 marks

Sl.No	TTL	CMOS
1	It stands for transistor logic.	It stands for complementary metal oxide semiconductor.
2	It has low noise immunity.	It has high noise immunity.
3	It typically operates at 5V.	It typically operates at 5V or 3.3V.
4	It consumes more power.	It consumes less power.
5	It uses BJTs	It uses MOSFETs
6	It has low fan out capability.	It has high fan out capability.
7	TTL chips do not have CMOS logic.	There are CMOS chips that have TTL logic and are meant as replacements for TTL chips.
8	The propagation delays of TTL are usually 10nS.	The propagation delays for the CMOS lies between 20 to 50nS

- Input D3 has the highest priority and D0 has the lowest priority.



9(b). Explain BCD to 7-segment decoder.

10 marks

Seven segment decoder is a digital circuit that can decode a digital input to the seven-segment format and simultaneously drive a 7-segment LED display using the decoded information.

BCD to 7-segment decoder is used to convert a BCD or a binary code into a 7 segment code. It has 4 input lines and 7 output lines.

Block diagram:

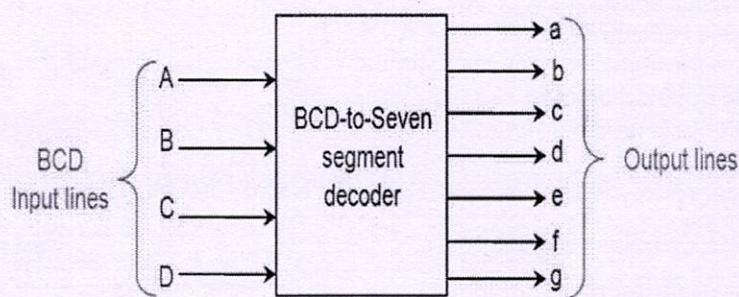


Fig 1. BCD-to-seven segment decoder

IC 7447 BCD-to-seven segment Decoder

IC 7447 is a BCD -to- seven segment Decoder which translates the 8421 BCD code to a code that lights the proper segments on the common -anode seven-segment LED display.

IC 7447 is one such IC with active low outputs.

Seven segment displays make use of segments, and each segment contains and the seven LED are labeled from a to g.

The digits from 0 to 9 can be displayed by forward biasing the different LEDs.

9	TTL components are less expensive.	CMOS components are more expensive.
10	TTL circuits draw more power.	CMOS circuits draw less power.
11	It is complex and costlier design.	It is simpler and cheaper design.
12	TTL components are less susceptible to damage from electrostatic discharge.	CMOS components are more susceptible to damage from electrostatic discharge.

10(b). Define the following:**10 marks**

- (i) Fan in
- (ii) Fan out
- (iii) Propagation delay
- (iv) Power dissipation
- (v) Noise margin

(i) Fan in:

It is defined as the number of inputs connected to the gate without any degradation in the voltage level..

(ii) Fan out:

It is defined as the maximum number of the inputs of the same IC family that a gate can drive without falling outside the specified voltage limits.

➢ Higher the fan out higher is the current supplying capacity of the gate.

(iii) Propagation delay:

It is defined as time delay between the instant application of an input pulse and the instant of occurrence of the corresponding output pulse.

➢ It is expressed in ns

(vi) Power dissipation:

It is defined as the measure of power consumed by the gate when fully driven by all its inputs.

(v) Noise margin

It is defined as the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output..

Certificate

"I certify that the model answer script that is prepared by me for the subject code 20EC11T (DIGITAL ELECTRONICS) are from the prescribed text books and model answer script and scheme of valuation prepared by me are correct"

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