1ST SEMESTER DIPLOMA EXAMINATION, AUGUST/SEPTEMBER-2022

FUNDAMENTALS OF COMPUTER- **20CS11T**)

SCHEME OF VALUATION

i) Answer one full question from each section

ii) One full question carries 20marks

SECTION -I

1. a. Listing any 3 features of number system - (**3*1=3m),** List any 2 number system with an example **(2*1=2m)**

   b. Statement of any one demorgan's law -**1m,** proof using truth table- **4m**

   c. Finding 2's complement of minuend - **(2m)** + perform addition –**(2m)** + result- **(1m)**

   d. Definition of an Universal Gate -**1m,** diagram -**3m** explanation -**1m**

2. a. Meaning of Logic Gate -**2m,** 3 Logic gates and their symbol- **(3*1=3m)**

   b. *Because of the more length of solution*, **consider Any two solutions (2.5*2=5m)**

   c. Finding Excess 3 code- **3m**, BCD code-**2m***(exclude ASCII)*

   d. Truth table-**5m**. (based on columns and their correctness marks may be allotted)

SECTION -II

3. a. Solving the Expression - **5m**

   b.Definition/understanding of Flipflop-**1m**, Listing types of flipflops-**2m**, Any 2 applications-**2m**

   c. Any five difference between Combinational and Differential circuits- **(5*1=5m)**

   d. Diagram of 4:2 encoder- **2m**, Truth table -**3m**

4. a.i) finding 1's complement- **2m** ii) finding 2's complement – **3m**

   b. Definition/Understanding of Shift register -**1m.** Listing types-**2m**, Any 2 applications-**2m**

   c. Comparator circuit diagram -**3m**, Truth table-**2m**

   d. Drawing a clock signal-**1m**, Indicating or explaining each term – (**4*1=4m)**

SECTION -III

5. a. Drawing Full adder circuit – **3m**, Write Sum AND Carry expression-**2m**

   b. Solving problem -**5m**

   c. 4 applications – (**4*1=4m)**

   d. Diagram -**3m**, working Explanation -**3m**

6.a. Drawing Full Subtractor circuit – **3m**, Difference and Borrow expression-**2m**

   b. i-1m ii-1m iii-1m iV-2m **(1+1+1+2=5m)**

   c. Each generation 2 features- (**4*1=4m)**

d. Any 3 comparisons/ differences –**(3*2=6m)**

SECTION -IV

7.a. Identifying and listing any 3 security threats during browsing – **(3*2=6m)**, any 2 counter measures **-2m**

b. Drawing functional units **-3m**, explanation- **3m**

c. Listing or drawing Flynn's classification – **2m**, 1Feature of each class – (**4*1=4m**)

8. a. i) category of networking **-2m**

ii) Networking devices – **3m**

iii) Drawing topology **-3m**

b. Arranging the memory in hierarchy **-3m,** any 3 applications-**3m**

c. BIOS features **-2m** , 4 differences between BIOS and UEFI –**(4*1=4m)**

SECTION -V

9. a. 4 differences between Mobile OS and Computer OS – (**4*1=4m)**

b. 5 variable naming rules – **(5*1=5m)**

c. flowchart **-4m**

d. algorithm **-7m(** based on algorithm structure and understanding, marks may be awarded)

10. a. any 4 Comparisons **-4m**

b. 5 symbols–**(5*1=5m)**

c. Algorithm **-4m**

d. Flowchart **-7m**(based on symbols and understanding marks may be awarded)

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FUNDAMENTALS OF COMPUTER- **20CS11T**)

Model Answer

Note : i) Answer one full question from each section

ii) One full question carries 20marks

SECTION – I

1) a) Any **Three** features of Number Systems: **(3*1=3m)**

i) The number system is the system of naming or representing numbers for indicating Quantities

ii) Each numeral system is characterized by its base.

iii) The numeral systems have a base or set of symbols that allow to represent the different numeral quantities.

iv) Each element within the numeral system has a weighted value based on its position.

v) The number 0 expresses or denotes the absence of a given quantity.

vi) We may perform arithmetic operations on numbers of number system

List any **two** number systems with **example(2*1=2m)**

i) Binary ii) Octal iii)Decimal iv) Hexadecimal

b) i) Demorgan's First law: $\overline{A.B} = \bar{A} + \bar{B}$ **(1m)**

Proof using TruthTable: **(4m)**

A	B	$\bar{A}$	$\bar{B}$	A·B	$\overline{A \cdot B}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

(or)

ii) Demorgan's Second law: $\overline{A + B} = \bar{A}.\bar{B}$ **(1m)**

Proof using Truth Table: **(4m)**

A	B	$\bar{A}$	$\bar{B}$	A+B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

c) Given to perform $1101_{(2)}$-$1001_{(2)}$ using 2's complement method

Step 1: find 2's complement of subtrahend **(2m)**

Subtrahend is: 1001_2
Its 1's complement: 0110_2
2's complement is: 0111_2

Step2: Add above 2's complement to minuend: **(2m)**

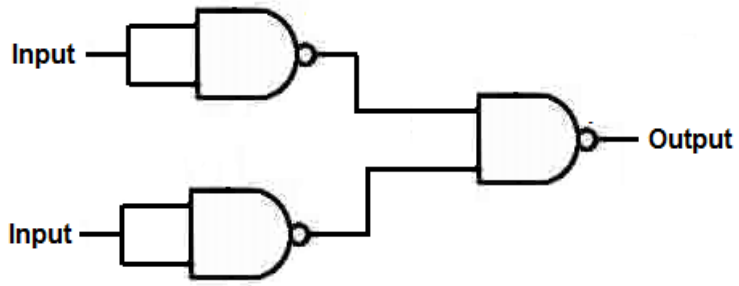
Minuened: 1101_2
2's c of subtrahend: 0111_2
Sum: 10100_2

Step 3: Since we got carry bit 1, we discard it and answer is positive **(1m)**

Result is: **0100_2** //(i.e in decimal 13-9=4)

d) NAND is called as Universal gate, because we can obtain all the basic gates like OR, AND etc using multiple NAND gates. **(1m)**

OR gate using NAND gates (3m)

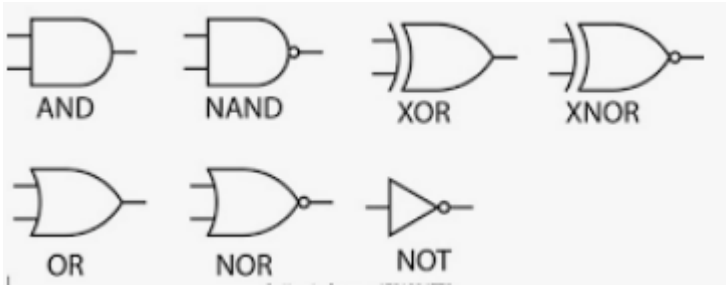


Explanation:**(1m)**
Using 3 NAND gates we can Obtain OR gate, when connected as above diagram. Inputs to 2 NAND 's are to be shorted and their output are to be input to third NAND gate to get **OR** output

2. a)Logic Gate: (2m)

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Example: AND gate, OR gate.

Logic gates and their symbols (any 3): (3*1=3m)



b) Answer any 2 out of 3 **(2.5*2=5m)**

i) 999 $_{(10)}$ to Octal:

Divide 999 by 8 as below:

999/8=124 with remainder 7
124 / 8 = 15 with remainder 4
15 / 8 = 1 with remainder 7
1 / 8 = 0 with remainder 1

Rewrite the remainders from bottom to top. **Result: $1747_{(8)}$**

ii) $10101111_{(2)}$ to Hexadecimal

First, convert 10101111_2 into decimal as below:

$10101111_{(2)} = 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$
$= 175_{10}$

Now convert 175_{10} to hexadecimal as below:

175 / 16 = 10 with remainder 15 (F)
10 / 16 = 0 with remainder 10 (A)

Result is: $AF_{(16)}$

iii) First, convert 123.77_8 into decimal, by using above steps:
$= 1 \times 8^2 + 2 \times 8^1 + 3 \times 8^0 + 7 \times 8^{-1} + 7 \times 8^{-2}$
$= 83.984375_{10}$

Now, we have to convert 83.984375_{10} to binary

83 / 2 = 41 with remainder 1
41 / 2 = 20 with remainder 1
20 / 2 = 10 with remainder 0
10 / 2 = 5 with remainder 0
5 / 2 = 2 with remainder 1
2 / 2 = 1 with remainder 0
1 / 2 = 0 with remainder 1
83 = 1010011 ------- (1)
0.984375 × 2 = 1 + 0.96875
0.96875 × 2 = 1 + 0.9375
0.9375 × 2 = 1 + 0.875
0.875 × 2 = 1 + 0.75
0.75 × 2 = 1 + 0.5
0.5 × 2 = 1 + 0

0.984375 = 0.111111------- (2)

Result: **$1010011.111111_{(2)}$**

c) Given: $149_{(10)}$

i) EXCESS3 code: **(3m)**

1	4	9
+3	+3	+3
=4	=7	=12
0100	0111	1100

Result: **010001111100**

ii) BCD code: **(2m)**

1	4	9
0001	0100	1001

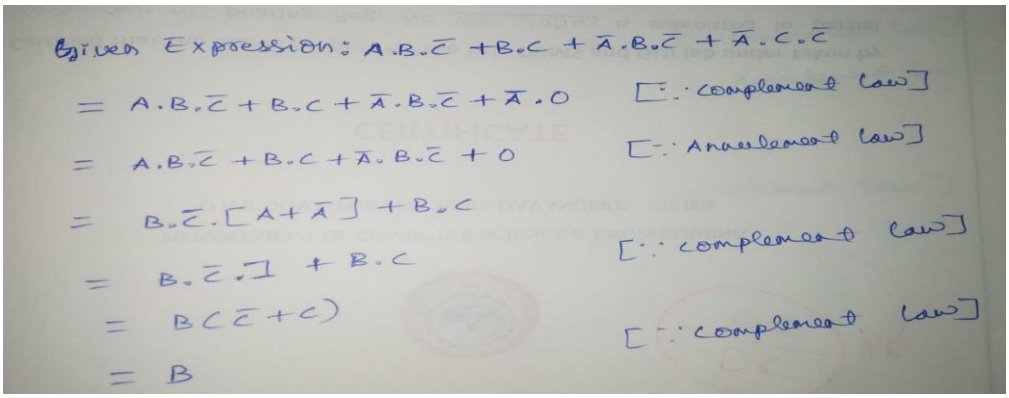
Result:**000101001001**

d) To Verify LHS is equal to RHS for the equation, the truth table is as below: ***(award marks based on the correctness of colums and values)***

A	B	$A+B$	$\bar{A}$	$\bar{A}.B$	$A+\bar{A}.B$
0	0	0	1	0	0
0	1	1	1	1	1
1	0	1	0	0	1
1	1	1	0	0	1

SECTION II

3. a) Simplify the given expression: **(5m)**



b) A flip flop is an electronic circuit used to store binary data. The stored data can be changed by applying varying inputs. **(1m)**

<u>Types of flip flops</u>: (2m)

i. RS Flip Flop
ii. JK Flip Flop
iii. D Flip Flop
iv. T Flip Flop

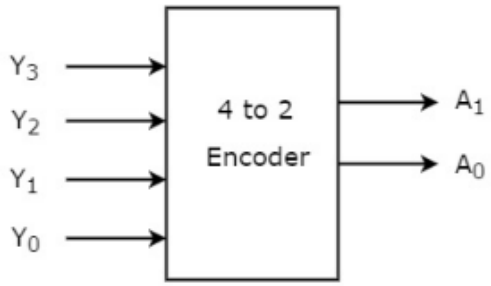
<u>Applications</u> (any 2 of the below): **(2m)**

Counters, Storage registers, Shift registers, Data storage, Bounce elimination switch, Latch, Data transfer, Registers

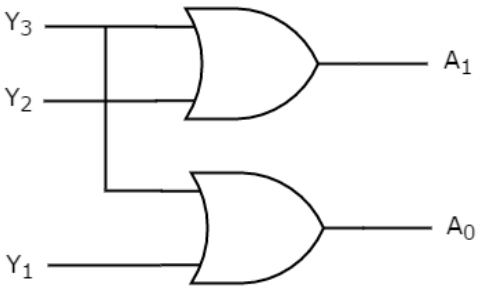
c) Any five differences: **(5*1=5m)**

Combinational Circuit	Sequential Circuit
1. Depends upon the present input only	1. Depends upon present input as well as past input
2. Combinational circuit is time-independent and it is very fast in operation	2. Sequential circuit is time-dependent and comparatively slower in operation
3. There is no feedback path between output and input	3. There is a feedback path available between output and input
4. The main elementary building block of a combinational circuit is basic logic gate	4. The elementary building block of a sequential circuit is the flip flop
5. The combinational circuits are mainly used for arithmetic and boolean operations	5. The sequential logic circuits are used for data storing
6. The operation of a combinational circuit is very simple	6. The operation of a sequential circuit is very complex
7. The combinational circuit does not need any external triggering so they are clock independent	7. The sequential circuits require external triggering means they are clock dependent

d) 4:2 encoder circuit: (2m)



(OR)



Truth table: (3m)

Inputs				Outputs	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

4. a) i) To find 1's complement of $01011_{(2)}$**(2m)**

Convert 1 to zero and zero to one

0 1 0 1 1

1's c: 1 0 1 0 0

Result: $10100_{(2)}$

ii) To find 2's complement of $11011_{(2)}$ **(3m)**

-Find 1's complement :

1 1 0 1 1

1's c: 0 0 1 0 0

-Add 1 to 1's complement

0 0 1 0 0

+1

0 0 1 0 1

Result: $00101_{(2)}$

b) <u>SHIFT REGISTER</u>: A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another is known as **Shift Register**. **(1m)**

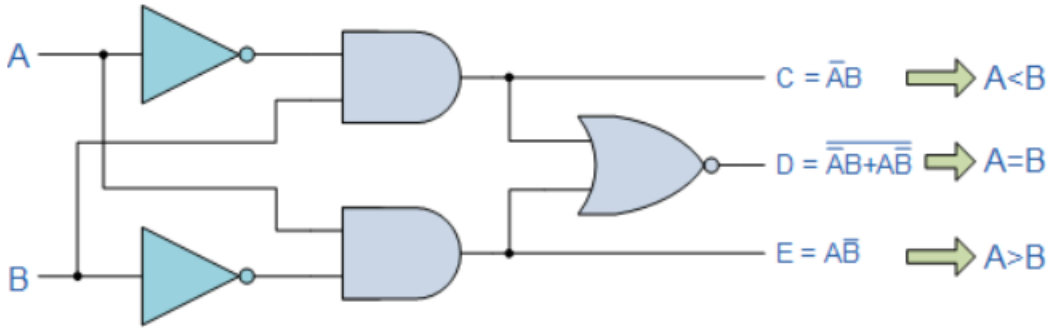
Types of Shift registers: (2m)

- Serial In Serial Out (SISO)
- Serial In Parallel Out (SIPO)
- Parallel In Serial Out (PISO)
- Parallel In Parallel Out (PIPO)

Applications (any 2): **(2m)**

- Parallel to serial conversion
- IO expansion for microcontrollers
- To induce Time delay
- In sequential devices

c) Comparator circuit : (3m)



Truth Table: (2m)

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

d)

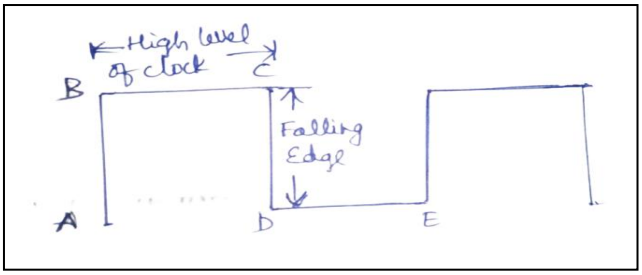


Fig: Digital clock cycle **(1m)**

(1mark for each bilow bits)

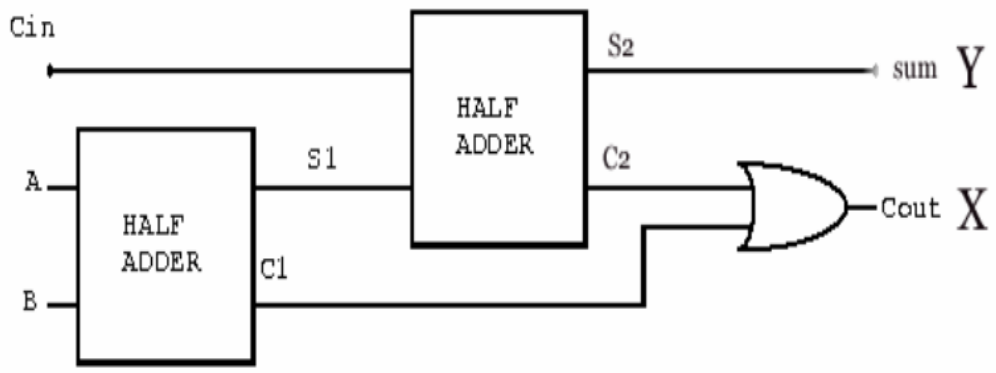
i. **Clock frequency**: clock frequency (F) is the number of clock cycles per second.

ii. **Clock period**: clock period is the time duration of a Clock cycle (or) Inverse of clock frequency. It is equal to 1/F

iii. **Falling edge of clock:** the line of the clock that connects a High-point towards the low-point. Ex: the edge **CD** in above diagram

iv. **High -level of clock**: the duration of the clock signal for which it stays at High level. Ex: the edge **BC** in above diagram

5. a) **Diagram**: (**3m)**



Sum, X= (A ⊕ B) ⊕C_{in}(1m)

Carry, Y= A.B + C_{in}.(A ⊕ B) (1m)

b) Given: Nibble means 4 bits to be transferred, N=4bits

Clock cycle time period, T=5 milliSeconds

For N bits time needed to shift data using SISO shift register = (2N-1)*T

= (2*4-1)*5

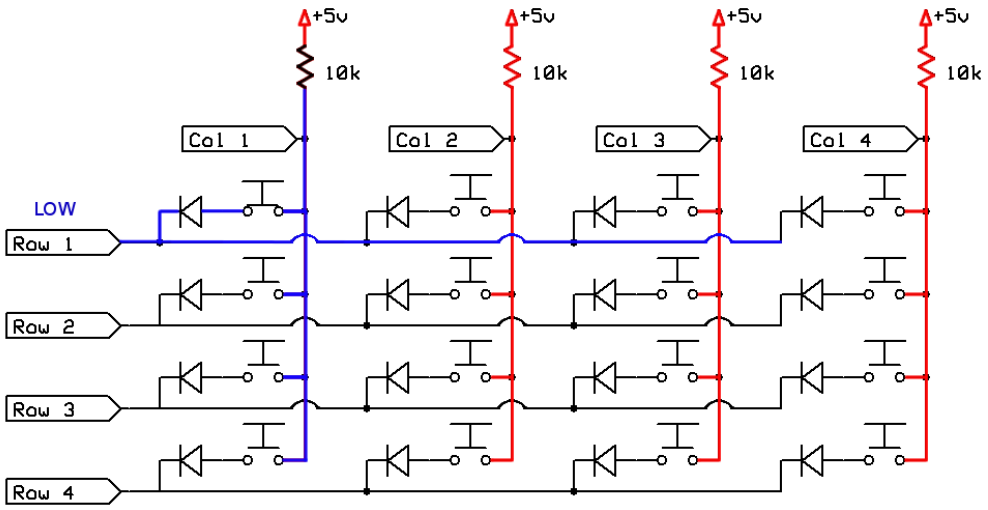
= 35 milliSeconds (5M)

c) Applications of computer: (any 4)**(4*1=4m)**

- Business
- Education
- Marketing
- Banking
- Insurance
- Communication
- Health Care
- Military
- Engineering Design

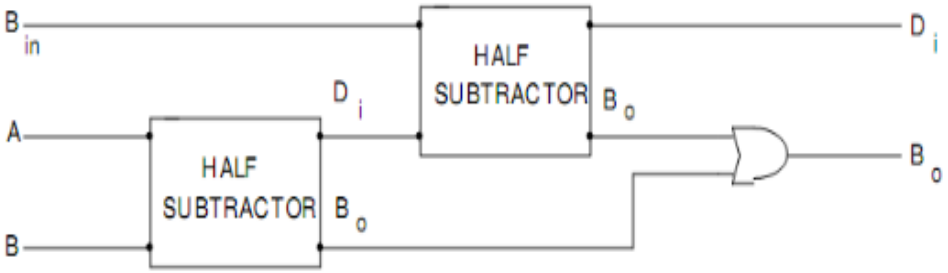
(any other relevant answer conveying the meaning may be awarded marks)

d) A keyboard has own processor and circuitry that carries information to and from that processor. A large part of this circuitry makes up the key matrix.A keyboard contains many push-buttons called "keys". When one of these are pushed, an electrical circuit is closed, and the keyboard sends a signal to the computer that tells it what letter, number or symbol it would like to be shown on the screen. **(2m)**



(***Any other diagram conveying above mechanism may be awarded marks)*****(3m)**

6. a) **Diagram** – **(3m)**



Difference, D = (A ⊕ B) ⊕ B_{in} **(1m)**

Borrow, B_o= A'B+ A'.B_{in}+B.B_{in} **(1m)**

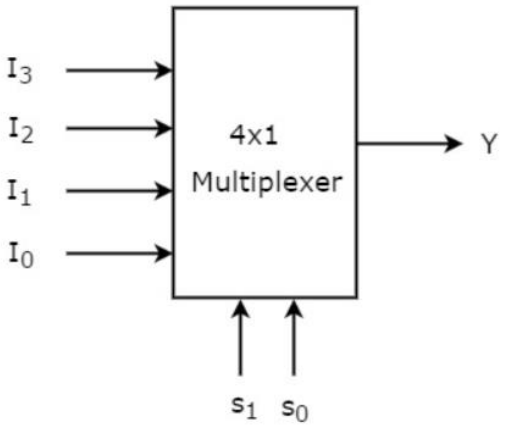
b) b) Given is 4:1 multiplexer:

i. 4 inputs are given **(1m)**

ii. 1 output taken **(1m)**

iii. Select lines selects one of the multiple inputs and connect it to the Output**(1m)**

iv. **(2m)**



c) **Any 2 features** of each generation **(4m)**

Generation of computers	**Features**
1st Generation (1946-1959)	Vacuum tube technology, Supported machine language only, Very costly, Generated a lot of heat, Huge size, Non-portable, Consumed a lot of electricity
2nd Generation (1959-1965)	Use of transistors, Supported machine and assembly languages, Reliable and Smaller size as compared to first generation computers, produced less heat as compared to first generation
3rd Generation (1965-1971)	IC used, Supported high-level language, More reliable and faster in comparison to previous two generations
4th Generation (1971-1980)	VLSI technology used, Pipeline processing, Very cheap, Portable and reliable, Very small size
5th Generation (1980 onwards)	ULSI technology, Development of true artificial intelligence & Natural language processing, Advancement in Superconductor technology, powerful computers at cheaper rates

d) Any three differences (3*2=6)

LAN	MAN	WAN
LAN stands for Local Area Network.	MAN stands for Metropolitan Area Network.	WAN stands for Wide area network.
LAN's ownership is private.	MAN's ownership can be private or public.	While WAN also might not be owned by one organization.
The transmission speed of LAN is high.	While the transmission speed of MAN is average.	Whereas the transmission speed of WAN is low.
The propagation delay is short in LAN.	There is moderate propagation delay in MAN.	Whereas there is long propagation delay.
There is less congestion in LAN.	While there is more congestion in MAN.	Whereas there is more congestion than MAN in WAN.
LAN's design and maintenance is easy.	While MAN's design and maintenance is difficult than LAN.	WAN's design and maintenance is also difficult than LAN as well MAN.
There is more fault tolerance in LAN.	While there is less fault tolerance.	In WAN, there is also less fault tolerance.
Used in College, School, Hospital.	Used in Small towns, City.	Used in Country/Continent.
Allows Single pair of devices to communicate.	Allows Multiple computers can simultaneously interact.	Allows A huge group of computers communicate at the same time.

SECTION IV

7. a) Security threats on unsecured website (**any three**): **(3*2=6m)**

i. Phishing attacks – Users may be trapped into fake sites that look similar to genuine sites. Cyber criminals may convince / force users to provide sensitive data like banking details, password etc.

ii. Use of unsecure protocols. Ex: HTTP instead of HTTPS for secure communications

iii. Ransomware attack – User's sensitive data is encrypted. But it will be decrypted only after paying money to attacker

iv. Online File editing sites may misuse our uploaded data. When we upload our files say our images or videos, they may be misused by them without user's consent.

v. User may be prompted to download Malwares, virus, Trojans etc through attractive/catchy links

Drive in downloads – where without user's notice virus, spyware may get installed on user's computer

vi. Denial of service attack – Here user may be denied of service he requested because of flooding of requests by botnet

vii. Honey traps

Measures to deal with security threats (**any 2**) : **(2*1=2m)**

i. Keeping the software and systems updated

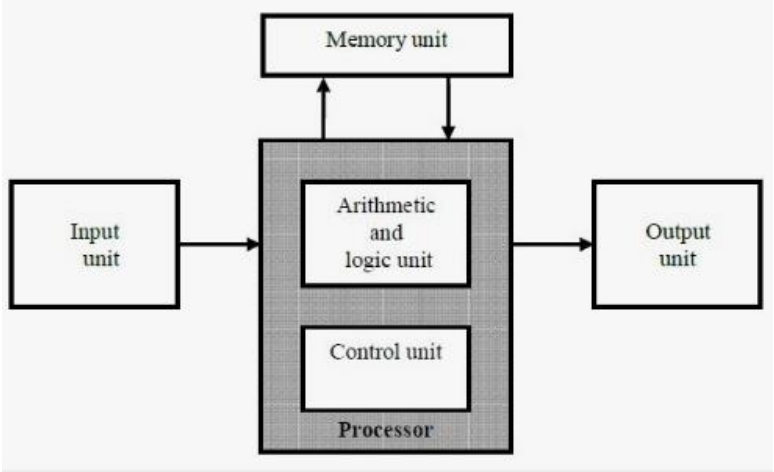
ii. Using secure communication protocols

iii. Installing and properly configuring Firewalls

iv. awareness/educate to distinguish between original vs fake sites

(Any other appropriate correct answers may be awarded marks)

b) Diagram of Functional units of a Computer: **(3m)**



Explanation:(3m)

Various Functional units of computer are:

i.**Input Unit:** Data or Instructions to a computer is input using any Input device. Commonly used input devices are Keyboard, Mouse, Joystick, scanner etc.

ii.**Central Processing Unit(CPU):** CPU- also known as brain of computer, is constituted of Arithmetic and Logic Unit(ALU) and Control Unit(CU).

ALU is responsible for performing all the Arithmetic like addition, subtraction etc and Logical operations like AND, OR etc. The intermediate results are stored on temporary storage called the Registers.

CU controls and coordinates all the processes being executed on the computer. It generates the timing signal responsible to which all the processes are synchronized.

iii**.Memory Unit**: Memory unit store the programs and the data on which the instructions of programs operate. Instructions are fetch from memory, executed on CPU and result is stored back to memory.

iv.**Output Unit**: This unit renders the output to the users. Commonly used output devices are Monitor, Printer, Speaker etc.

c) Flynn's classification of computers: (**Listing or Table) - (2m)**

	Single Data	Multiple Data
Single Instruction	SISD	SIMD
Multiple Instruction	MISD	MIMD

Features: any two each **(4*1=4m)**

i. **SISD** (Single Instruction Single Data): Instructions are executed sequentially, Von Neumann Architecture based, Single CPU computer,

ii. **SIMD** (Single Instruction Multiple Data): includes many processing units under the supervision of a common control unit, Vectors processors, Parallel Processing

iii. **MISD** (Multiple Instruction Single Data): multiple processing units operate on one single-data stream,May be pipelined, Theoretical model only (not practically used)

iv. **MIMD** (Multiple Instruction Multiple Data): Multiple processors in a parallel computer execute different instructions and operate on various data at the same time, Multiprocessing, Ex: Cray T90, Cray T3E, IBM-SP2

8. a) i. **Categoty of networking: (2m)**

-Local Area Network (LAN) have to be setup separately for each department.

-All LANs are connected to Wide Area Network(WAN) through a router

ii. **Networking devices needed:(3m)**

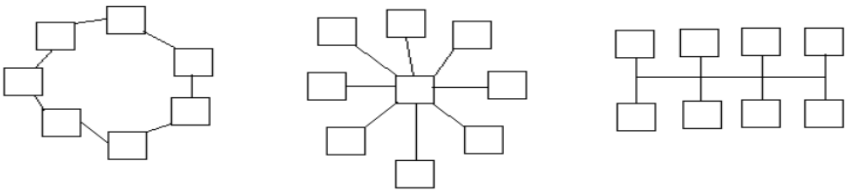
-Each department needs an **Ethernet switch** of 64ports or a **Wireless Switch**

-A **Router** to which all the Switches are connected

-LAN cable(cat5/6) as per the requirement

iii. **Topology (3m)**

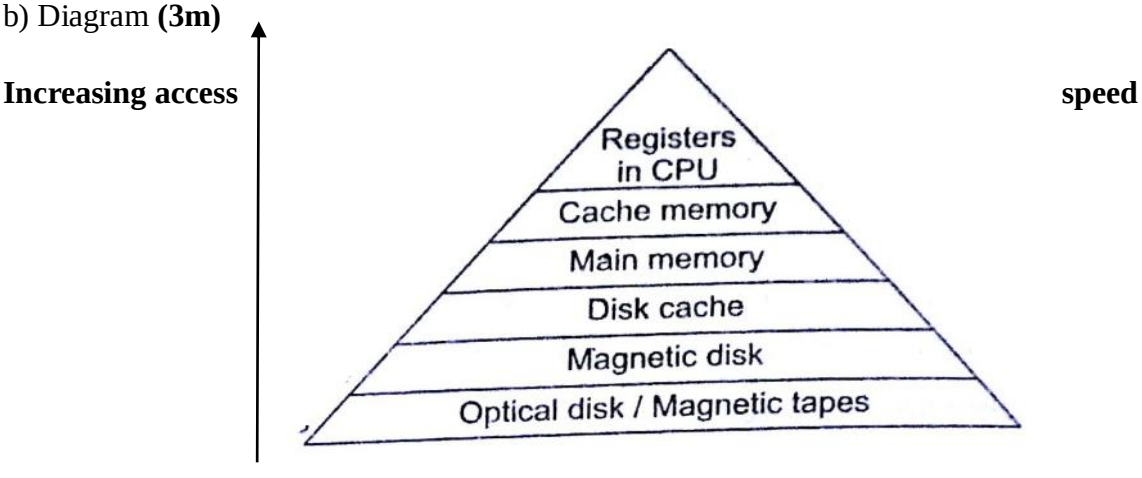
-In every department all the 50 systems may be connected to LAN using either Bus topology, Star Topology or Ring Topology **(any one).**



-All the LAN switches are connected to Router in Star topology

(Any other answer if Justified may be awarded marks accordingly)

b) Diagram **(3m)**



Applications(any 3):(3m)

Registers: Used in CPU to store intermediate result

Cache memory: used to increase speed of access

Main memory: It is the addressable memory by the CPU. All the instructions and data are stored here before loaded toc cpu.

Disk cache: Part of hard disk, used as cache memory to increase disk access speed

Magnetic disk / tape: Large storage devices, used for permanent/persistent storage of data

c) **BIOS (any two features)**:(**2m**)

- BIOS refers to Basic Input/Output system

- It is embedded on EPROM, BIOS is set of instruction responsible for booting of the Computer

- Runs through Power On Self Test (POST) process.

- Configuration of Booting and Hardware may be done through BIOS

Differnces (**any 4**) - **(4*1=4m)**

BIOS	**UEFI**
BIOS refers to Basic Input/Output system	UEFI refers to Unified Extensible Firmware Interface
It works on 16bit mode	Supports 32bit and 64bit mode
Uses MBR (Master boot record) to save information about hard drive	Uses GPT (GUID Partition Table)) to save information about hard drive
BIOS doesn't support GUI	UEFI supports GUI
Hard disk drive is limited to maximum size of 2TB	Hard disk Drive may of size larger than 2TB
Require more boot time than UEFI	Booting takes less time than in BIOS
Less secure	More secure than BIOS

SECTION V

9. a) Any 4 differences- (4*1=4m)

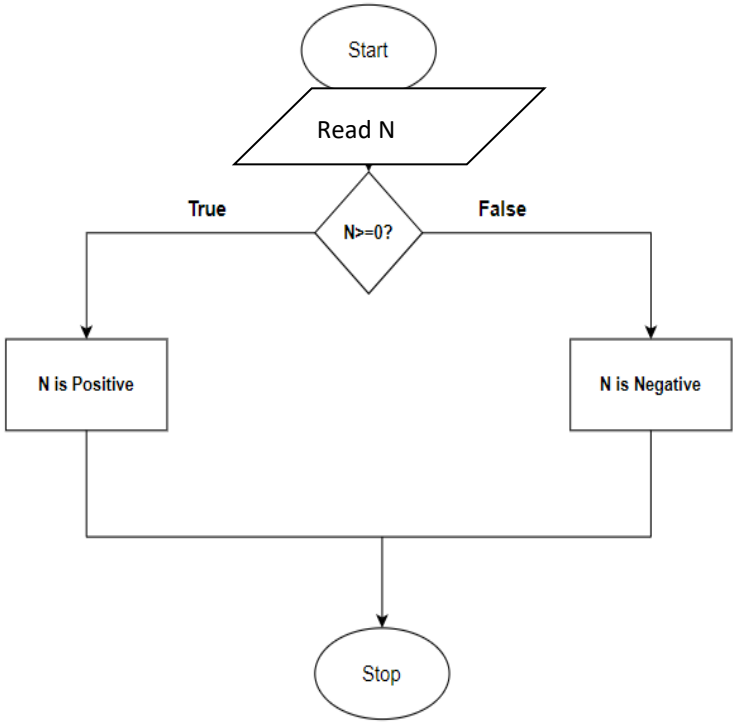
Mobile OS	**Computer OS**
Mobile OS helps and supports to run application software on mobile devices	Computer OS allows user to run their applications on Computer
Mobile OS is simple and lightweight compared to Computer OS (small in size)	Computer OS is complex and heavy weight compared to Mobile OS (large in size)
Supports less number of functionalities/ services	Supports large number of functionalities/ services
Boot time is lesser than Computer OS	Boot time is more than Mobile OS
Applications are designed to consume less	No such restrictions imposed on the applications

memory and space	
Ex: Android, Bada, Blackberry OS, iOS etc	Ex: Windows 10, Mac, Redhatetc

b) Variable Naming rules in programming language **(any 5): (5*1=5m)**

I. Variable name must begin with a letter, dollar sign ($) or an underscore (_):
II. You cannot use reserve words to name variables
III. variable are case sensitive:
IV. Special symbols except underscore are not allowed in variable name
V. Multiple consecutive underscores are not allowed
VI. Variable name should be meaningful, such that it describes the value
VII. Space is not allowed within a variable

c) **(4m)**



d) ALGORITHM :**(7m)**

STEP 1: Start

STEP 2: Insert ATM card and enter PIN

STEP 3: IF login is successful THEN

IF Operation is ACCOUNT BALANCE THEN

display Account BALANCE

ELIF Operation is PRINT STATEMENT THEN

print Mini statement

ELIF Operation is WITHDRAW CASH THEN

ask user to enter amount

WITHDRAW amount

ELSE

Print 'Unsuccessful login'

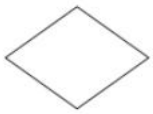
STEP 5: Stop

(ANY OTHER SUITABLE ASSUMPTIONS AND DEEMED TO BE CORRECT MAY BE AWARDED MARKS)

10. a) a) Any 4 difference **(4*1=4m)**

Multiprocessing	**Multiprocessing**
It is a mechanism provided using multiple processors	This mechanism doesn't need multiple processors
Multiple processes are run on multiple processors	Multiple programs are kept in main memory at a time.
Does not ensure the better CPU utilization as multiple processors may sit idle.	Ensures better CPU utilization, as processor runs another program when ongoing process is halted
Uses concept of Parallel processing	Uses concept of Context-switching
Not cost effective	Cost effective
Ex: In a quad-core processor 4 processes may run paralelly.	Ex: More than one program residing in RAM

b) any 5 symbols: (5m)

Flowchart Symbol	Symbol Name
	Terminal (Start or Stop)
	Flow Lines or Arrow
	Input / Output
	Process
	Decision
	Connector
	Annotation

c) ALGORITHM :**(4m)**

STEP 1: START

STEP 2: Read an integer value from user, say N

STEP 3: IF N%2== 0 THEN

Print "N is an Even number"

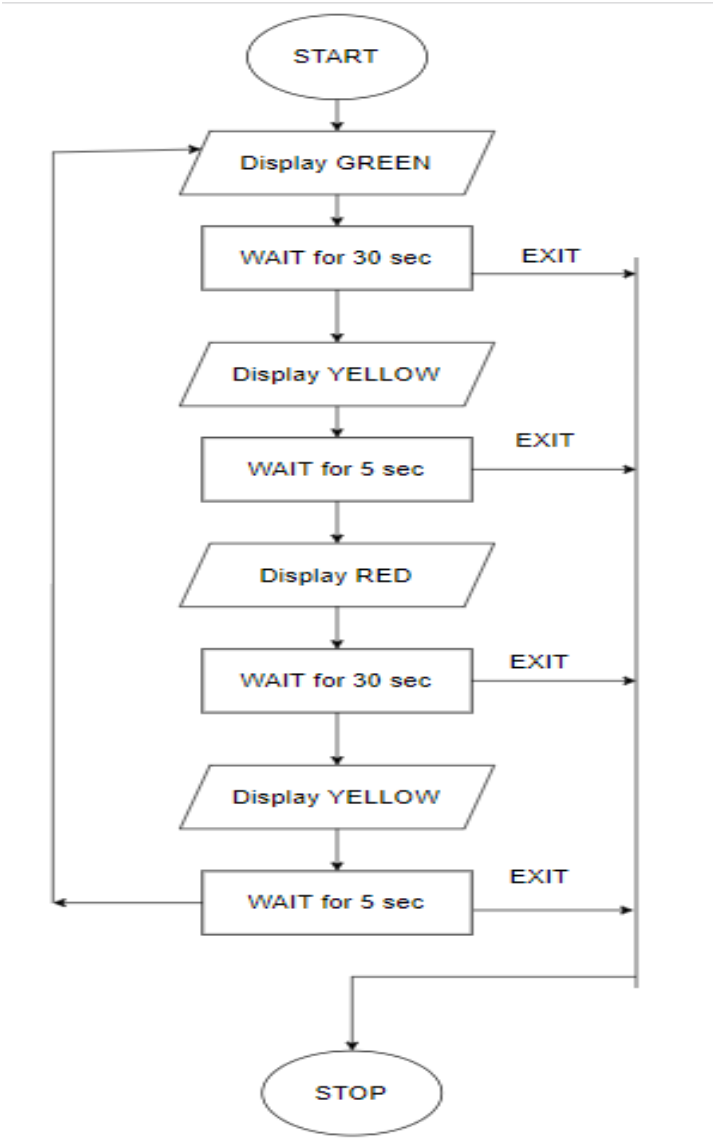
ELSE

Print "N is an Odd Number"

ENDIF

STEP 4: END

d) Flowchart: **(7m)**



(Any Other Suitable Assumptions and found To Be Correct May Be Awarded Marks Accordingly)

Certificate

This is to certify that all the answers pertaining to the subject Fundamentals of Computers (20CS11T) are borrowed from the prescribed text book specified in the syllabus copy.

AKKASALI NEELAKANTACHARI
Lecturer in CSE. DRR Govt. Polytechnic,
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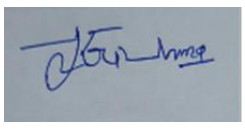
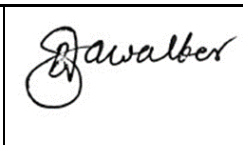
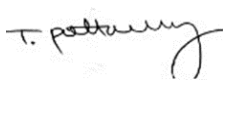
Board Members:

Sd/-

				
Krishna M D	Sharmila D	BharatKumar V S	Puttaswamy T	Usha D