3480 **Code : 20EC11T**

Register Number | | | | | | | | | | |

I Semester Diploma Examination, April/May-2021

DIGITAL ELECTRONICS

Time : 3 Hours] **[Max. Marks : 100**

Instructions : (1) Answer **one** full question from each Section.
(2) **One** full question carries **20** marks.

SECTION – I

1. (a) Perform the following operations : **10**
   (i) Convert Decimal 928 into Hexadecimal.
   (ii) Convert Hexadecimal 7 AC.39 to the Binary.
   (iii) Subtract $(1101)_2$ from $(1111)_2$ using 1's complement method.

   (b) (i) Write a note on ASCII code. **4**
   (ii) Write the procedure for conversion from Binary to Gray code with an example. **6**

2. (a) (i) Add $(AB8)_{16}$ and $(1F5)_{16}$ **10**
   (ii) Add $(654)_8$ and $(236)_8$
   (iii) Convert $(110111.11)_2$ into decimal.

   (b) (i) Define logic gate. Write symbol and TT of AND and XOR gates. **5**
   (ii) List the laws of Boolean algebra. **5**

SECTION – II

3. (a) State and prove DeMorgan's theorems. **10**

   (b) Simplify logic expressions using Boolean algebra. Draw the logic diagram. **10**
   (i) $Y = (A + B)(A + \bar{B})(\bar{A} + B)$
   (ii) $Y = ABCD + AB\bar{C}D + \bar{A}BCD$

4. (a) Define the following : **10**
   (i) K-map
   (ii) Product term
   (iii) Sum term
   (iv) S.O.P.
   (v) P.O.S.

   (b) Simplification of Boolean expression using K-map. Draw the logic diagram. **10**
   $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C}D + ABCD.$

SECTION – III

5. (a) (i) Explain half subtractor with truth table. **5**
   (ii) Write the comparison between serial and parallel adder. **5**

   (b) Explain working of a full adder with logic diagram and truth table. **10**

6. (a) Explain working of a 3 bit parallel adder circuit. **10**
   (b) Explain two bit magnitude comparator with truth table and gate level circuit. **10**

SECTION – IV

7. (a) (i) Define Multiplexer and list the applications. **5**
   (ii) Define Demultiplexer. Explain the operation of 1 : 4 demultiplexer. **5**

   (b) Explain the working of 8 : 1 multiplexer with logic circuit, symbol and truth table. **10**

8. (a) Explain operation of 1 : 16 demultiplexer. **10**
   (b) (i) List the advantages and disadvantages of ICs. **5**
   (ii) Classify IC's based on scale of integration. **5**

SECTION – V

9. (a) Sketch and explain logic circuit of BCD to decimal decoder. **10**
   (b) Explain priority encoder, with a neat logic diagram and truth table. **10**

10. (a) Explain the working of decimal to BCD encoder. **10**
   (b) (i) Compare features of Standard TTL, CMOS and ECL. **5**
   (ii) Describe the interfacing between TTL and CMOS. **5**

I Semester Diploma Examinations, Aug- 2021

DIGITAL ELECTRONICS

Code: 20EC11T **Scheme of Valuation and Rubrics**

Q. NO	MAX MARKS	SCHEME	
1 a)	10M	i) Conversion Decimal to Hex	4M
		ii) Conversion Hex to Binary	4M
		iii) One's complimentary subtraction	2M
b)	10M	i) ASCII stands for	1M
		Features	3M
		Applications	1M
		ii)Conversion Binary to Gray code procedure	4M
		Examples	1M
2 a)	10M	i) Add numbers with base	4M
		ii) Add numbers with base	4M
		iii) convert binary into decimal	2M
b)	10M	i)Definition of logic gate	1M
		Symbol	2M
		Truth table	2M
		ii) I Law	2M
		II Law	2M
		III Law	1M
SECTION -II			
	10M	Statement (each)	2x2=4M
		Expression (each)	1x2=2M
		Truth table (each)	2x2=4M
b)	10M	i)simplification	3M
		Logic diagram	2M
		ii) simplification	3M
		logic diagram	2M
4 a)	10M		
		Definition of each term(2M)	2X5=10M
b)	10M	4 variable k map	2M
		plotting variables on a k map	2M
		Grouping	2M
		simplified expression	2M
		Logic diagram	2M
SECTION-III			
5 a)	10M	i)Definition with block diagram	1M
		Truth table	2M
		Logic diagram	1M
		explanation	1M
		ii)Each comparison	1X5=5M
b)	10M	Definition with block diagram	3M
		Truth table	2M

		Logic expression	2M
		Logic diagram	3M
6 a)	10M	Definition with block diagram	4M
		expression	2M
		explanation	4M
b)	10M	Definition with block diagram	2M
		Truth table	2M
		Logic expression	2M
		Logic diagram	2M
		explanation	2M
		SECTION-IV	
7 a)	10M	i)Definition	1M
		Each applications	1X4=4M
		ii) Definition	1M
		Truth table	1M
		Logic diagram	2M
		Explanation	1M
b)	10M	Block diagram	2M
		Truth table	2M
		Logic diagram	4M
		explanation	2M
8 a)	10M	Block diagram	2M
		Truth table	2M
		Logic diagram	4M
		explanation	2M
b)	10M	i) Each advantages	1/2x5=2.5M
		Disadvantages	1/2x5=2.5M
		ii) Each classification	1X5=5M

SECTION-V

9 a)	10M	Definition with block diagram	2M
		Truth table	2M
		Logic expression	2M
		Logic diagram	2M
		explanation	2M
b)	10M	Definition with Block Diagram	2M
		Truth Table, Logic Diagram, Explanation	2+4+2=8M
10 a)	10M	Block diagram	2M
		Truth table	3M
		Logic diagram	3M
		explanation	2M
b)	10M	i) Each comparison	1X5=5M
		ii) Diagram	2M
		explanation	3M

Scheme of Valuation: April/May-2021

Diploma Examination, April/May-2021

Subject Title**: Digital Electronics (20EC11T)** Time: 3 Hrs

Semester: 1 Max. Marks: 100

SECTION-I

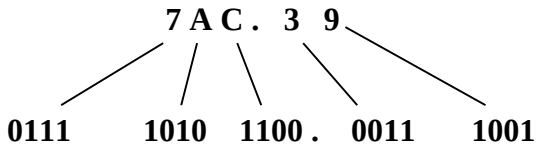
1. a) Perform the following Operations **10Marks**

i) Convert Decimal 928 into Hexadecimal
(Conversion Decimal to Hex-04M)

16	928
16	58 ----- 0
	3 ------ 10(A)

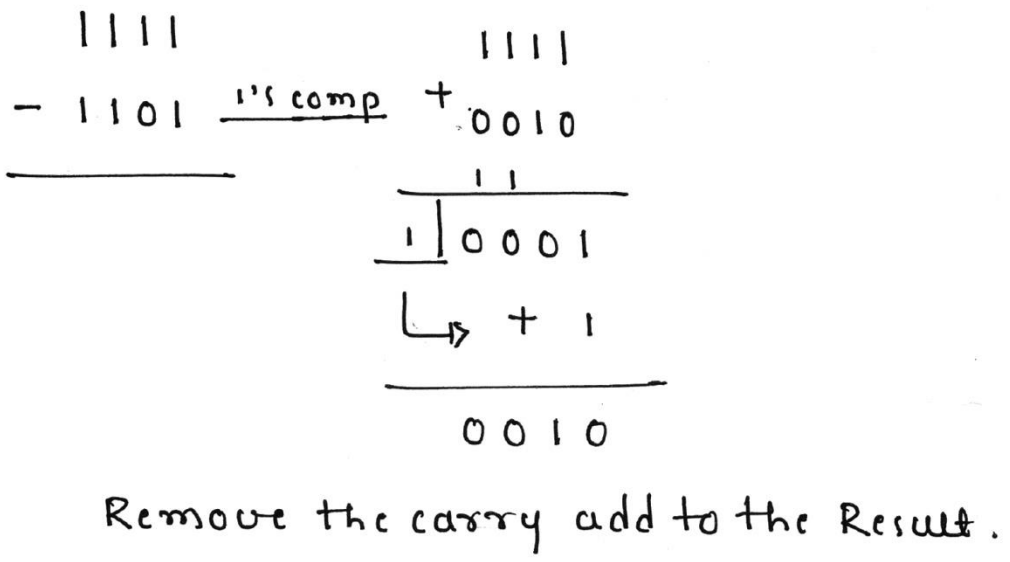
$928_{10} = 3A0_{16}$

ii) Convert Hexadecimal 7AC.39 to the Binary
(Conversion Hexadecimal to Binary-04M)



$7AC.39_{6} = 11110101100.00111001_{2}$

iii) Subtract $(1101)_2$ from $(1111)_2$ using1's Compliment Method
(One's Complementary Substraction - 2 M)



1. (b) i) Write a note on ASCII Code **5M**
(ASC II Stands for 1M + Features 3M + Applications 1M)

Ans :- ASCII Stands for American Standard Code for Information Interchange. It is also known as alphanumeric Code. It is a 7 bit Code in Which the Decimal Digits are represented by the BCD Code preceded by 011. Since it is a 7 bit Code, It represent 2^7 = 128 Symbols. These Symbols are assigned to different alphanumeric Characters. (Letters, Numbers and Other Special Symbols) For Example The Hexadecimal Nos 30H to 39H represents 0 to 9 decimal nos and 41H to 54H represents capital letters A through Z. The 7 bit code format is $D_6D_5D_4D_3D_2D_1D_0$ Where each D is a "0 or 1"
Applications: 1) Printer, 2) Keyboard

ii) Write the procedure for conversion from Binary to Gray Code with an Example 5M

(Conversion Binary to Gray Code Procedure 4M + Example 2M)

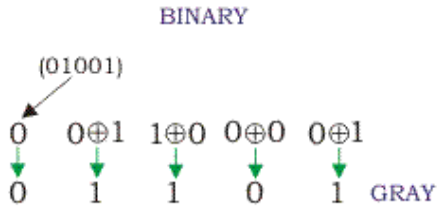
Ans : Binary to Gray

Procedure:-

1) The Most significant bit in the Gray Code is the same as the Corresponding bit in the Binary number

2) Going from left to right, add each adjacent pair of binary bits to get the next gray code bit, discard carry.

Example :-



2. (a) i) Add $(AB8)_{16}$ and $(IF5)_{16}$ **10M**

(Add numbers with Base 04M)

Ans : $AB8_{16}+1F5_{16}$ + $AB8_{16}$

$1F5_{16}$
CAD_{16}

1st Column : $8_{16}+5_{16}=13\rightarrow D$

2nd Column : $B_{16}+F_{16}=26$
$= 11_{10}+15_{10}=26_{10}$
$26_{10}-16_{10}=10_{16} \rightarrow A$
A_{16} with a carry 1
3rd Column : $A_{16}+1_{16}+1_{16}=12_{16}\rightarrow C$

ii) Add $(654)_8$ and $(236)_8$
(Add numbers with base 04M)

Ans : 654_8+236_8

$$\begin{array}{r} 654_8 \\ +236_8 \\ \hline 1112_8 \end{array}$$

1st Column : 4+6=10
10-8=2 with carry 1
2nd Column : 5+3+1=9
9-8=1 with carry 1
3rd Column : 6+2+1=9
9-8=1 with carry 1

iii) Convert $(110111.11)_2$ into decimal
(Conversion Binary to decimal)

Ans :-

$$110111.11_2 = 1\times2^5+1\times2^4+0\times2^3+1\times2^2+1\times2^1+1\times2^0+1\times2^{-1}+1\times2^{-2}$$

$$= 1\times32+1\times16+0\times8+1\times4+1\times2+1\times1+1\times\frac{1}{2}+1\times\frac{1}{4}$$

$$= 32+16+0+4+2+1+0.5+0.25$$

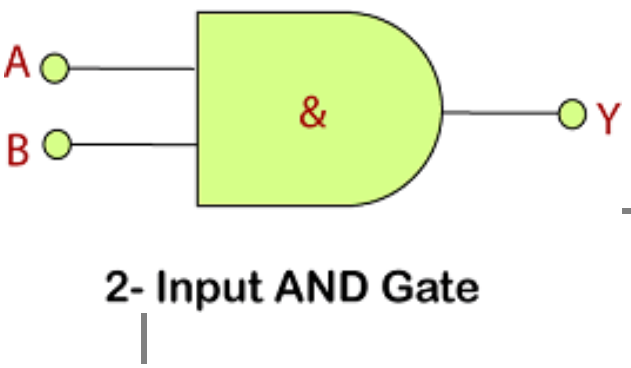
$$110111.11_2 = 55.75_{10}$$

2. b) i) Define logic gate. write symbol and TT And x or gates **5M**

(Definition 1M + Symbol 2M + TT 2M)

Ans : Logic Gate is a Digital Circuit with one or more input Signals, But only one Output Signal. All the input Signals and Output Signal are either low or high Voltage levels.

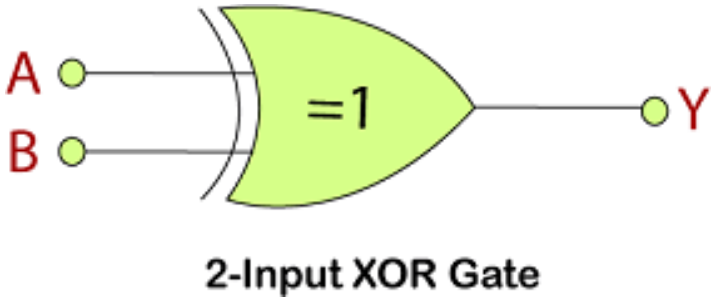
AND Gate



2- Input AND Gate

Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

XOR Gate



2-Input XOR Gate

Inputs		Output
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

ii) List the laws of Boolean Algebra **5M**

(I Law 2M + II Law 2M + III Law 1M)

Ans : i) Commutative Law : This law states that no matter in which order we use the variables. It means that the order of Variables doesn't matter in this law.

A.B = B.A

A + B = B + A

ii) Associative Law : This law states that the operation can be performed in any order when the variables priority is Same as

(A.B)C = A.(B.C)

(A+B)+C=A+(B+C)

iii) Distributive Law : This law allows us to open up brackets. Simply we can open the brackets in Boolean expressions.

A. (B+C) = AB+AC

SECTION-II

3 a) State and prove Demorgan's Theorem's
(Each theorem statement 2x2=4M + Each Expression 2x2=4 + Each Truth Table 1x2=2)

Ans : I Theorem

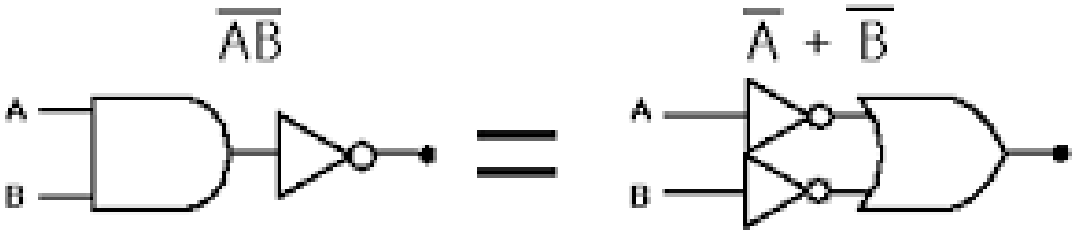
Statement : States that " The compliment of product is equal to the sum of their individual complements

$$\text{i.e } \overline{AB} = \bar{A}+\bar{B}$$

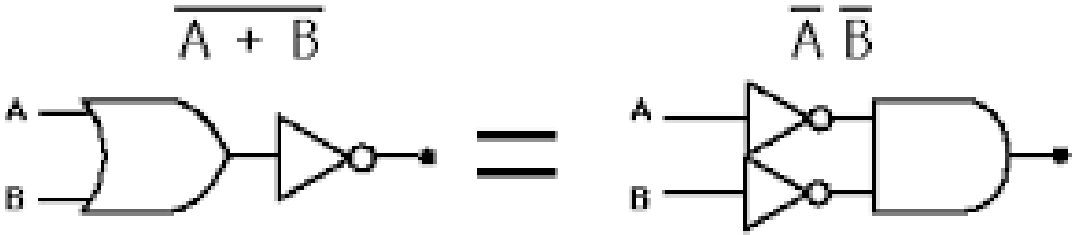
II Theorem

Statement : States that "The complement of sum is equal to the product of the individual complements"

$$\text{i.e } \overline{A+B} = \bar{A}.\bar{B}$$



A NAND gate is equivalent to an inversion followed by an OR



A NOR gate is equivalent to an inversion followed by an AND

A	B	$\bar{A}$	$\bar{B}$	$A \cdot B$	$\overline{A \cdot B}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

A	B	$\bar{A}$	$\bar{B}$	A+B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

b) Simplify logic expressions using Boolean Algebra Draw the Logic Diagram 10M
(Simplification 3x2=6M-Logic Diagram 2x2=4M)

i) $Y = (A+B)(A+\bar{B})(\bar{A}+B)$

Ans: $Y = (A+B)(A+\bar{B})(\bar{A}+B)$

$= A\underline{A} + A\bar{B} + AB + \underline{B\bar{B}}\ (\bar{A}+B)$

$= A + A\bar{B} + AB + 0\ (\bar{A}+B)$

$= A\ (1 + \underline{\bar{B} + B})\ (\bar{A}+B)$

$= A\ (1+1)\ (\bar{A}+B)$

$= A \cdot 1\ (\bar{A}+B)$

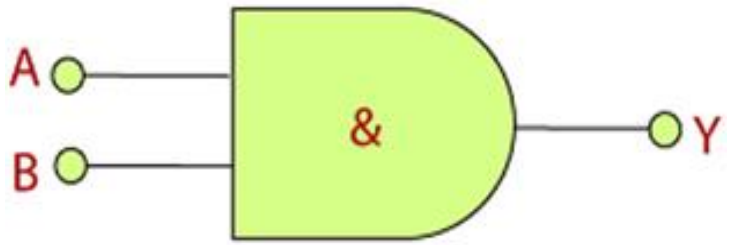
$= A\ (\bar{A}+B)$

$= \underline{A\bar{A}} + AB$

$= 0 + AB$

$Y = AB$

logic diagram



ii) $Y = ABCD + AB\bar{C}D + \bar{A}BCD$

$= ABD(C+\bar{C}) + \bar{A}BCD$

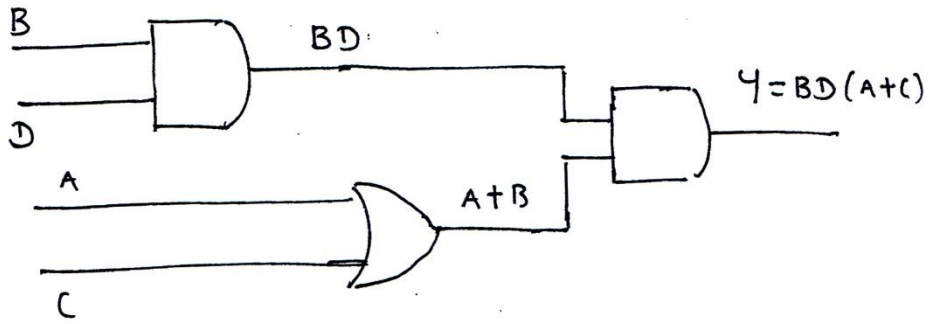
$= ABD(1) + \bar{A}BCD$

$= ABD + \bar{A}BCD$

$= BD(A+\bar{A}C)$

$Y = BD(A+C) \quad [\because A+\bar{A}B = A+B]$

logic diagram



4) a) Define the following **10M**

(Definition of Each Term 2x5=10M)

i) K-Map : The K-Map is a Systematic way of Simplifying Boolean expressions with the help of the K-Map method, We can find the simplest POS and SOP expressions, Which is known as minimum expression.

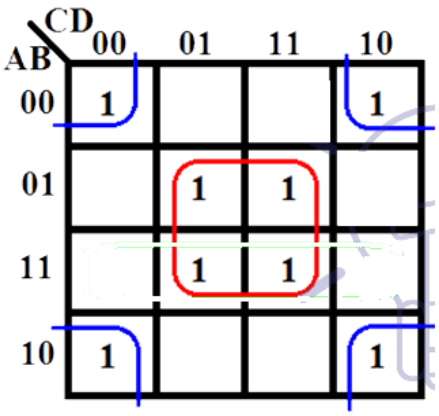
ii) Product Term : A Product term is a logical product of Several Variables. The Variables may or may not be complemented
Ex : ABC, $\bar{A}$ B $\bar{C}$
iii) Sum Term : A Sum Term is a Sum of Several Variables. The variables may or may not be complemented
Ex : A+B+C, $\bar{A}$+B+$\bar{C}$
iv) SOP : Sum of Products expression is Several product terms logically added i.e two or more AND[ed] Functions OR[ed] together.
Ex : 1) AB+BC, 2) $\bar{A}$BC+BD

v) POS : Product of Sum expression is Several Sum terms logically multiplied i.e two or more OR[ed] terms AND[ed] together.
Ex : 1) (A+B) ($\overline{A}$+B) (A+$\overline{B}$), 2) (A+B+C) ($\overline{A}$+B+C) (A+$\overline{B}$+$\overline{C}$)

4. b) Simplification of Boolean Expression using K-Map Draw the Logic Diagram 10M
Y = $\overline{A}\overline{B}\overline{C}\overline{D}$ + $\overline{A}\overline{B}$CD + A$\overline{B}\overline{C}\overline{D}$ + A$\overline{B}$CD + $\overline{A}$B$\overline{C}$D + $\overline{A}$BCD + ABC$\overline{D}$ + ABCD
(Draw 4 Variable K-Map 2M + Plotting Variables on a K-Map 2M + Grouping 2M + Simplified Expression 2M + Logic Diagram 2M)

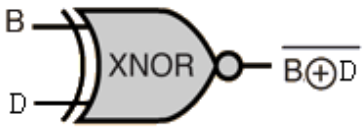
Y = $\overline{A}\overline{B}\overline{C}\overline{D}$ + $\overline{A}\overline{B}$CD + A$\overline{B}\overline{C}\overline{D}$ + A$\overline{B}$CD + $\overline{A}$B$\overline{C}$D + $\overline{A}$BCD + ABC$\overline{D}$ + ABCD

4 Variable Key Map



Y = B D+$\overline{B}$ $\overline{D}$

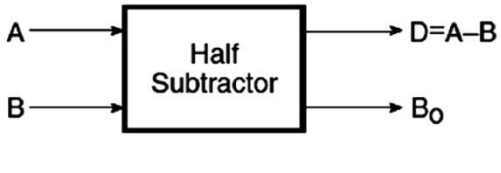
Logic Diagram



SECTION - III

5. (a) (i) Explain half subtractor with truth table. 5M
(Definition with Block diagram 1M + Truth Table 2M + Logic Diagram 1M + Explanation 1M)
Ans :- Half-subtractor is a combinational circuit that can be used to subtract one binary digit from another to produce a DIFFERENCE output and a BORROW output. The BORROW output here specifies whether a '1' has been borrowed to perform the subtraction. The truth table of a half-subtractor, as shown below, explains this further.

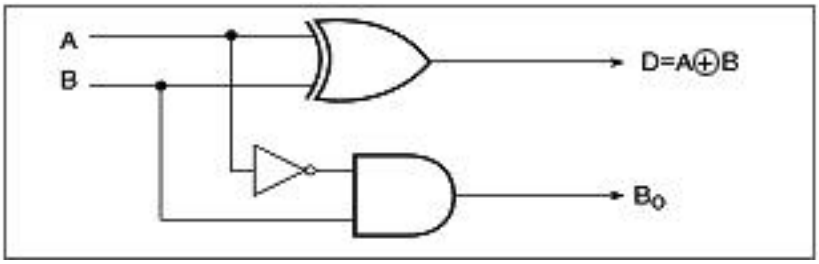
The Boolean expressions for the two outputs are given by the equations



A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = \overline{A}.B + A.\overline{B}$$

$$B_o = \overline{A}.B$$



It is obvious that there is no further scope for any simplification of the Boolean expressions given. While the expression for the DIFFERENCE (D) output is that of an EX-OR gate, the expression for the BORROW output (Bo) is that of an AND gatewith input a complemented before it is fed to the gate.
The below figure shows the logic implementation of a half-subtractor.

(ii) Write the Comparison between serial and parallel adder. 5M

(Each Comparison 1x5=5)

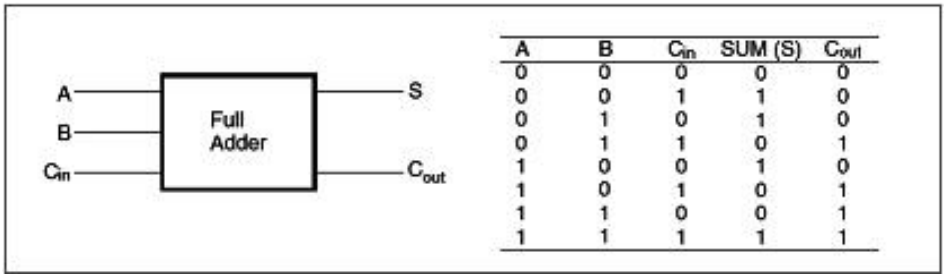
Ans :-

Serial adder	Parallel adder
Serial adder is less fast.	Parallel adder is fast as compare to serial adder.
It requires fewer components for operation.	It require large component for operation.
Addition process is perform by bit-by-bit process	Addition process is performing by parallel order. Means all bits add simultaneously.
It requires one full adder circuit.	No. of full adder circuit is equal to no. of bits in binary adder.
Time required for addition depends on number of bits.	Time required does not depend on the number of bits'.

5. (b) Explain working of a full adder with logic diagram and truth table. 10M

(Definition with Block Diagram 3M + Truth Table 2M + Logical Expression 2M + Logic Diagram 3M)

Ans :-The full-adder accepts two input bits and an input carry and generates a sumoutput and an output carry. The basic difference between a full-adder and a half-adder is that the full-adder accepts an input carry. The below figure shows the truth table of a full adder circuit showing allpossible input combinations and corresponding outputs.



A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean expressions for the two output variables for the SUM output (S) and forthe CARRY output (Count) are :

$$\text{Sum} = \bar{A}\,\bar{B}\,C_{in} + \bar{A}\,B\,\bar{C}_{in} + A\,\bar{B}\,\bar{C}_{in} + A\,B\,C_{in}$$

$$= C_{in}(\bar{A}\,\bar{B} + A\,B) + \bar{C}_{in}(\bar{A}\,B + A\,\bar{B})$$

$$= C_{in}(A \odot B) + \bar{C}_{in}(A \oplus B)$$

$$= C_{in}(\overline{A \oplus B}) + \bar{C}_{in}(A \oplus B)$$

$$= C_{in} \oplus (A \oplus B)$$

$$\text{Carry} = AB + AC_{in} + BC_{in}$$

$$= AB + AC_{in}(B + \bar{B}) + BC_{in}(A + \bar{A})$$

$$= AB + ABC_{in} + A\bar{B}C_{in} + ABC_{in} + \bar{A}BC_{in}$$

$$= AB(1 + C_{in} + C_{in}) + A\bar{B}C_{in} + \bar{A}BC_{in}$$

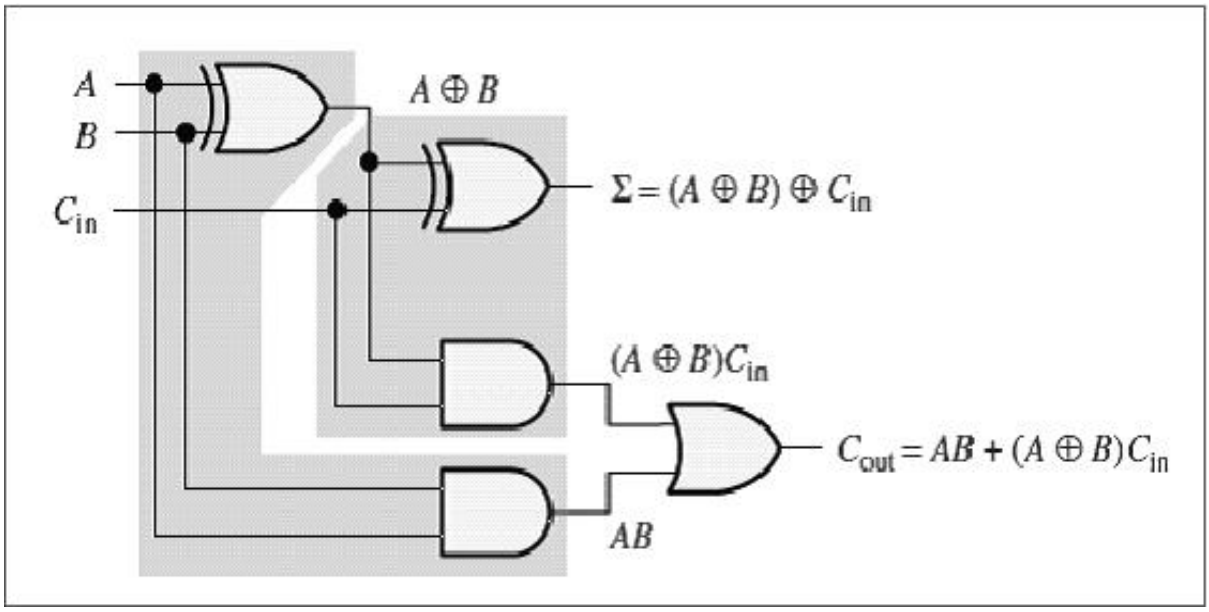
$$= AB + A\bar{B}C_{in} + \bar{A}BC_{in}$$

$$= AB + C_{in}(A\bar{B} + \bar{A}B)$$

$$= AB + C_{in}(A \oplus B)$$

$A + A = A$

$1 + A = 1$

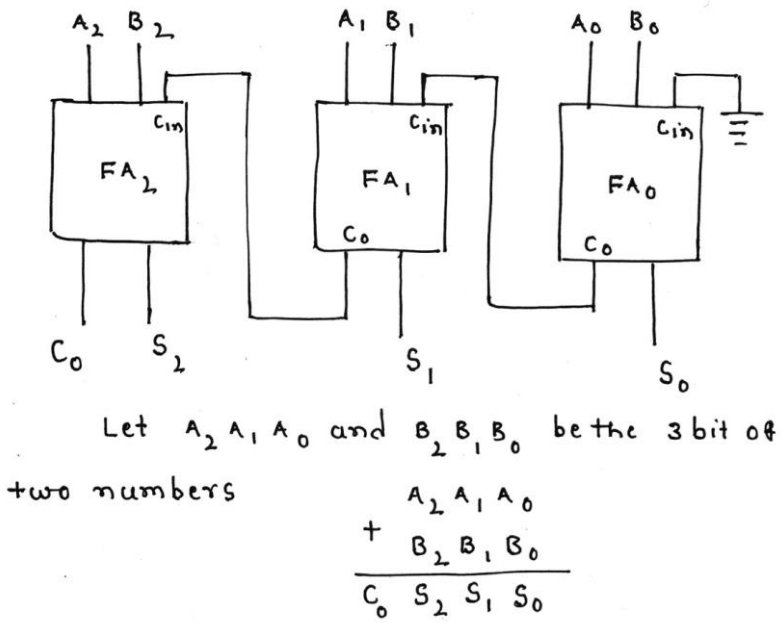


6. (a) Explain Working of a 3 bit parallel adder circuit. 10M

(Definition with Block Diagram 4 M + expression 2M + Explanation 4M)

Ans :- The 3 bit adder using full adder this is capable of adding two 3 bit number resulting in a 3 bit sum and a carry output. Since all bit the augends and addend are fed into the adder circuit simultaneously and the addition in each position are taking place at the Same time, this circuit is known as parallel adder.

Block Diagram



The Circuit uses 3 full adder circuits. These circuits are connected in parallel or cascade form Each full adder circuit has 3 inputs and two Outputs (Sum and Carryout). Since FA_0 address the two LSB it has no output carry (There is no preciding Stage) and hence it is connected to ground.

Ex :- 101 where $A_2=1$ $A_1=0$ $A_0=1$

101 where $B_2=1$ $B_1=0$ $B_0=0$

1011 The Sum Should be

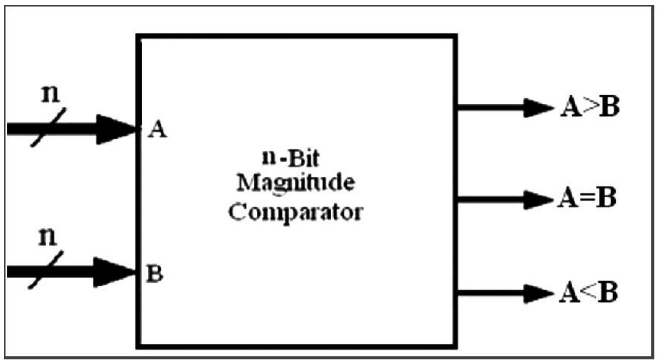
C0=1, $S_2=0$ $S_1=1$ and $S_0=1$

6) b) Explain two bit magnitude comparator with truth table and gate level circuit 10M

(Defn with Block Diagram 2M + TT 2M + Logical Expression 2M + Logic Diagram 2M + Expln 2M)

Ans :-Comparator is a Special Combination circuit designed primarily to compare a relative magnitude of two binary numbers. The below fig shows the Block Diagram of n bit Comparator, It recieves "n" bit numbers "a" and "b" as inputs and outputs are (A>B, A=B, A<B) depending upon the relative magnitudes of two numbers, One of the Outputs will high.

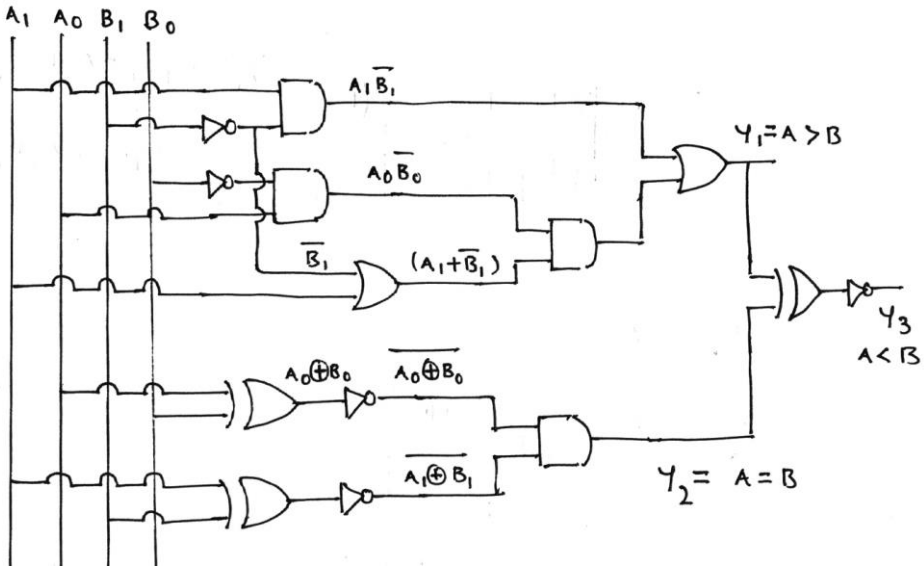
Block Diagram of n bit Comparator



Truth Table

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Logic Diagram



In digital system, comparison of two numbers is an arithmetic operation thatdetermines if one number is greater than, equal to, or less than the othernumber. So comparator is used for this purpose. Magnitude comparator is a combinational circuit that comparestwo numbers, A and B, and determines their relative magnitudes. The outcome of comparison is specified by three binary variablesthat indicate whether A>B, A=B, or A<B, 2-Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0& B1, B0).

SECTION - IV

7 a) i) Define Multiplexer and list the applications **5M**
(Definition 1M + Each Application 1x4=4M)

Ans :- The Multiplexer is a Combinational Logic Circuit which is having many inputs and single output, The particular input is passed to the output depends upon the values on the Select lines

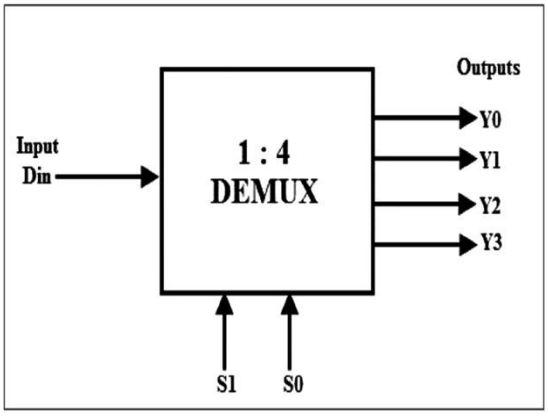
Applications :- (Any 4)

1) Data Routing
2) Data Bussing
3) Multiplexer as a Function Generator
4) Parallel to Serial Converter
5) Cable TV Signal Distribution
6) Telephone Network
7) Sharing Printer

ii) Define Demultiplexer. Explain the Operation of 1:4 Demultiplexer **5M**
(Definition 1M + TT 1M + Logic Diagram 2M + Explain 1M)

Ans :- The Demultiplexer is a Combinational Logic Circuit which is having single input and many outputs, the data on one input is routed to any one output depends upon the values on the Select lines.

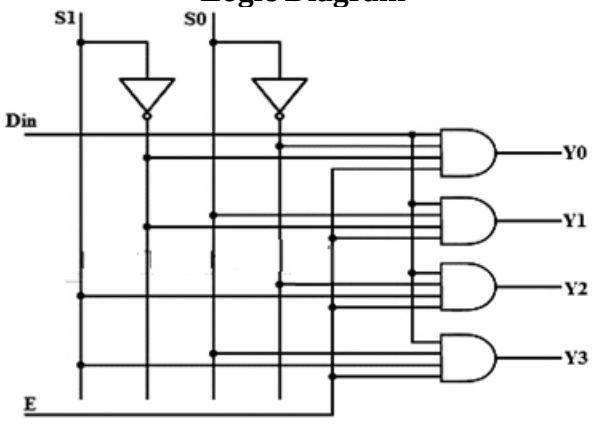
Block Diagram



Truth Table

Data Input	Select Inputs		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

Logic Diagram

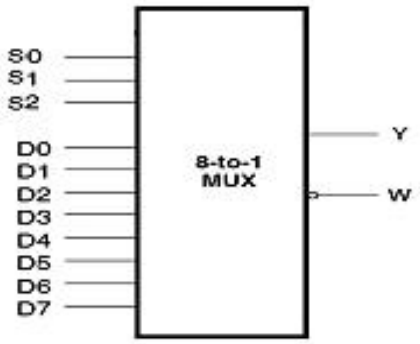


A 1:4 demultiplexer has one input and 4 outputs. Two Select lines are used to select one of the four outputs. The above fig shows a 1 to 4 line demux circuit. The input data line goes to all of the AND gates. The two Select lines enable only one gate at a time and the data appearing on the input line will pass through the Selected gate to the associated output line. For ex : if S_1=0 and S_0=0 the o/p Y_0 is connected to the input if S_1=0 and S_0=1 the o/p Y_1 line and so on.

7. b) Explain the working of 8:1 Multiplexer with logic Circuit, Symbol and TT 10M (Block Diagram 2M + TT 2M + Logic Diagram 4M + Explanation 2M)

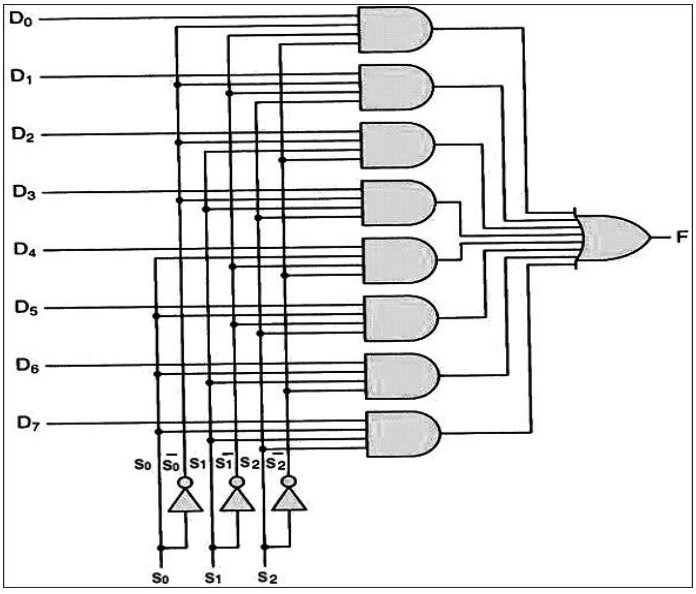
Ans :- In a 8:1 Multiplexer, it has 8 inputs and only one outputs as shown in a fig below

Block Diagram **Truth Table**



Inputs			Output
Select			
S2	S1	S0	Y
X	X	X	L
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Logic Diagram



The Binary data applied to the Select inputs $S_2S_1S_0$, Decides which one of the input will be made available at output Y

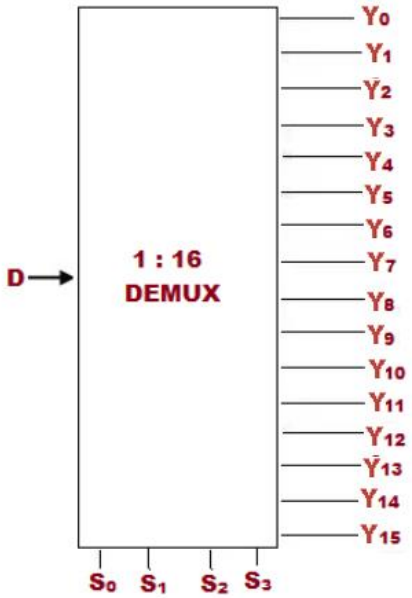
For Ex : if S_2=0, S_1=0, S_0=0 the Do i/p will be made available at output Y and if S_2=1, S_1=0, S_0=0 then D4 i/p will be made available at output y and so-on in 8:1 mux where S_2, S_1 and S_0 are select lines.

8. a) Explain operation of 1:16 demultiplexer **10M**

(Block diagram 2M + TT2+ Logic Diagram 4M + Explanation 2M)

Ans :-

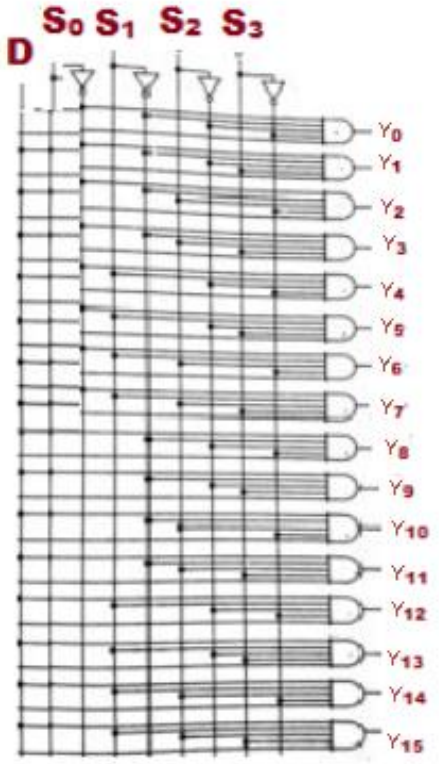
Block Diagram



Truth Table

INPUTS				OUTPUTS															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	A	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Logic Diagram



A 1:16 demux has one input and 16 outputs. Four Select lines are used to select one of the 16 outputs. The above logic diagram shows a 1:16 demux circuit The input data line goes to all of the AND Gates. The 4 Select lines enable only one gate at a time and the data appearing on the input line will pass through the Selected Gate to the associated output line for example if = S_3=0, S_2=0, S_1=0 and S_0=0 the output Y_0 is connected to the input. if S_3=1, S_2=1, S_1=0 and S0=0 the output Y_{12} is Connected to the input and So-on.

8. b) i) List the advantages and disadvantages of ICS **5M**

(Each advantage + Disadvantage 1/2 x5=2.5+1/2x5=2.5=5)

Ans :- **Advantages :**
1) Smaller in Size
2) Less Weight
3) Low Cost
4) Highly Reliable
5) Low Power Consumption
6) Easy Replacement.

Disadvantages :
1) Repair is not possible
2) Large Capacitance Can't be fabricated
3) Coils or Inductors Can't be fabricated
4) Cannot handle large power
5) Delicate Careful and handling is needed.

8. b) ii) Classify IC's based on Scale of Integration **05M**
(Each classification 1Mx5=5M)

Ans :-
1) SSI (Small Scale Integration) : IC's under this Category contains 0-12 electronic components or logic Gates, On a Single Chip.
Ex : Basic Logic Gates, Flip Flops

2) MSI (Medium Scale Integration) : MSI Describes integrated circuits to have 13 to 99 electronic components or equivalent logic gates on a Single Chip.
Ex : Adders, Registers, Encoders.

3) LSI (Large Scale Integration) : LSI Describes integrated circuit, to have 100 to 9,999 electronic components or equivalent logic gates on a Single Chip.
Ex : Microcontroller, RAM's ROM's

4) VLSI (Very Large Scale Integration) : VLSI describes integrated circuits with complexities of 10,000 to 99,999 electronic components or equivalent logic gates on a single chip.
Ex : Advanced Microprocessors, Memory Chips.

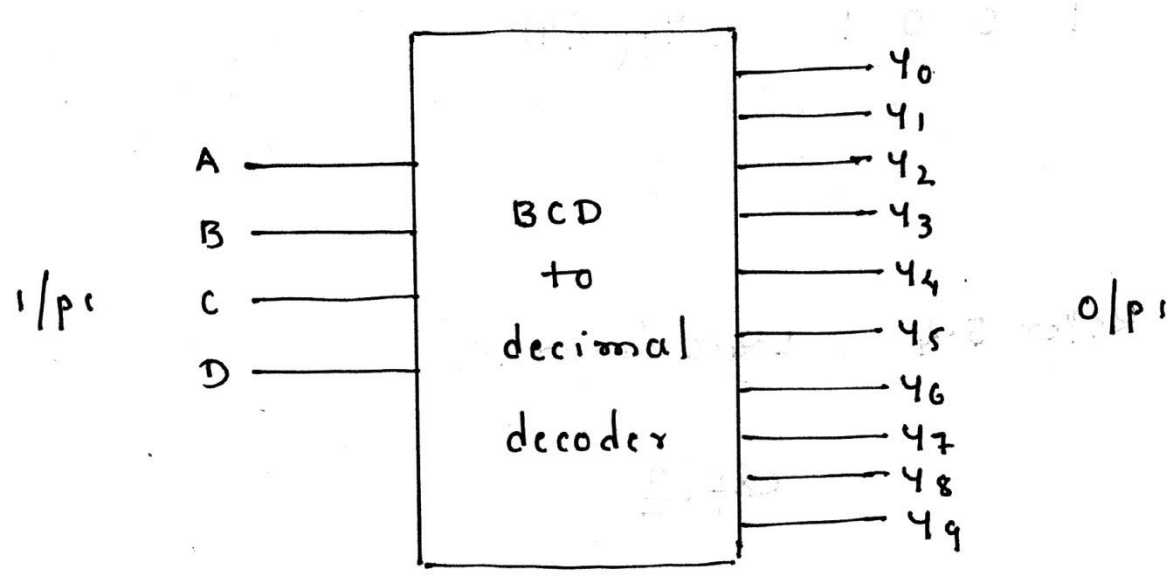
5) ULSI (Ultra Large Scale Integration) : It is the Next level of Complexity with more than 1,00,000 electronic Components or Equivalent Logic Gates on a Single Chip.
Ex : Single Chip Computers, Large Memory Chips.

SECTION-V

9. a) Sketch and explain logic circuit of BCD to Decimal Decoder. **10M**
(Definition with Block Diagram 2M + TT 2M + Logic Diagram 4M + Explanation 2M)

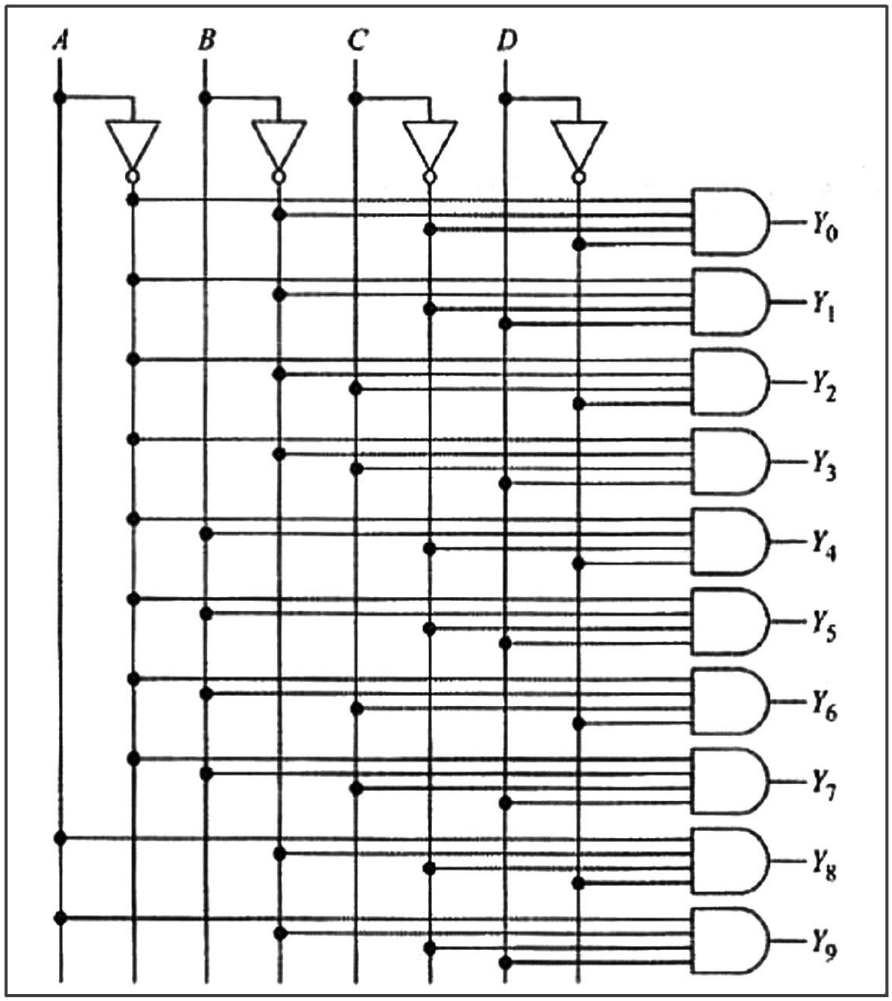
Ans :- The Decoder is a Combinational logic circuit that converts coded information such as binary into recognizable form such as a decimal

Block Diagram.



I/P				O/P
A	B	C	D	Decimal digits
0	0	0	0	Y_0 (0)
0	0	0	1	Y_1 (1)
0	0	1	0	Y_2 (2)
0	0	1	1	Y_3 (3)
0	1	0	0	Y_4 (4)
0	1	0	1	Y_5 (5)
0	1	1	0	Y_6 (6)
0	1	1	1	Y_7 (7)
1	0	0	0	Y_8 (8)
1	0	0	1	Y_9 (9)

Logic Diagram



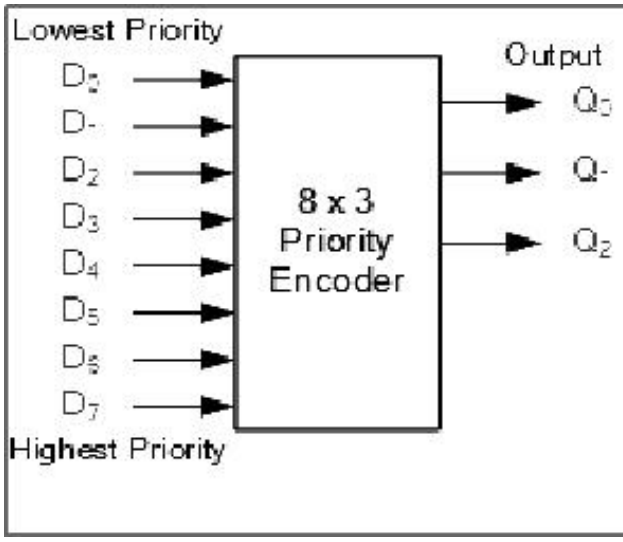
The BCD-to decimal decoder converts each BCD code (8421 code) into one of ten possible decimal digit indications. It is frequently referred as a 4- line-to-10-line decoder or a 1-of-10 decoder. The circuit shown below is called a l-of-10 decoder because only 1 of the 10 output lines is high. For instance, when ABCD is 0011, only the Y3 AND gate has all high inputs; therefore, only the Y3 output is high, If ABCD changes to 1000, only the Y8 AND gate has all high inputs; as a result, only the Y8 output goes high. If you check the other ABCD possibilities (0000 to 1001), you will find that the subscript of the high output always equals the decimal equivalent of the input BCD digit. For this reason, the circuit is also called a BCD-to-decimal converter.

9. b) Explain priority Encoder, With a neat Logic Diagram and Truth Table. 10M

(Definition with Block Diagram 2M + TT 2M + Logic Diagram 4M + Explanation 2M)

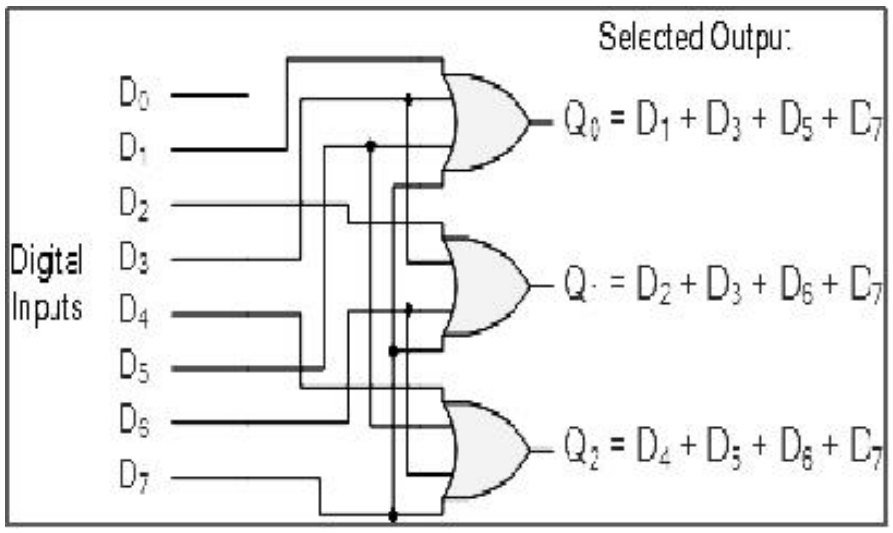
Ans :- The priority encoder is a Combinational logic circuit which produce a output corresponding to the highest order digit appearing on the input and ignoring all others.

Block Diagram



Truth Table

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1



Priority encoders are available in standard IC form and the TTL 74LS148 is an8-to-3 bit priority encoder which has eight active LOW (logic "0") inputs and provides a 3-bit code of the highest ranked input at its output.

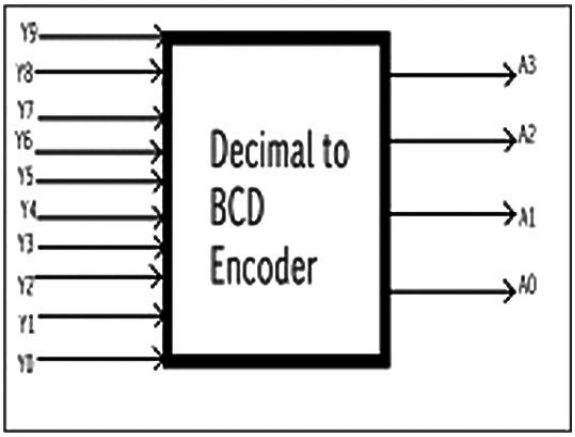
Priority encoders output the highest order input first for example, if input lines "D2", "D3" and "D5" are applied simultaneously the output code would be for input "D5" ("101") as this has the highest order out of the 3 inputs. Once input"D5" had been removed the next highest output code would be for input "D3" ("011"), and so on.

10. a) Explain the Working of decimal to BCD Encoder **10M**

(Block Diagram 2M + TT 2M + Logic Diagram 4M + Explanation 2M)

Ans :- In a decimal to BCD Encoder has 10 input lines and 4 output lines

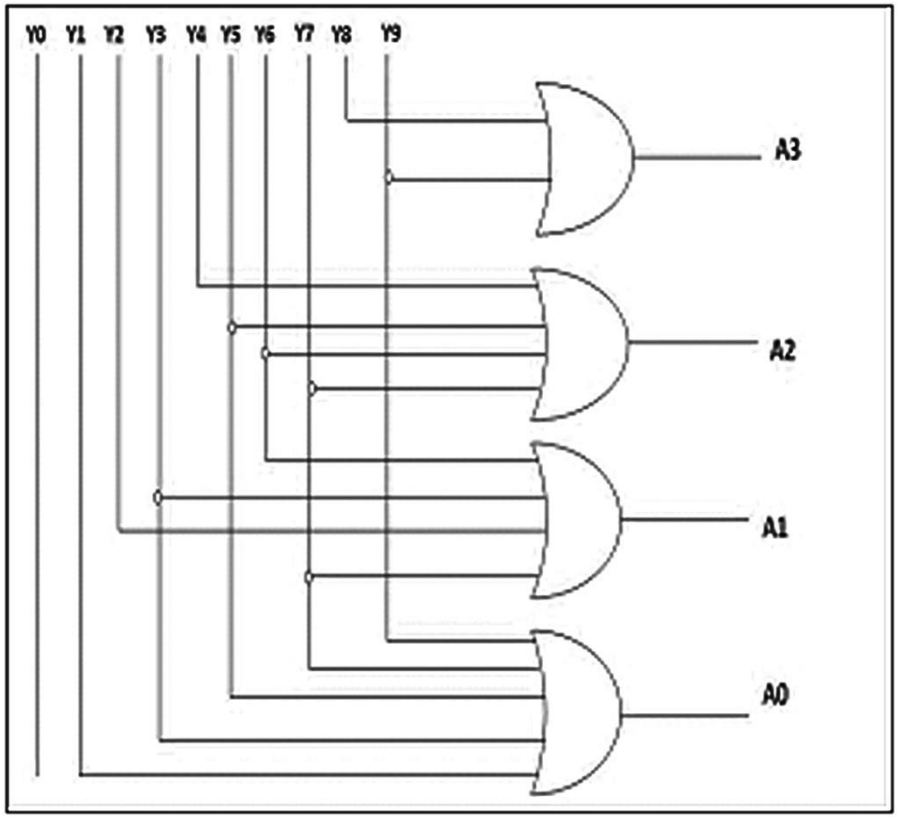
Block Diagram



Truth Table

INPUTS										OUTPUTS			
Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

Logic Diagram



The decimal to binary encoder usually consists of 10 input lines and 4 output lines.Each input line corresponds to the each decimal digit and 4 outputs correspond to the BCD code. This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on theoutput lines.

10. b) i) Compare features of Standard TTL, CMOS and ECL 5M

(Each Comparison 1x5=05M)

Ans :-

Comparison between TTL, ECL, and CMOS

SPECIFICATION	TTL	ECL	CMOS
Components	Transistors & passive elements	Transistors & passive elements	MOSFETs
Basic Gate	NAND	OR/NOR	NAND/NOR
Noise Immunity	Strong	Good	Very strong
Fan-out	10	25	More than 50
tPD in ns	1.5-30	1-4	1-210
Noise margin	Moderate	Low	High
Power/gate in mWatt	10	40-55	0.0025
Clock rate in MHz	35	>60	10
Figure of Merit	100	40-100	0.7

ii) Describe the Interfacing between TTL and CMOS **5M**

(Circuit Diagram 2M + Explanation 3M)

Ans :-

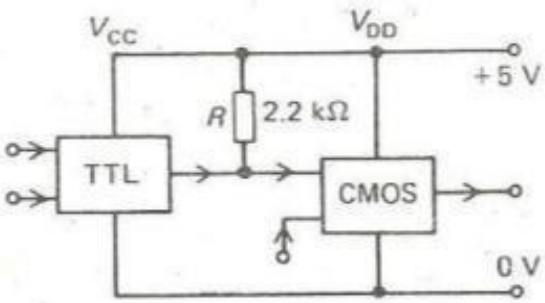


Fig-1(a) TTL to CMOS interfacing

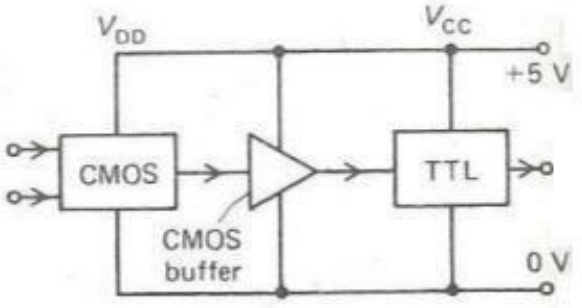


Fig-1(b) CMOS to TTL interfacing

Figure-1 depicts TTL to CMOS interfacing and CMOS to TTL interfacing circuits. When 5V supply is given to TTL and CMOS ICs, logic levels of TTL and CMOS are different. One TTL IC can drive any number of CMOS ICs. However, TTL output in 'high state' yields 2.4 Volt which is lower than the minimum voltage required by CMOS IC (which is 3.5V) . For TTL to CMOS interfacing, standard pull up resistor is connected which solves the interfacing problem as mentioned. This is shown in figure-1(a). A CMOS IC can easily drive any low power schottky TTL IC directly. But to interface standard TTL IC, buffer is provided in between CMOS and TTL ICs.This is shown in figure-1(b).

CERTIFICATE

I certify that the model answer script that are prepared by me for the subject code **20EC11T- Digital Electronics** are from the prescribed text books and model answer script and scheme of valuation prepared by me are correct.

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