Verification of Self Project on CV for Placement 2025

My name is Adipta Halder (Roll No: 21EC37023), a final year student of the Department of Electronics and Electrical Communication Engineering, enrolled in its dual degree course. I am writing to request your assistance in verifying the self-project that I have included in my CV for the upcoming placement session. Your verification would greatly enhance the credibility of my CV and strengthen the representation of my skills and accomplishments to potential employers. The details of the project are as follows:

Project: Verilog implementation of the MIPS32 processor with a five-stage pipeline

Google Drive link: MIPS32 CPU ADIPTA

Github Link: GitHub - Adipta152/MIPS32-RISC-PROCESSOR-ERP-2025: MIPS32 BASED RISC PROCESSOR FEATURING 5 STAGE PIPELINE

Onedrive Link: MIPS32 RISC PROCESSOR 21EC37023 PROOF - OneDrive

- Implemented a 32-bit MIPS processor in Verilog with a standard 5-stage pipeline, enabling instruction-level parallelism
- Developed datapath and control modules, including ALU, register file, memory, and unified control unit
- Implemented a subset of MIPS32 integer-based instructions, including Register, Immediate, and Jump types
- Developed a pipeline hazard management system with data forwarding, pipeline stalling etc.
- Verified the processor functionality with a custom Verilog testbench

Mayank Sharad
(Professor's Signature)

Adipta Halder
(Student's Signature)