8-bit-CAM-Content-Addressable-Memory

INTRODUCTION:

Content Addressable Memory (CAM) is a specialized type of computer memory used in applications that require high-speed searching and data retrieval based on content matching. This paper presents the design and analysis of an 8-bit CAM system. The CAM architecture is explored in detail, focusing on key components such as the match line, comparison circuitry, and SRAM used as data storage cells. The design process involves determining the appropriate cell layout and organization to achieve optimal performance, considering factors such as power consumption and latency.

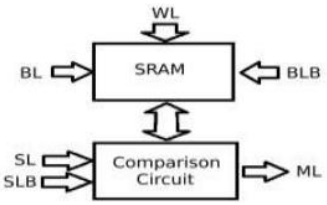


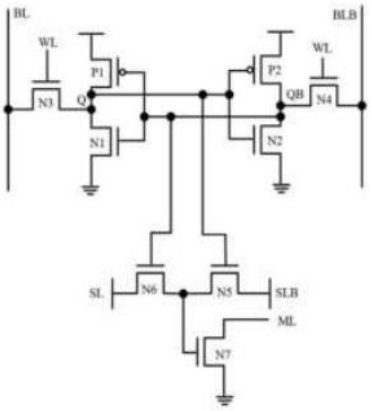
Fig1: Basic CAM Circuit

BL	BLB	SL	SLB	ML
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1

Table 1: CAM Operation

1 Bit NAND-CAM Design:

In this design, the SRAM uses a 6T configuration, where two cross-coupled inverters store a bit. These inverters are connected to two inputs, BL and BLB, for writing data into memory. The word line (WL) is always high for both read and write operations. The SRAM interfaces with the comparison circuit, which is designed using NAND gates. In this circuit, SL and SLB serve as inputs, and the overall output is ML. A pre-charge circuit, connected with an inverter, helps obtain the output ML. Initially, the ML lines are in a pre-charge phase and discharge to the ground when all CAM cells match. However, a significant drawback of using NAND gates in the CAM is the voltage drop across the next stage due to the pass transistors used in the comparison circuit.



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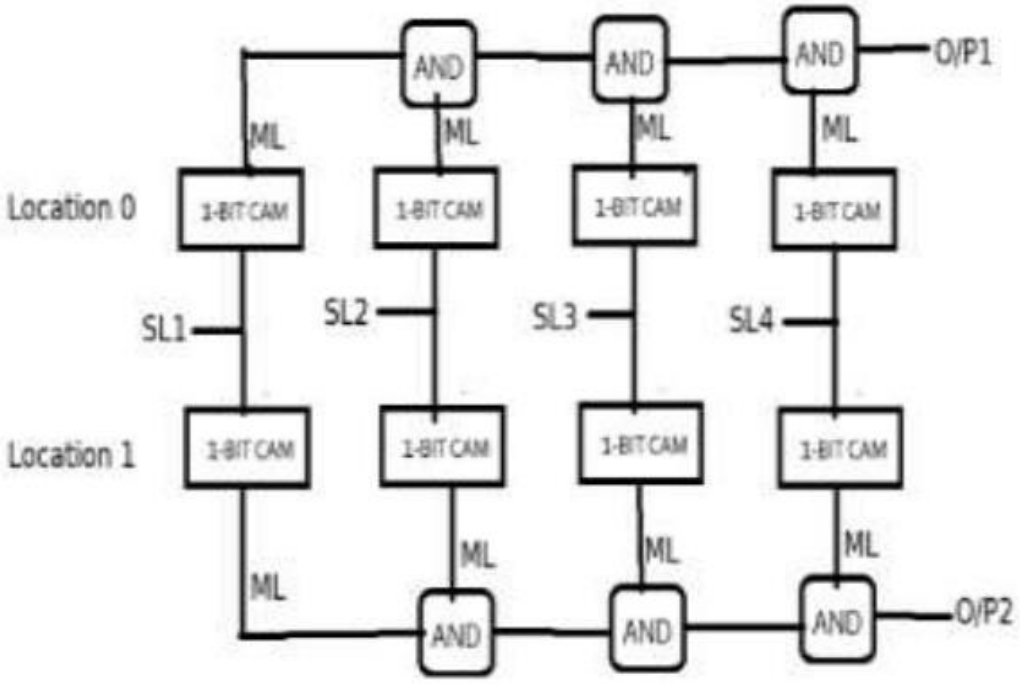
8-BIT CAM DESIGN:

After designed 8-bit structure, we realized the delay is increases when the bit-size increases then we go for different combination to decrease the delay, and finally we designed a full structured CAM which gives address when the searched sequence is stored in CAM and give high voltage value when the sequence is not present in CAM. In the above figure one sequence of 4-bit is stored in 0th location and another sequence of 4-bit is stored in 1st location when the searched sequence is matched with any one of the sequences then the respected o/p will be 1. Here the sequence will search serial manner when SL1and SL2 is matched with any one of the locations then the match line will be 1 for both and it will give as input to AND gate and the o/p of AND gate will 1. Similarly, it checks for all 4- bits when all 4-bit is same as searched sequence then the last AND gate output will be 1 that means the searched sequence is present in the memory. For understanding the accessing of address of the matched location we designed 16-bit CAM.



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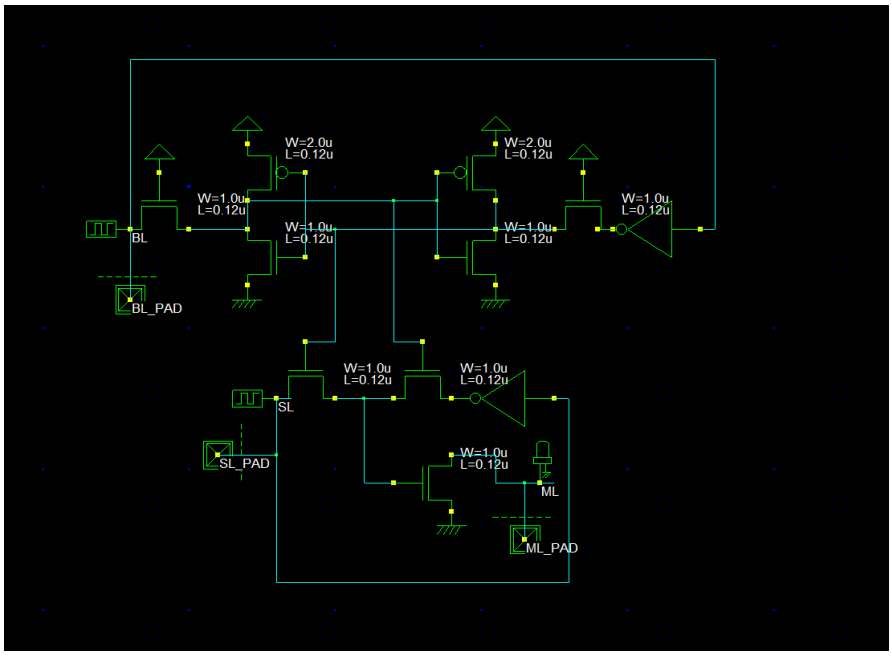
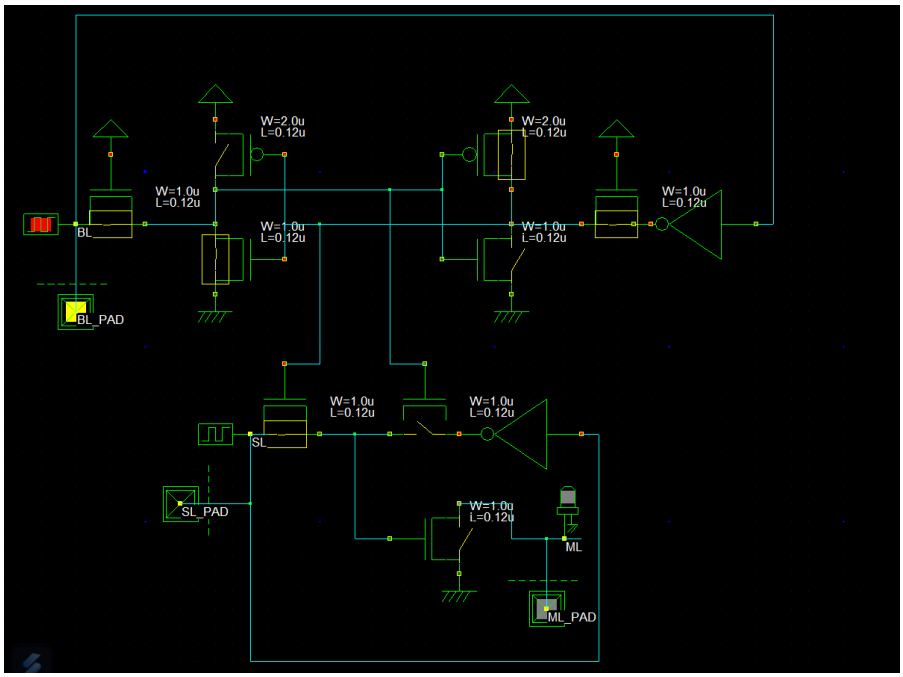
Simulation of 1 Bit CAM:





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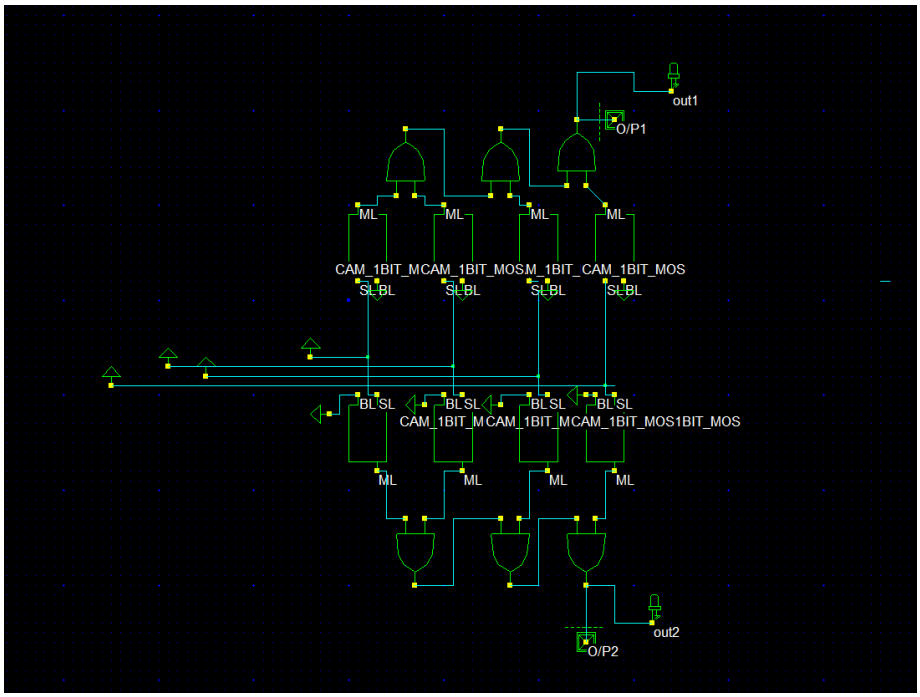
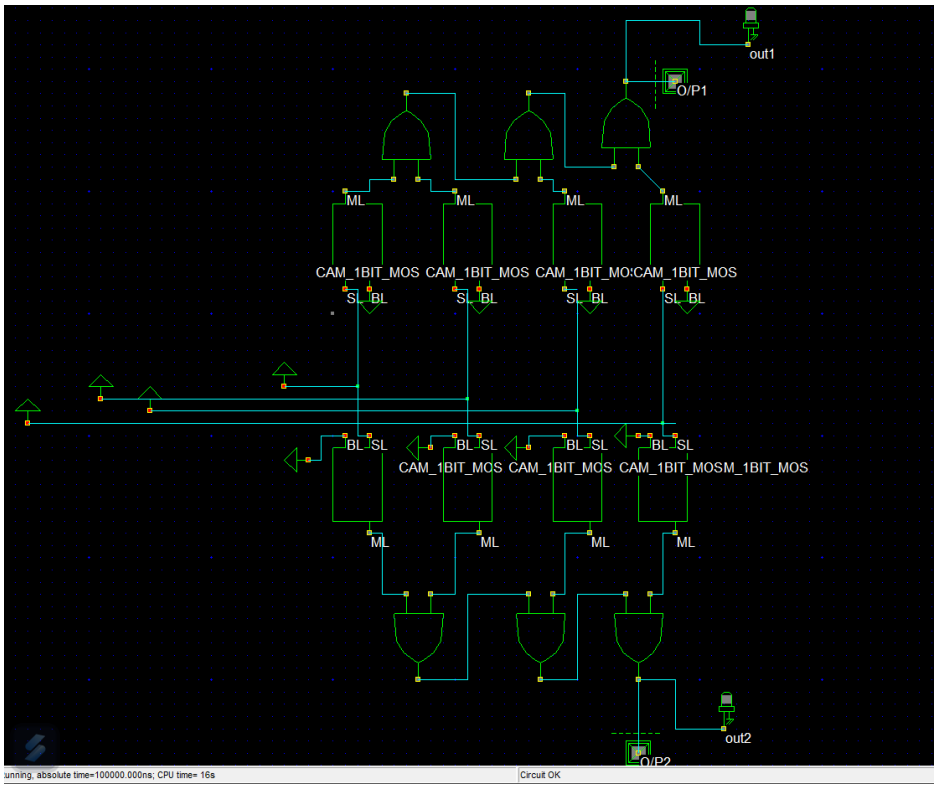
Simulation of 8 Bit CAM:





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Timing Diagram: