--Question Starting--
Match the following cache memory organization techniques with their implications on system performance and complexity:
1. Fully Associative Cache 2. Direct Mapped Cache 3. Set Associative Cache
A. Simplifies hardware design but increases miss penalty due to higher associativity
B. Minimizes conflict misses but requires complex hardware to search all blocks
C. Balances between hardware complexity and conflict misses by dividing cache into sets
Choose the correct answer from the options given below:
(1) 1-B, 2-C, 3-A
(2) 1-A, 2-B, 3-C
(3) 1-C, 2-A, 3-B
(4) 1-B, 2-A, 3-C
Answer Key: 1
Solution:
? Fully Associative Cache: Any block can go into any cache line, which minimizes conflict misses but requires hardware to compare all tags for every access, leading to increased complexity and potential delays.
? Direct Mapped Cache: Each block maps to exactly one cache line, simplifying hardware design but increasing conflict misses when multiple blocks compete for the same line.
? Set Associative Cache: Divides cache into sets, each containing multiple lines, reducing conflict misses relative to direct mapping while keeping hardware complexity manageable.
Hence, Option (1) is the right answer.

--Question Starting--
3. Match the following CPU scheduling algorithms with their fundamental characteristics:
1. Shortest Job First (SJF) 2. Round Robin (RR) 3. Priority Scheduling
A. Preemptive or non-preemptive; selects process with the smallest expected CPU burst
B. Cycles through processes for fair CPU time distribution; time quantum is fixed
C. Selects processes based on the highest priority; may lead to starvation
Choose the correct answer from the options given below:
(1) 1-A, 2-B, 3-C
(2) 1-B, 2-C, 3-A
(3) 1-C, 2-A, 3-B
(4) 1-A, 2-C, 3-B
Answer Key: 1
Solution:
? Shortest Job First (SJF): Selects the process with the least expected CPU burst time, optimizing average waiting time, can be preemptive or non-preemptive.
? Round Robin (RR): Gives each process a fixed time quantum in cyclic order, promoting fairness but possibly increasing context switches.
? Priority Scheduling: Processes are selected based on priority, which can be preemptive or non-preemptive, but may cause starvation of lower-priority processes.
Hence, Option (1) is the right answer.

--Question Starting--
4. Match the following memory management hardware techniques with their operational principles:
1. Memory Management Hardware with Base and Limit Registers 2. Paging Hardware 3. Segmentation Hardware
A. Divides memory into fixed-size blocks; uses page table for address translation
B. Uses registers to define the bounds of a process's address space
C. Supports variable-sized segments; maintains segment tables for address translation
Choose the correct answer from the options given below:
(1) 1-B, 2-A, 3-C
(2) 1-A, 2-B, 3-C

(3) 1-C, 2-A, 3-B
(4) 1-B, 2-C, 3-A
Answer Key: 1
Solution:
? Memory Management with Base and Limit Registers: Uses registers to specify the starting address and size of a process's memory region, providing simple protection.
? Paging Hardware: Implements fixed-size page frames and uses page tables for address translation, avoiding external fragmentation.
? Segmentation Hardware: Supports variable-sized segments, with segment tables mapping logical to physical addresses, allowing logical division of memory.
Hence, Option (1) is the right answer.