ADITH SUREPALLY

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EXPERIENCE & TRAINING

Analog Layout Design Trainee | MosChip Technologies, Hyderabad August 2025 – October 2025

- Mastered the end-to-end full-custom layout flow (schematic-to-GDSII) using the **Cadence Virtuoso** suite for design and **PVS/Assura** for physical verification in 90nm CMOS technology.
- Executed the complete physical layout for a portfolio of critical analog and standard cell blocks, including **Op-Amps, Bandgap References (BGR), DACs, a PLL, and D-Flipflops**.
- Applied advanced layout techniques to optimize performance, including **common-centroid & interdigitation matching**, and mitigated issues like **crosstalk, parasitics, and latch-up** using strategic shielding, guard rings, and deep N-well isolation.

Intern | NSIC (National Small Industries Corporation), Hyderabad *May 2023 – June 2023*

- Designed and assembled a prototype for an RFID-based locker system, integrating microcontrollers with RF readers and actuators and also enhanced with SIM 800C GSM Module.

PROJECTS

- **Analog & Standard Cell Layout Portfolio (90nm CMOS)** | MosChip Training Program

Executed the complete physical layout (floorplanning, placement, routing, and PVS/Assura verification) for a diverse portfolio of industry-standard circuits.
Key Analog Blocks: Successfully laid out an **Op-Amp** focusing on common-centroid matching, a **Bandgap Reference (BGR)**, a **Digital-to-Analog Converter (DAC)**, and a complex **Phase-Locked Loop (PLL)**.
Digital & Standard Cells: Created full-custom layouts for standard cells, including logic gates (NAND, NOR), MUX, and a **D-Flipflop**, and designed a **Level Shifter** utilizing deep N-well isolation techniques.

- **VLSI Implementation of a Cryptographic RNB Multiplier** | *B.Tech Major Project*

Designed the complete schematic-level architecture for multiple configurations (SISO, SIPO, PISO, PIPO) of a Residue Number System (RNS) based multiplier using the **Cadence Virtuoso** editor.
Validated the circuit's logical correctness through simulation, demonstrating a strong grasp of digital design principles in a VLSI context

EDUCATION AND CERTIFICATION

B.Tech, Electronics & Communication | Sreyas Institute of Engineering & Technology | 2024 | **6.85 CGPA**
Intermediate (Class XII) | Narayana Junior College, Hyderabad | 2021 | **84%**
Secondary School (Class X) | Dilsukhnagar Public School, Hyderabad | 2019 | **87%**
NPTEL Certifications: CMOS Digital VLSI Design, Embedded System Design, Digital Communication

TECHNICAL SKILLS

EDA TOOLS : Cadence Virtuoso, Cadence PVS, Cadence Assura
Verification : DRC, LVS, Antenna Checks, ERC, Latch-up Analysis
Layout Techniques : Common-Centroid Matching, Interdigitation, Shielding, Guard Rings, Deep N-well, Parasitic Mitigation
Languages & OS : SKILL (Basic), Perl (Basic), Linux/Unix Environment

SUMMARY

Detail-oriented VLSI engineering graduate specializing in analog IC layout. Possesses hands-on experience from an intensive training program, covering the end-to-end physical design of standard cells and complex analog circuits like Bandgap References and PLLs. Strong grasp of advanced layout techniques to optimize for performance and reliability in deep-submicron nodes