ADITH SUREPALLY

Phone : +91 7893747970
E-Mail : adithsurepally@gmail.com
LinkedIn : surepallyadith
Portfolio : https://adithsurepally.vercel.app

EXPERIENCE & TRAINING

Technical Operations Engineer |ARS Tech, Hyderabad (May 2024 – Present)

- Embedded Systems Development: Engineered and optimized core firmware using C++, ensuring robust performance and hardware-software integration for PIC16F676, PIC16F868, MS51FB9AE, etc. IC's for the Power Management, Wireless Auto machines, etc. projects.
- Full-Stack & Automation Engineering: Developed internal web interfaces and custom software tools to automate manual processes, significantly increasing operational throughput and workflow efficiency.
- Operational Logistics: Managed the end-to-end technical fulfillment process, overseeing the configuration, quality assurance, and secure dispatch of hardware devices for global/local shipment.
- Strategic Growth Support: Contributed to the company's scaling phase by identifying and implementing technical solutions that streamlined cross-departmental operations and supported business development goals.

Analog Layout Design Trainee | MosChip Technologies, Hyderabad (August 2025 – December 2025)

- Mastered end-to-end full-custom layout flow (schematic-to-GDSII) using Cadence Virtuoso and PVS/Assura for physical verification in **45nm CMOS technology** covering restrictive design rules, layout-dependent effects, and advanced verification methodologies.
- Executed complete physical layout for **15+ critical analog and standard cell blocks** including Op-Amps with common-centroid matching, BGRs, DACs, PLLs, and D-Flipflops achieving **zero DRC/LVS violations** across both technology nodes.
- Collaborated with schematic design to optimize transistor parameters including modifying finger count and multipliers achieving **15-20% layout area reduction** while maintaining device matching specifications.
- Applied advanced layout techniques including common-centroid/interdigitation matching, strategic dummy device placement to mitigate WPE (Well Proximity Effect) and STI (Shallow Trench Isolation) stress effects, and implemented shielding, guard rings, and deep N-well isolation for latch-up prevention.

Intern | NSIC (National Small Industries Corporation), Hyderabad (May 2023 – June 2023)

- Designed and assembled a prototype for an RFID-based locker system, integrating microcontrollers with RF readers and actuators and also enhanced with SIM 800C GSM Module.

KEY PROJECTS

Analog & Standard Cell Layout (45nm CMOS) | MosChip Training

- Executed complete layout with GDSII generation for Op-Amp (common-centroid matching), BGR, DAC, PLL, standard cells (INVERTER,NAND, NOR,AND,OR,MUX, D-FF), and Level Shifter utilizing deep N-well isolation with iterative schematic-layout optimization for performance and area trade-offs across **45nm technology node.**

Cryptographic RNB Multiplier (90nm CMOS and TRANSMISSION LOGICS) | B.Tech Project

- Designed schematic architecture for SISO (Serial-In Serial-Out), SIPO (Serial-In Parallel-Out), PISO (Parallel-In Serial-Out), PIPO (Parallel-In Parallel-Out) configurations of RNB (Reordered Normal Basis) multiplier with Transmission and CMOS logic styles in Cadence Virtuoso with functional validation.

EDUCATION AND CERTIFICATION

B.Tech, Electronics & Communication Engineering | Sreyas Institute of Engineering & Technology | 2024 | 6.85 CGPA

Intermediate | Narayana Junior College, Hyderabad | 2020 | 84%

School |Dilsukhnagar Public School, Hyderabad | 2018 | 87%

Certifications: NPTEL - CMOS Digital VLSI Design, Embedded System Design, Digital Communication, Etc.

TECHNICAL SKILLS

- **Layout & Verification:** Cadence Virtuoso, Cadence PVS (Physical Verification System), Cadence Assura | DRC (Design Rule Check), LVS (Layout Versus Schematic), ERC (Electrical Rule Check), Antenna Checks, Latch-up Analysis
- **Advanced Techniques:** Common-Centroid Matching, Interdigitation, Guard Rings, Deep N-well Isolation, Shielding, Parasitic Mitigation, Crosstalk Reduction, Dummy Device Placement, Multi-finger Optimization, Layout-Dependent Effects (LDE) Mitigation
- **Schematic-Layout Co-Optimization:** Transistor finger/multiplier tuning, dummy device strategic placement for WPE (Well Proximity Effect) mitigation, back-annotation for design collaboration
- **Technology Nodes:** 45nm and 90nm.
- **Analog/Standard Blocks:** Op-Amp, BGR, DAC, PLL, Level Shifter, Standard Cells (NAND, NOR, MUX, D-FF).
- **Languages and Environment:** SKILL, Bash, Linux, Windows.

PROFESSIONAL SUMMARY

Analog Layout Engineering Trainee with practical experience in full-custom IC layout (schematic-to-GDSII) for 45nm CMOS technologies using Cadence Virtuoso. Trained in converting schematic designs of analog blocks such as Op-Amps, Bandgap References (BGR), Phase-Locked Loops (PLL), ADC/DACs, and standard cells into physical layouts that meet strict verification standards (DRC, LVS, antenna, ERC). Exposure to advanced matching, parasitic minimization, latch-up prevention, dummy device placement, guard ring implementation, deep N-well isolation, slotting, metal fill, and ESD/antenna protection. Developed a strong understanding of schematic-layout co-optimization, layout-dependent effects (WPE, STI), area/density optimization, signal integrity concepts, and collaborating with verification teams. Ready to apply these skills to deliver effective layouts and learn best practices in top MNC environments.