TWO STAGE RC COUPLED AMPLIFIER

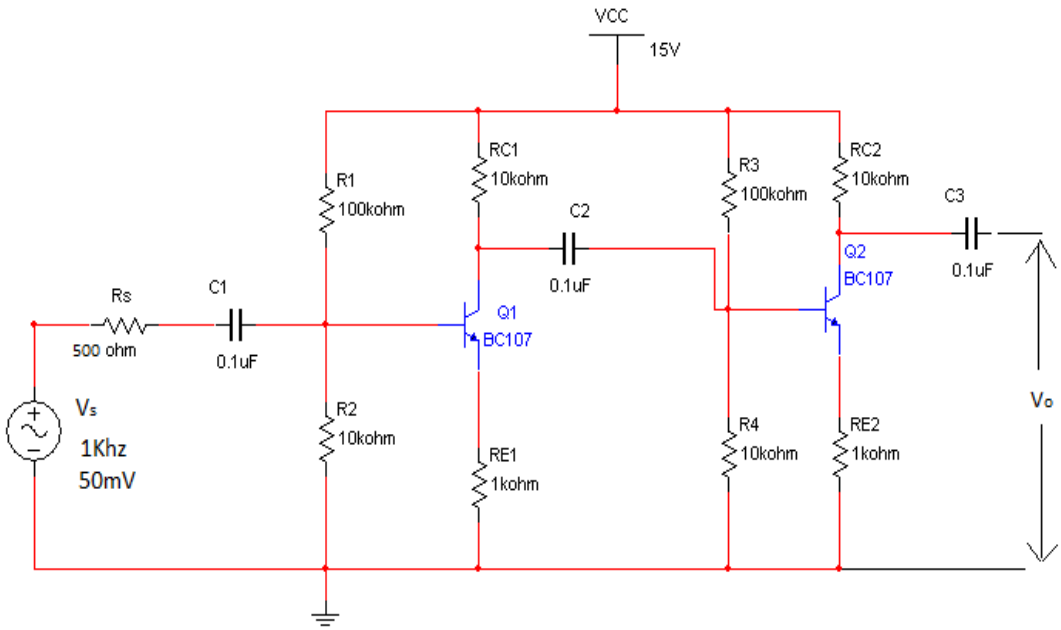
AIM:

1. To study the Two-stage RC coupled amplifier.
2. To measure the Mid band voltage gain of the amplifier at 1KHz.
3. To obtain the frequency response characteristic and the band width of the amplifier.

APPARATUS:

1. Two stage RC coupled amplifier trainer.
2. Function Generator.
3. C.R.O
4. Connecting patch cords.

CIRCUIT DIAGRAM:



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PROCEDURE:

1. Switch ON the power supply.
2. Connect the function generator with sine wave input 50mVp-p, 1Khz frequency at the input terminals.
3. Connect the C.R.O at output terminals.
4. Measure the voltage at the second stage of amplifier.
5. Now vary the input frequency from 10Hz to 1MHz in steps, and for every value of input frequency note the output voltage keeping the input amplitude at constant value.
6. Calculate the gain magnitude of the amplifier
7. Plot a graph of frequency versus gain (dB) of the amplifier. Sample frequency response graph is as shown in fig. Below.

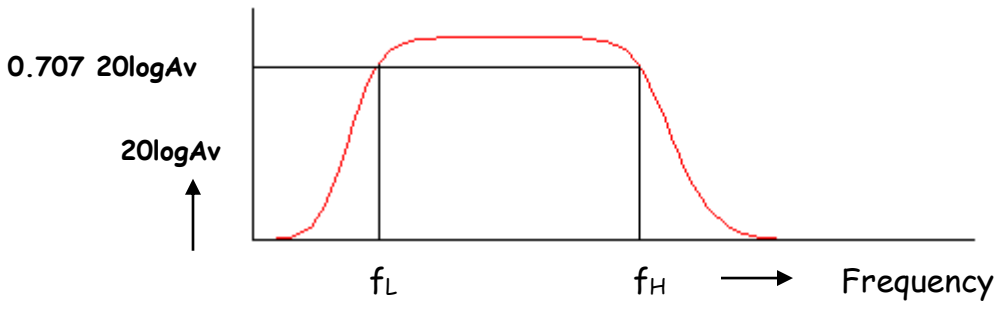
CALCULATIONS:

1. Cut off frequencies f_H = f_L=
2. Band Width, BW = $f_H - f_L$,
3. Mid band $\text{Voltage Gain } (A_{VS}) = \frac{\text{Output Voltage } (V_o)}{\text{Source Voltage } (V_S)}$ =

OBSERVATION: V_s = 50mV(p-p)

Frequency (Hz)	V_O (volts)	Gain=V_o/V_s	Gain in dB =20 log (V_o/V_s)dB

EXPECTED GRAPH:



RESULT:

Reasoning Questions

1. What are the advantages and disadvantages of multi-stage amplifiers?
2. Why gain falls at HF and LF?
3. Why the gain remains constant at MF?
4. Explain the function of emitter bypass capacitor, Ce?
5. How the band width will effect as more number of stages are cascaded?
6. Define frequency response?
7. Give the formula for effective lower cut-off frequency, when N-number of stages are cascaded.
8. Explain the effect of coupling capacitors and inter-electrode capacitances on overall gain.
9. By how many times effective upper cut-off frequency will be reduced, if three identical stages are cascaded?
10. Mention the applications of two-stage RC-coupled amplifiers.

NON-LINEAR WAVE SHAPING CIRCUITS
CLIPPERS

AIM:

a) To study the clipping circuits using diodes
b) To observe the transfer characteristics of all the clipping circuits in CRO.

APPARATUS:

1. Function Generator
2. Bread board
3. CRO
4. DC power supply (dual)
5. Resistors (2.2 KΩ)
6. Diodes (1N4007)
7. Connecting wires
8. CRO Probes

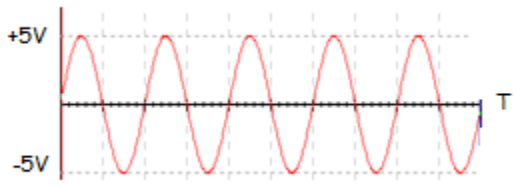
THEORY:

Clipping circuits basically limit the amplitude of the input signal either below or above certain voltage level. They are referred to as Voltage limiters, Amplitude selectors or Slicers. A clipping circuit is one, in which a small section of input waveform is missing or cut or truncated at the out put section.

Clipping circuits are classified based on the position of Diode.

1. Series Diode Clipper
2. Shunt Diode Clipper

Input Wave Form



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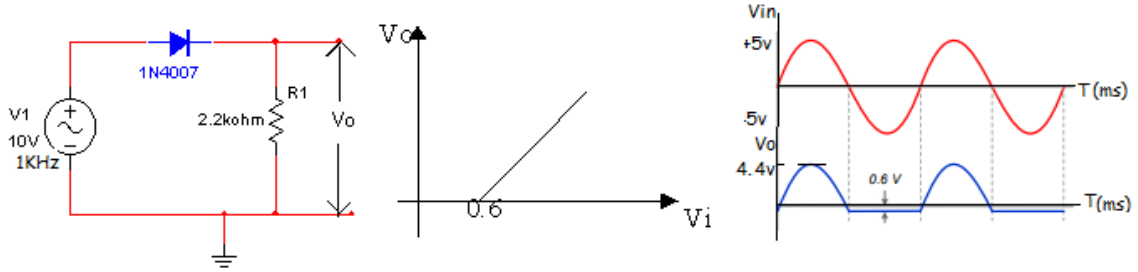
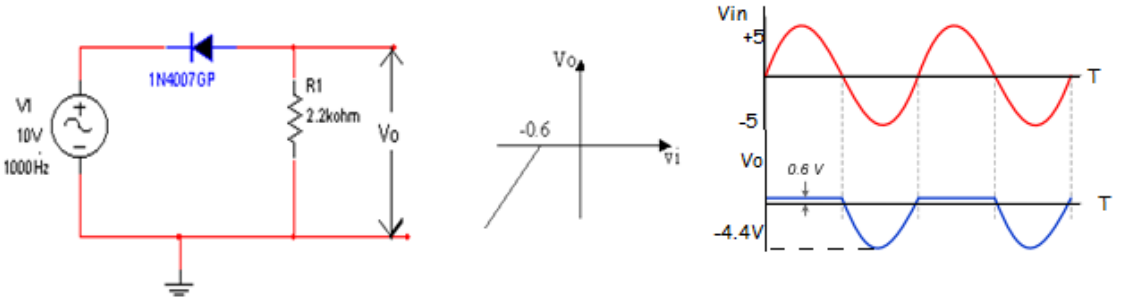
CIRCUIT DIAGRAM	TRANSFER CHARACTERISTICS	O/P WAVEFORMS

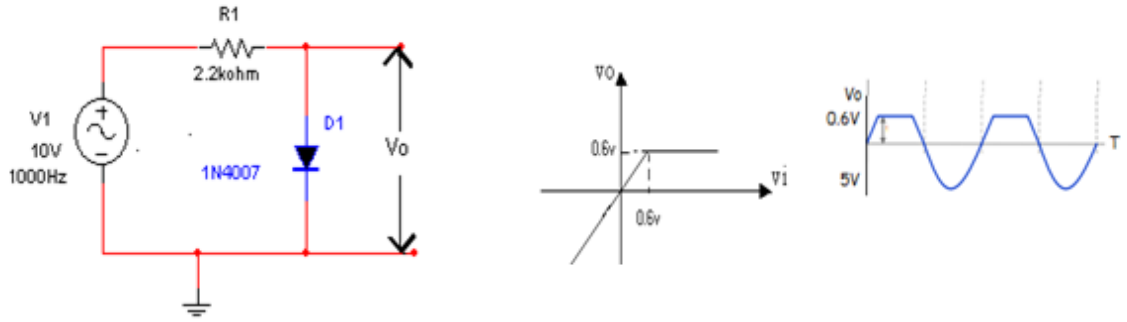
1. Series –ve clipper



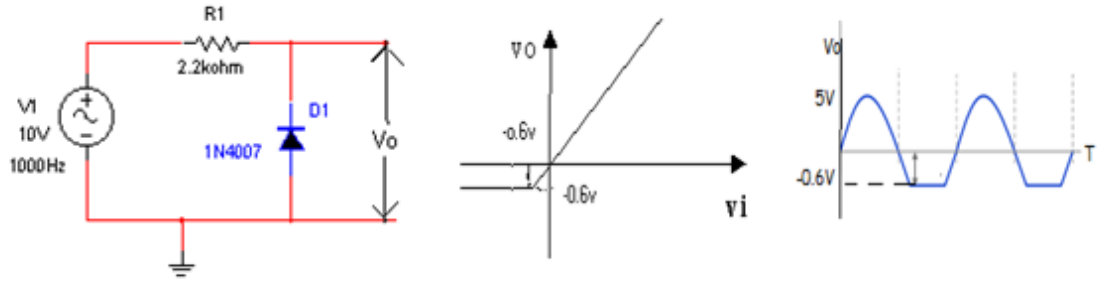
2. Series +ve clipper



3. Shunt +ve clipper

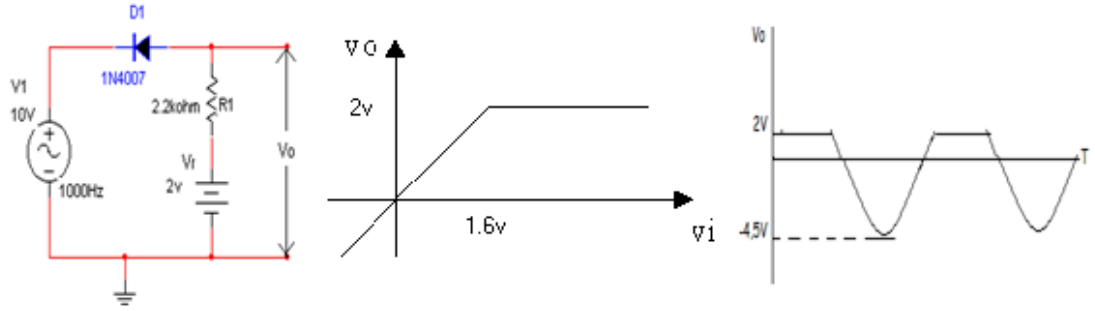


4. Shunt -ve clipper

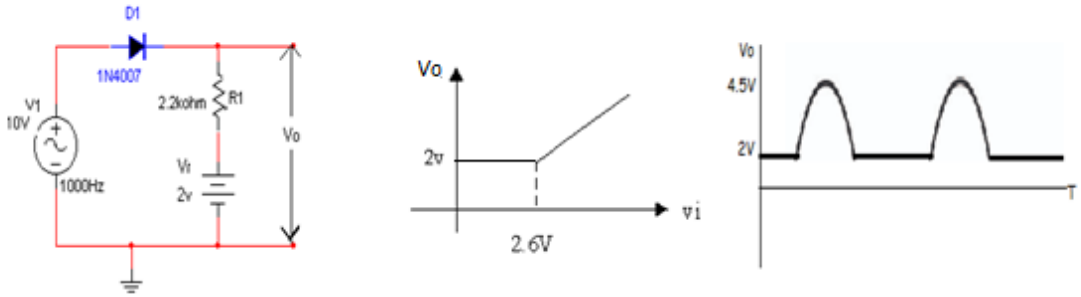


CIRCUIT DIAGRAM **TRANSFER CHARACTERISTICS** **O/P WAVEFORMS**

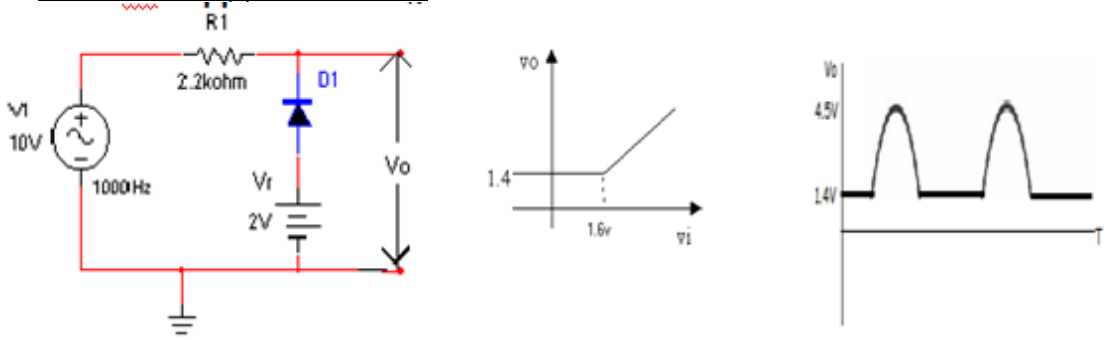
5. Series +ve clipper with $+V_R$



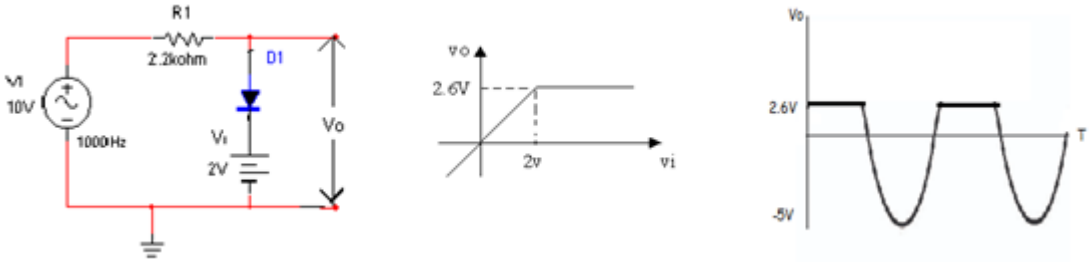
6. Series -ve clipper with $+V_R$



7. Shunt -ve clipper with $+V_R$

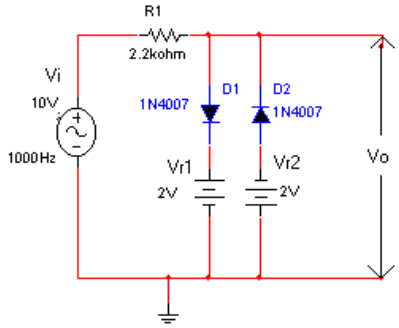


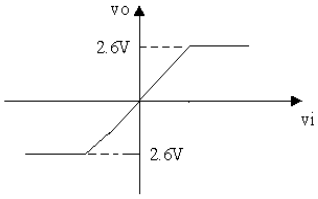
8. Shunt +ve clipper with $+V_R$

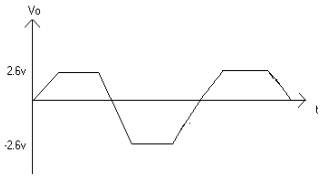


CIRCUIT DIAGRAM | **TRANSFER CHARACTERISTICS** | **O/P WAVEFORMS**

9. Double diode clipper







PROCEDURE:

1. Connect the circuit as shown in fig.1
2. In each case apply 10 V_{P-P}, 1KHz Sine wave I/P using a signal generator.
3. Observe the O/P waveform in DC mode on the CRO in comparison with I/P waveform.
4. Sketch the I/P as well as O/P waveforms and mark the numerical values.
5. Note the changes in the O/P due to variations in the reference voltage V_R = 2V.
6. O/P is taken across the load R_L.
7. To Obtain the transfer characteristics for all the figures follow the procedure.
8. Apply input to the X-Channel(CH2), Output to Y-Channel(CH1), then select XY mode button in the CRO.
9. Keep both the channels (CH1 & CH2) in GND position, adjust the dot at the center of the CRO screen. then release ground button and plot the transfer characteristics.
10. Repeat the above steps for all the figures.

PRECAUTIONS:

1. Set the CRO O/P channel in DC mode always.
2. Observe the waveform simultaneously by keeping common ground.
3. See that there is no DC component in the I/P.

4. To find transfer characteristics apply input to the X-Channel(CH2), O/P to Y-Channel(CH1), Both the channels modes must be in ground, adjust the dot at the center of the screen when CRO is in X-Y mode. Then release ground switch and plot the transfer characteristics.

RESULT:

Reasoning Questions

1. What is a clipping circuit?
2. What is piecewise linear mode of a diode?
3. What is a break region?
4. What is the significance of zero slope?
5. In a clipper circuit what is the function of non-linear device.
6. Compare the Series & Shunt Clippers.

NON-LINEAR WAVE SHAPING CIRCUITS
CLAMPERS

AIM: To study the clamping circuits using diodes and capacitors.

APPARATUS:

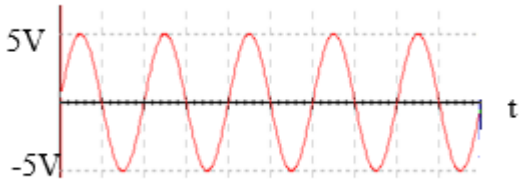
1. Function Generator.
2. Bread board
3. CRO
4. DC power supply (dual)
5. Resistors (100 KΩ)
6. Diodes (1N4007)
7. Capacitor (0.1μf)
8. Connecting Wires
9. CRO Probes

THEORY:

Clamping circuits add a DC level to an AC signal. A clamper is also refer to as DC restorer or DC re-inserter. The Clampers which clamp the given waveform either above or below the reference level, which are known as positive or negative clamping respectively.

I/P WAVEFORM

Vi=10V



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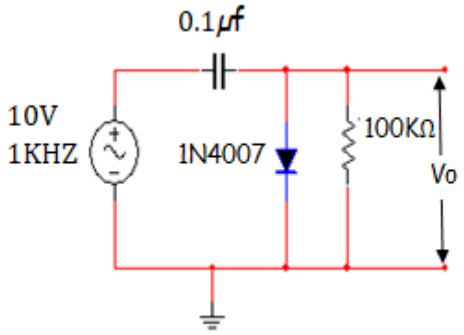
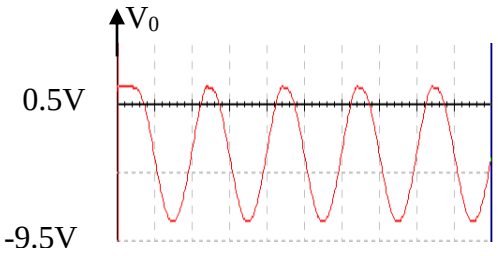
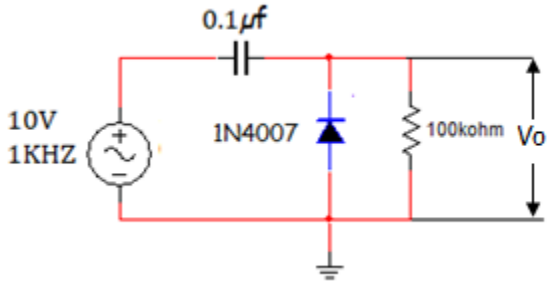
CIRCUIT DIAGRAM **O/P WAVEFORMS**

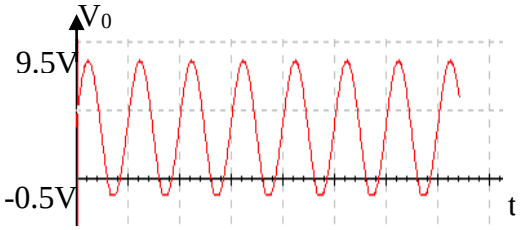
1. Negative Clamper



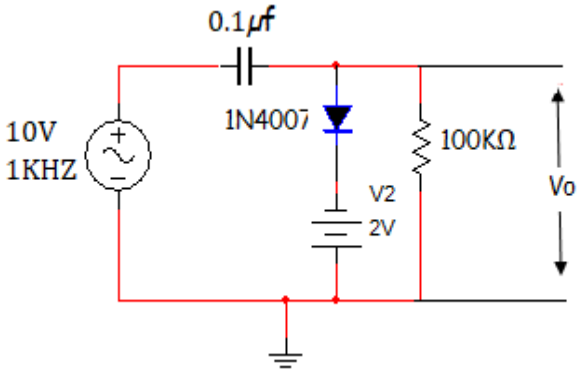


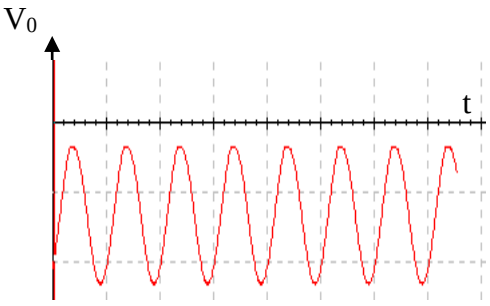
2. Positive Clamper



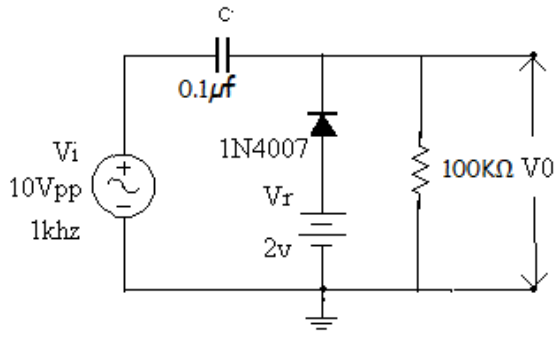


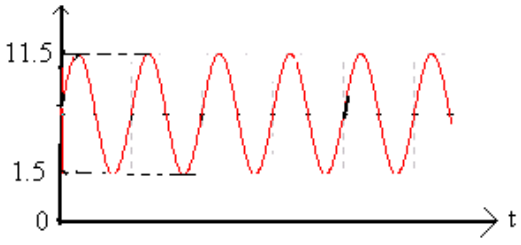
3. Negative clamper with -ve reference voltage



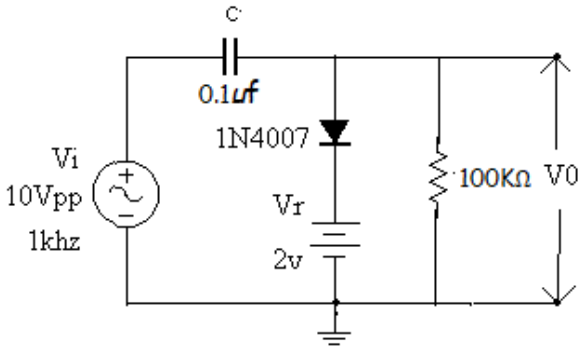


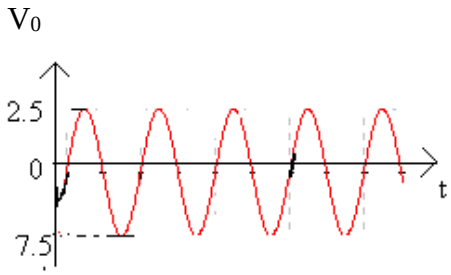
4. Positive clamper with +ve reference voltage



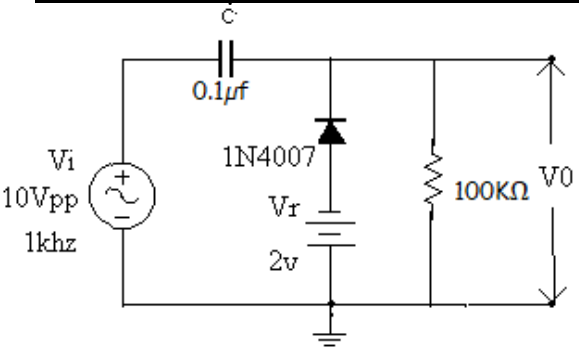


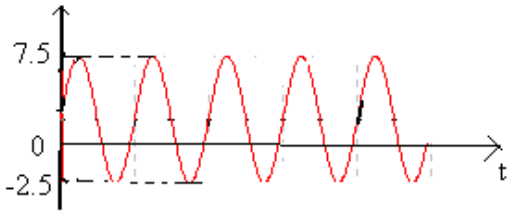
5. Negative clamper with +ve reference voltage





6. Positive clamper with -ve reference voltage





PROCEDURE:

1. Connect the circuit as shown in fig.1.
2. Apply a Sine wave of $10V_{P-P}$, 1 KHz at the input terminals with the help of Signal Generator.
3. Observe the I/P & O/P waveforms of CRO and plot the waveforms and mark the values with V_R = 2 V.
4. O/P is taken across the load R_L.
5. Repeat the above steps for all clamping circuits as shown.

RESULT:

Reasoning Questions

1. What is clamping circuit?
2. What are the applications of clamping circuits?
3. What is the synchronized clamping?
4. Why a clamper is called a dc inserter?
5. What is clamping circuit theorem. How does the modified clamping circuit theorem differ from this?
6. Differenciate –ve clamping circuit from +ve clamping circuits in the above circuits.
7. Describe the charging and discharging of a capacitor is each circuit.

BISTABLE MULTIVIBRATOR

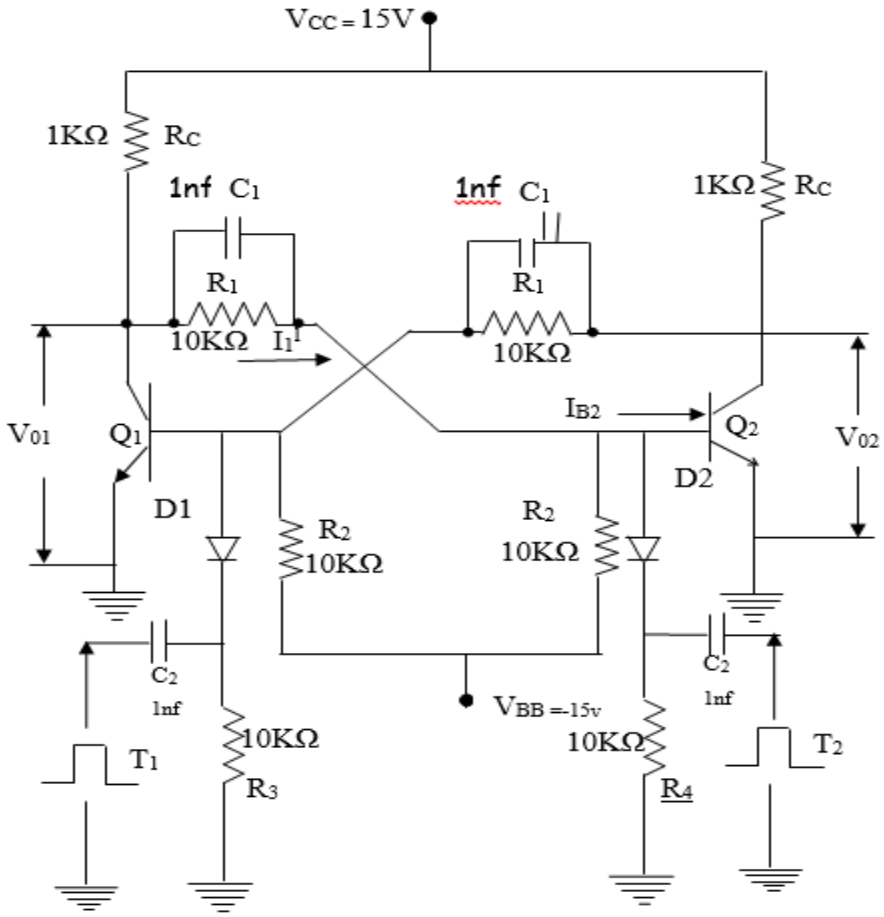
AIM:

a) Design the Bi-stable Multivibrator circuit and verify the operation.
b) Obtain the resolving time of Bi-stable Multivibrator and verify theoretically. Choose C = 1nf, V_{CESat} = 0.2V, I_{Cmax} = 15mA, V_{CC} = 15V, V_{BB} = -15V.

APPARATUS:

1. Bi-stable Multivibrator trainer kit
2. Function Generator
3. CRO
4. Connecting patch chords

CIRCUIT DIAGRAM:



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DESIGN:

$R_C = \frac{V_{CC} - V_{CESat}}{I_{C\max}} = (15 - 0.2) / 15mA \cong 1K\Omega$

$I_4 = 0.1\ Ic\ max = 0.1 \times 15mA = 1.5mA$

$R_2 = \frac{V_{BE(sat)} + V_{BB}}{I_4} = (0.7 + 15) / 1.5mA = 10.4K\Omega \cong 10K\Omega$

$I_{B2(min)} = I_{C2} / h_{fe} = 15mA/150 = 0.1mA$

$I_{B2} = 1.5\ I_{B2(min)} = 1.5(0.1mA) = 0.15mA$

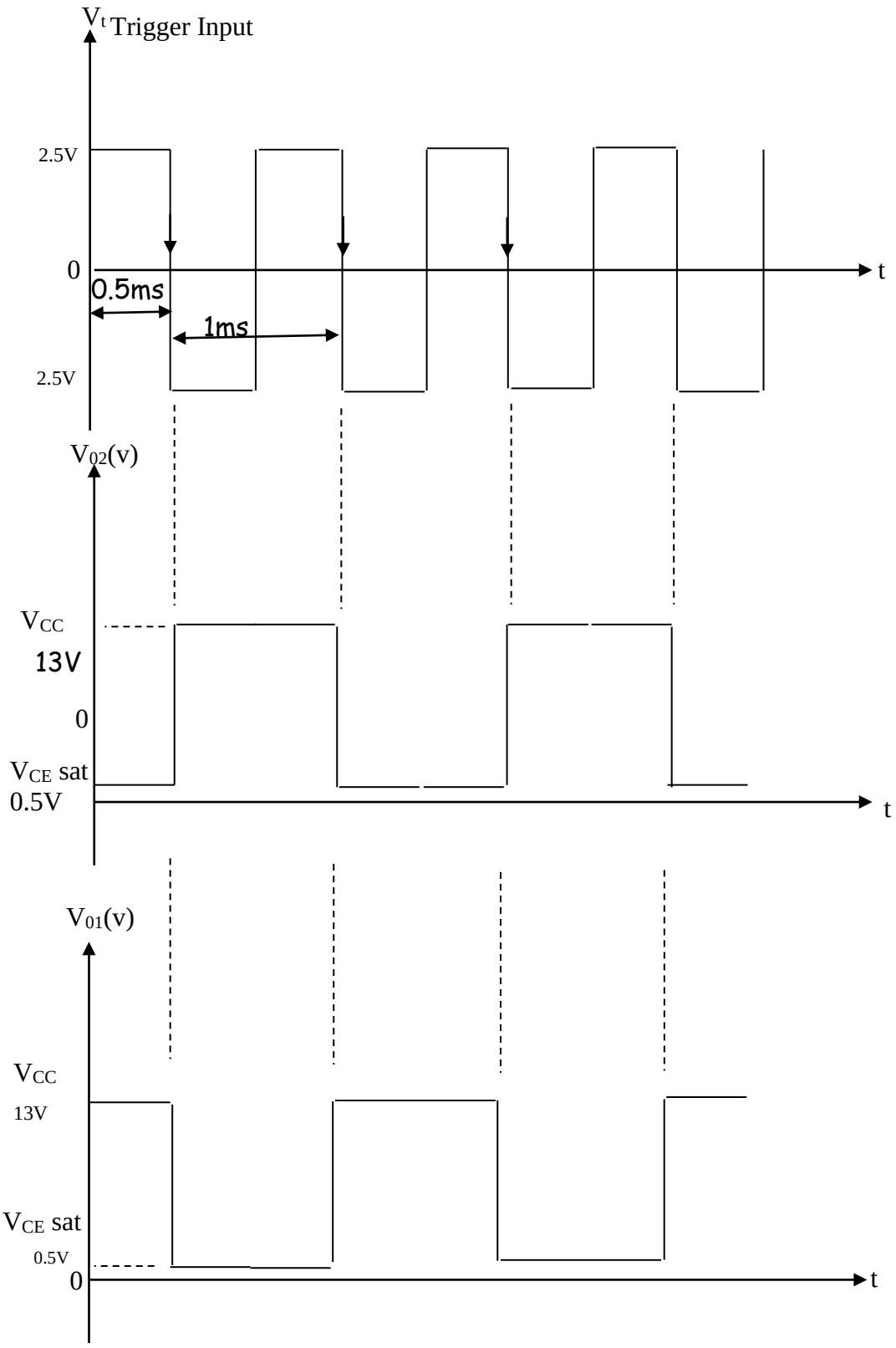
$I_1^{l} = I_{B2} + I_4 = 0.15mA + 1.5mA = 1.65mA$

$R_1 = \frac{Vcc - V_{BE(sat)}}{I_1^{l}} = (15\text{-}0.6)/1.65mA = 8.7K\Omega \quad R_1 \cong 10K\Omega$

PROCEDURE:

1. Switch ON the system and observe for the power LED indication.
2. Apply two Square waves (trigger I/P) 5Vp-p, 1KHz frequency at terminals T_1 & T_2. Observe both I/P & O/P waveforms on CRO in DC mode.
3. Now slowly increase the frequency and at one particular frequency the circuit does not respond and the output disappears. Just lesser than this frequency, the circuit again responds, this is the maximum allowable frequency.
4. Sketch the O/P waveforms, sample O/P waveforms are as shown in figure.

EXPECTED WAVEFORMS:



RESULT:

Reasoning Questions

1. What are the applications of a Bistable multivibrator?
2. Describe the operation of commutating capacitors.
3. Why a Binary is also called a flip flop?
4. Mention the name of different kind of triggering is used in the circuit shown?
5. What are the disadvantages of Direct Coupled Binary?
6. How many types of unsymmetrical triggering are there?

MONOSTABLE MULTIVIBRATOR

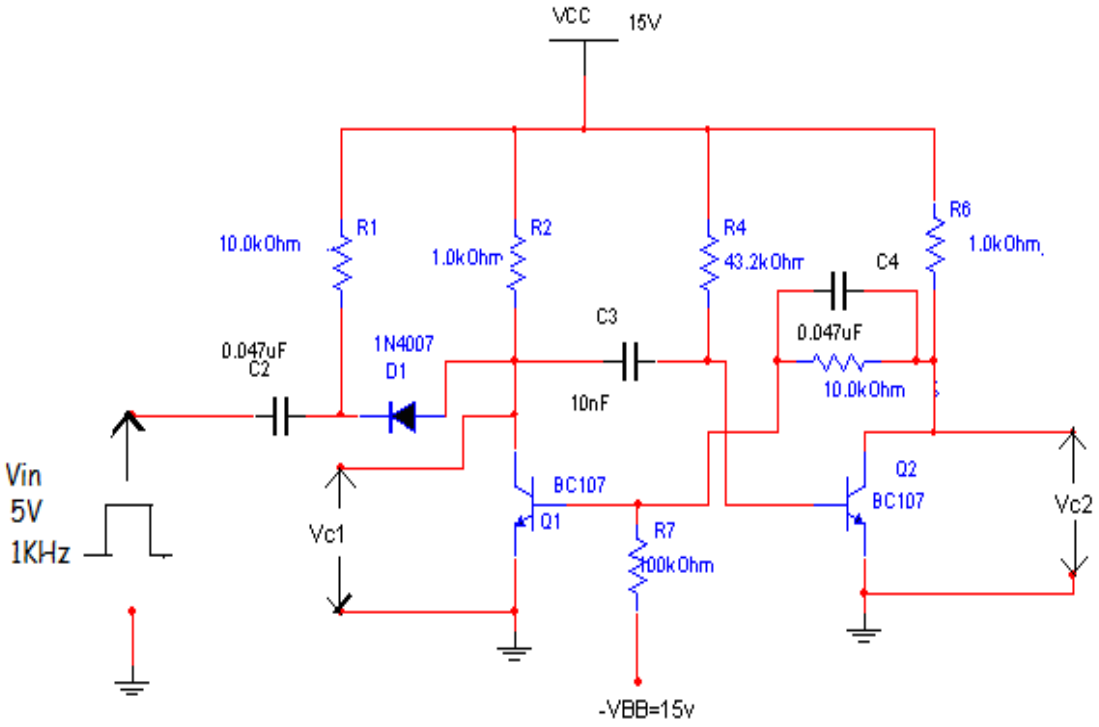
AIM:

To design a monostable multivibrator for the Pulse width of 0.3mSec. choose I_{Cmax} = 15mA, V_{CC} = 15V, V_{BB} = 15V, R_1 = 10KΩ and take the margin of –1.18V to keep the OFF Transistor in OFF state when no trigger is applied.

APPARATUS:

1. Monostable Multivibrator trainer kit
2. Function Generator
3. CRO
4. Connecting patch cards

CIRCUIT DIAGRAM:



Lab Incharge **HOD, ETE**

DESIGN:

T = 0.69 RC

Choose C = 10nf

0.3×10^{-3}Sec = $0.69 \times R \times 10 \times 10^{-9}$

R = 43.47 KΩ

Choose Icmax = 15mA

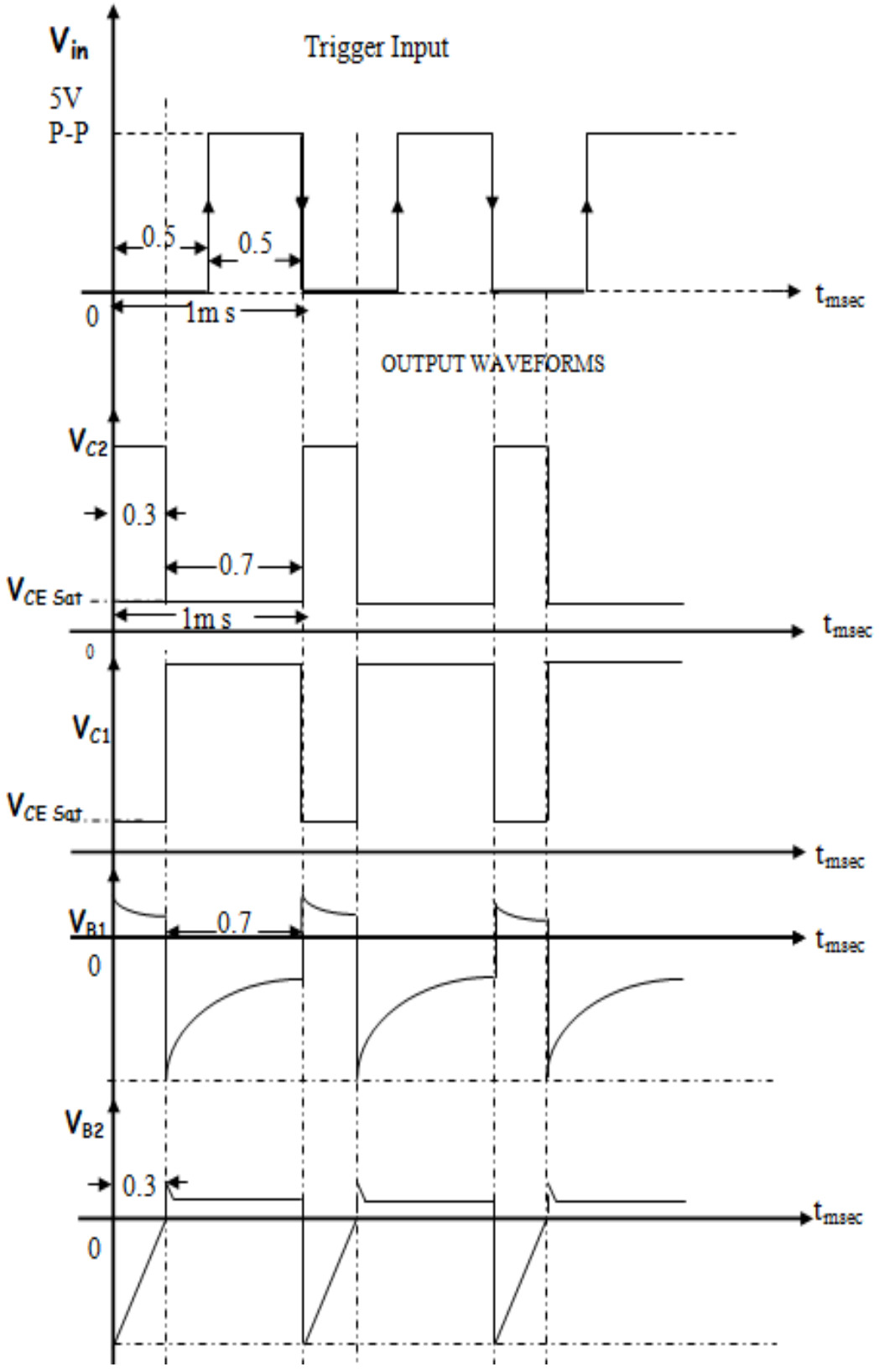
$R_C = \frac{V_{CC} - V_{CESat}}{I_{C\max}}$

R_C = (15 – 0.2) / 15mA ≅ 1KΩ

PROCEDURE:

1. Switch ON the trainer kit and observe power indication.
2. Wire the circuit as shown in the circuit diagram
3. Apply the triggering input to the circuit 1Khz, 5V and to the CRO's channel 1 to observe the input waveform. Apply Monostable O/P to the Channel 2 of the CRO.
4. Adjust the triggering pulse frequency to get stable pulse on the CRO and now measure the pulse width.
5. Obtain waveforms at different points like V_{B1}, V_{B2}, V_{C1} & V_{C2}.

EXPECTED WAVE FORMS:



RESULT:

Reasoning Questions

1. What are applications of Monostable Multivibrator?
2. Why a Monostable Multivibrator is called a going circuit?
3. Which change of state requires a triggering signal?
4. Explain the wave form of V_{B1}.
5. Describe the operation of the capacitor C3 in the circuit.
6. Why is the time period T also called Delay time?

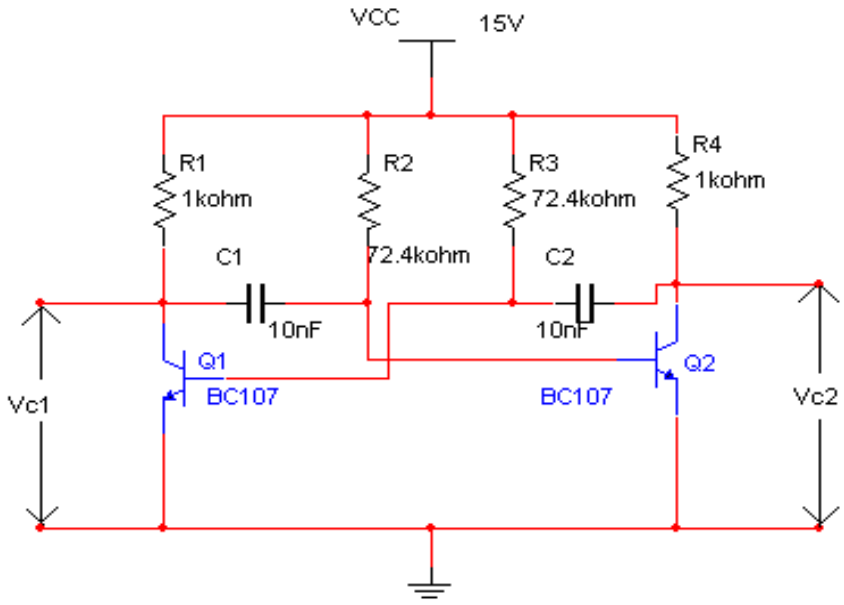
ASTABLE MULTIVIBRATOR

AIM: To design an Astable Multivibrator to generate a Square wave of 1KHz frequency. Choose C = 10nf.

APPARATUS:

1. Astable multivibrator trainer Kit
2. Function Generator
3. CRO
4. Connecting Patch Chords

CIRCUIT DIAGRAM:



THEORY:

The astable circuit has two quasi-stable states. Without external triggering signal the astable configuration will make successive transitions from one quasi-stable state to the other. The astable circuit is an oscillator. It is also called as free running multivibrator and is used to generate "Square Wave".

Lab Incharge **HOD, ETE**

DESIGN:

The period T is given by

$T = T_1 + T_2 = 0.69 (R_1C_1 + R_2C_2)$

For symmetrical circuit with $R_1 = R_2 = R$ & $C_1 = C_2 = C$

Let F = 1KHz

T = 1ms

$T = 1.38\ RC$

$10^{-3} = 1.38 \times R \times 10 \times 10^{-9}$

$R = \frac{10^{-3}}{1.38x10x10^{-9}} = 72.4K\Omega$ (when c=10nf)

Let VCC = 15V; hfe = 51 (for BC107)

$V_{BE\ Sat} = 0.7V$; $V_{CESat} = 0.3V$

Choose $I_{C\ max} = 10mA$,

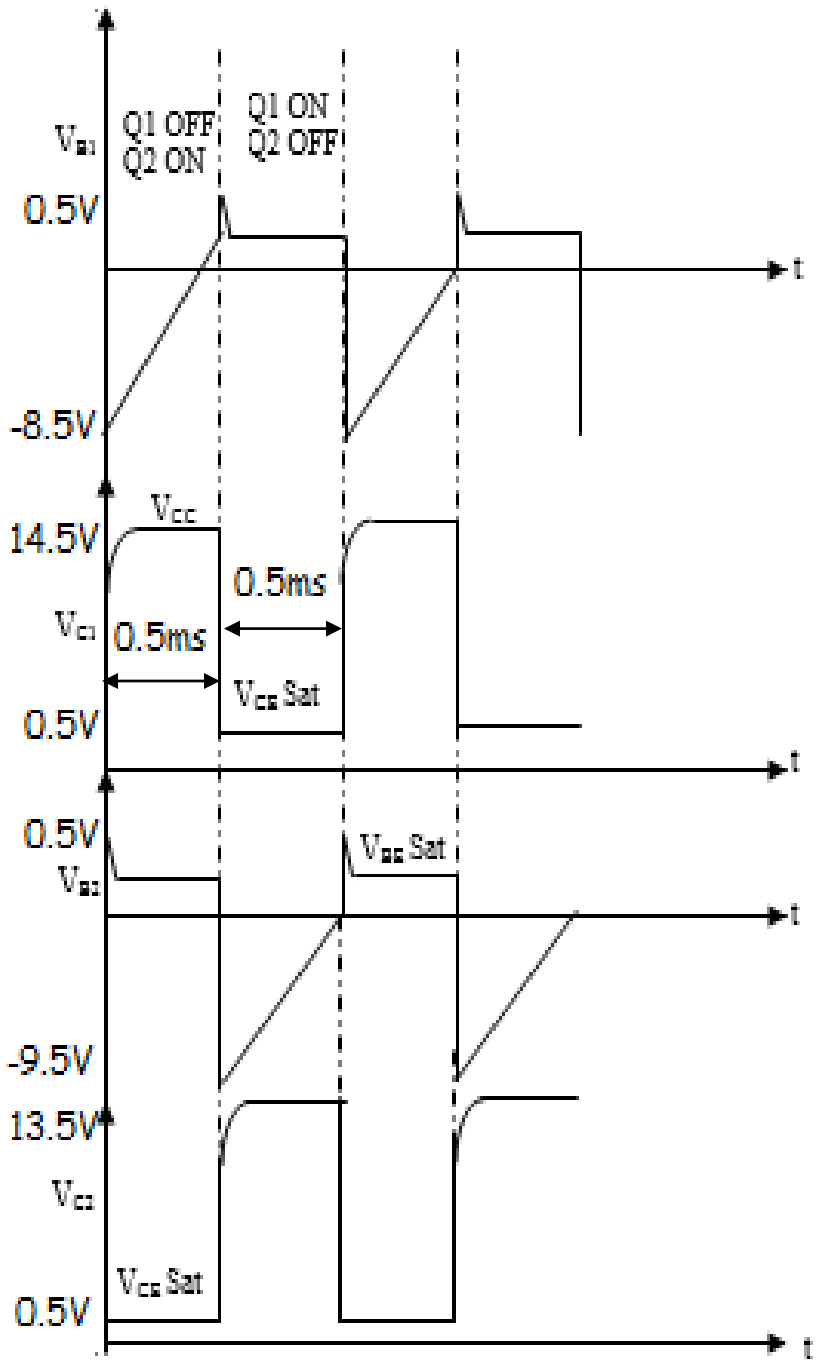
$R_C = (V_{CC} - V_{CESat}) / I_{Cmax} = (15 - 0.3) / (10 \times 10^{-3}) = 1.47K\Omega$

$\therefore R_C \cong 1K\Omega$

PROCEDURE:

1. Connect the circuit as shown in figure.
2. Observe the Output waveforms at Base and Collector terminals of Q_1 & Q_2 on CRO in DC mode and plot them.
3. Verify the frequencies theoretically.

EXPECTED WAVEFORMS:



RESULT:

Reasoning questions

1. Is it possible to change time period of the waveform without changing R & C? Support your answer?
2. Collector waveforms are observed with rounded edges. Explain?
3. Explain charging and discharging of capacitors in an Astable Multivibrator?
4. How can an Astable multivibrator be used as VCO?
5. Why do you get overshoots in the Base waveforms?
6. What are the applications of Astable Multivibrator?
7. How can Astable Multivibrator be used as a voltage to frequency converter?
8. What is the formula for frequency of oscillations?
9. What are the other names of Astable multivibrator?

SCHMITT TRIGGER

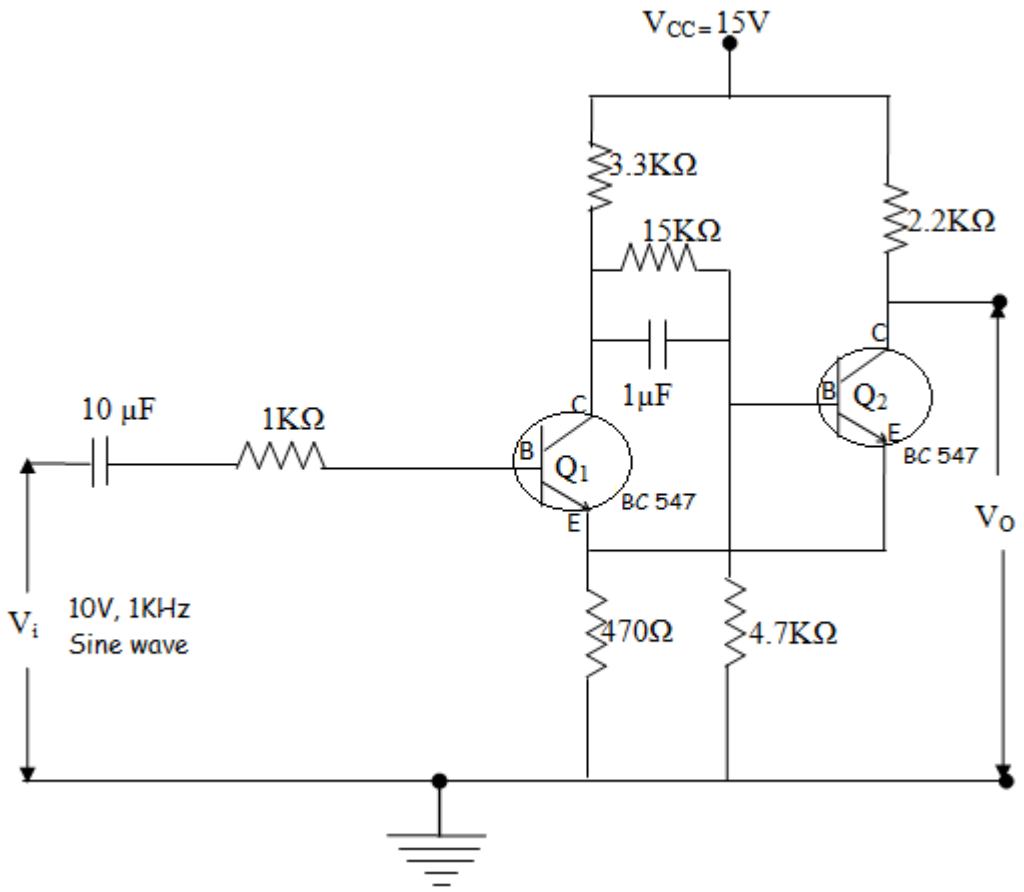
AIM:

(a) To design the Schmitt trigger circuit and obtain the UTP and LTP values.
(b) To obtain square wave from the sine wave input.

APPARATUS:

(1) Schmitt Trigger Trainer Kit.
(2) Function Generator
(3) C.R.O
(4) Connecting patch chords
(5) CRO Probes

CIRCUIT DIAGRAM:



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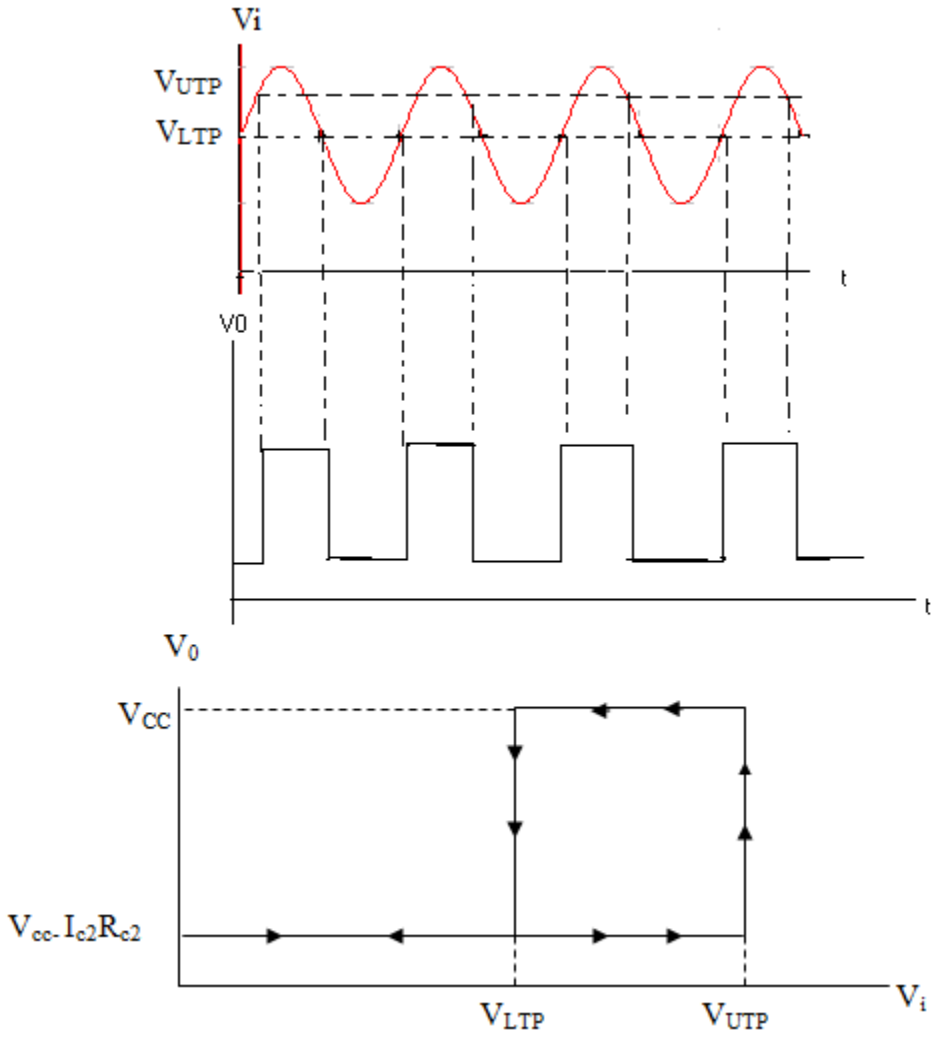
PROCEDURE:

(1) Switch ON the trainer Kit.
(2) Apply a sine wave input 10Vp-p, 1 KHz frequency to the circuit.
(3) Short circuit from C_1 to R_1 and to R_E
(4) When Vi is increasing, Q_1 goes from OFF to ON and Q_2 from ON to OFF.
(5) When Vi is decreasing, Q_1 goes from ON to OFF and Q_2 from OFF to ON.
(6) Observe and note down the input and output waveforms (in DC mode).
(7) Measure UTP & LTP values at output of Q_2

EXPECTED WAVEFORMS:



RESULT:

Reasoning Questions

1. What are applications of Schmitt Trigger?
2. Define hysteresis action?
3. Why a Schmitt Trigger called a squaring circuit?
4. What is UTP?
5. What is LTP?
6. What is the Difference between a Binary and Schmitt Trigger?

ADDER AND SUBTRACTOR USING OP-AMP 741

AIM: To Implement and study the mathematical operations such as Adder and Subtractor using IC 741 Op-amp.

APPARATUS:
1. Universal Bread Board Trainer Kit.
2. IC 741,100KΩ -5no.
3. Digital Multimeter, 20MHz CRO.
4. Patch Chords.

THEORY:

Summing Amplifier: Op-amp may be used to perform summing operation of several input signals in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively.

Subtractor: The basic difference amplifier can be used as a subtractor. The signals to be subtracted are connected to opposite polarity inputs i.e. in inverting or non-inverting terminals of the op-amp.

CIRCUIT DIAGRAM:

ADDER:

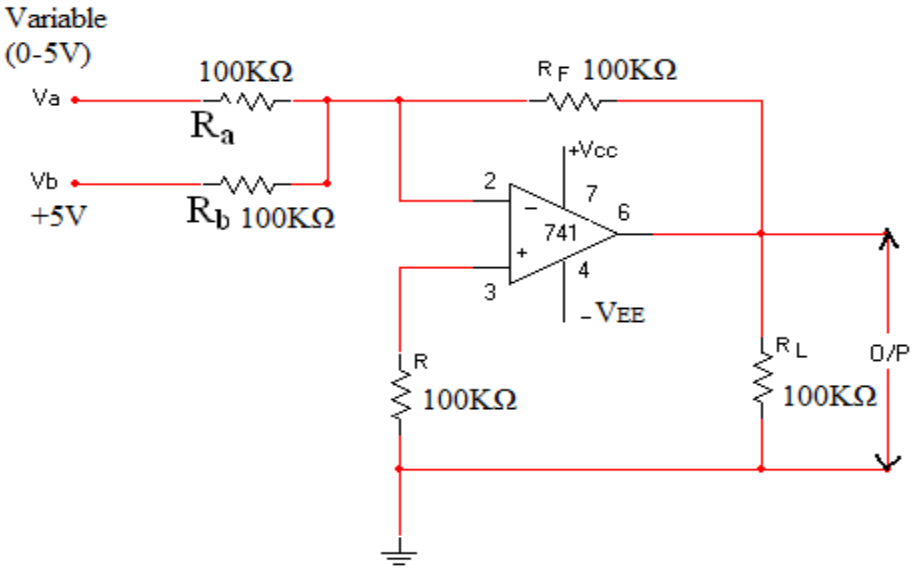


Fig (1)

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SUBTRACTOR:

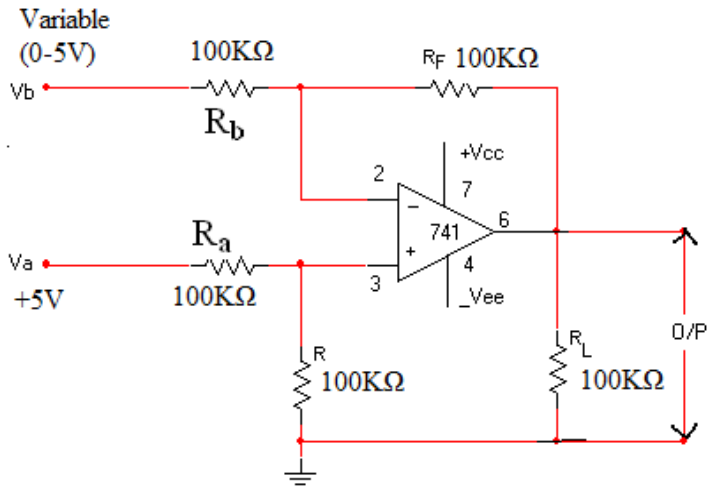


Fig (2)

PROCEDURE:

1. Connect the Adder circuit as shown in figure (1) and switch ON the trainer.
2. Apply the input voltages from the regulated supplies to the corresponding inputs.
3. Connect the voltmeter at the Output terminals, and note down the values and verify with theoretical values.
4. Repeat the above steps for different input voltages.
5. Now connect the subtractor circuit as shown in figure (2).
6. Repeat steps 2&3 and record the values.
7. Repeat the above steps for different input voltages.

CALCULATIONS:

ADDER:

The following assumptions must be taken into consideration for 741-Op-amp

1) V_{id}= 0V
2) Op-Amp draws no current i.e. $I_B^+ = I_B^- = 0A$

$$I = \frac{V_a}{R_a} + \frac{V_b}{R_b}$$

$V_O = - R_F I$

$$\Longrightarrow V_O = - R_F \left(\frac{V_a}{R_a} + \frac{V_b}{R_b} \right)$$

If $R_a = R_b$

$$V_O = - \frac{R_F}{R_a} (V_a + V_b) \qquad \text{-------I}$$

Verify whether the theoretical value is approximately equal to Practical value.

SUBTRACTOR

If $R_a = R_b$

$V_{Non-Inv} = V_a$, $V_{Inv} = V_b$

$$V_O = + \frac{R_F}{R_a} (V_{NonInv} - V_{Inv})$$

OBSERVATIONS:

ADDER

Inputs Voltages		Output Voltage V_o	
		Theoretical $V_o = -\frac{R_f}{R_a}(V_a + V_b)$	Practical (CRO/DMM)
V_a	V_b		

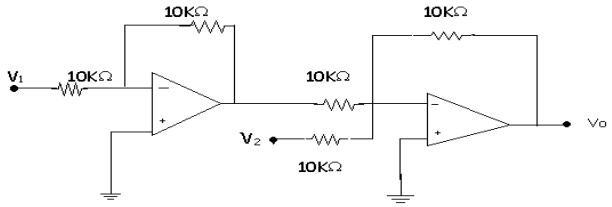
SUBTRACTOR

Inputs Voltages		Output Voltage V_o	
V_{Inv}	$V_{Non-Inv}$	Theoretical $V_O = \frac{Rf}{Ra}(V_{NonInv} - V_{Inv})$	Practical (CRO/DMM)

RESULT:

Reasoning questions:

1. Draw an Op- amp circuit whose output Vo is $V_1 + V_2 - V_3 - V_4$.
2. Calculate V_O for the above circuit for $V_1 = 5V$, $V_2 = 2V$.



3. Show that the o/p of Inverting adder is $V_0 = -\frac{R_f}{R_1}(v_a + v_b + v_c + -----$

4. Draw the circuit of non-inverting adder with 3 inputs and find the o/p voltage V_0
5. What is a mixed adder and how do you construct using Op-Amp IC 741.
6. Design a mixed adder for $V_0 = V_1 + 2V_2 - V_3 - 5V_4$.
7. Design a subtractor for $V_0 = V_a - 5V_b - 2Vc$.
8. Mention the other mathematical operations obtained using Op-Amps.

INTEGRATOR AND DIFFERENTIATOR USING OP-AMP 741

AIM: To analyze and design the Integrator& Differentiator using op-amp IC 741.

APPARATUS: 1. Integrator & Differentiator trainer kit,
2.1MHz Function generator,
3. 20MHz oscilloscope,
4. Connecting patch chords.

CIRCUIT DIAGRAM:

Integrator:

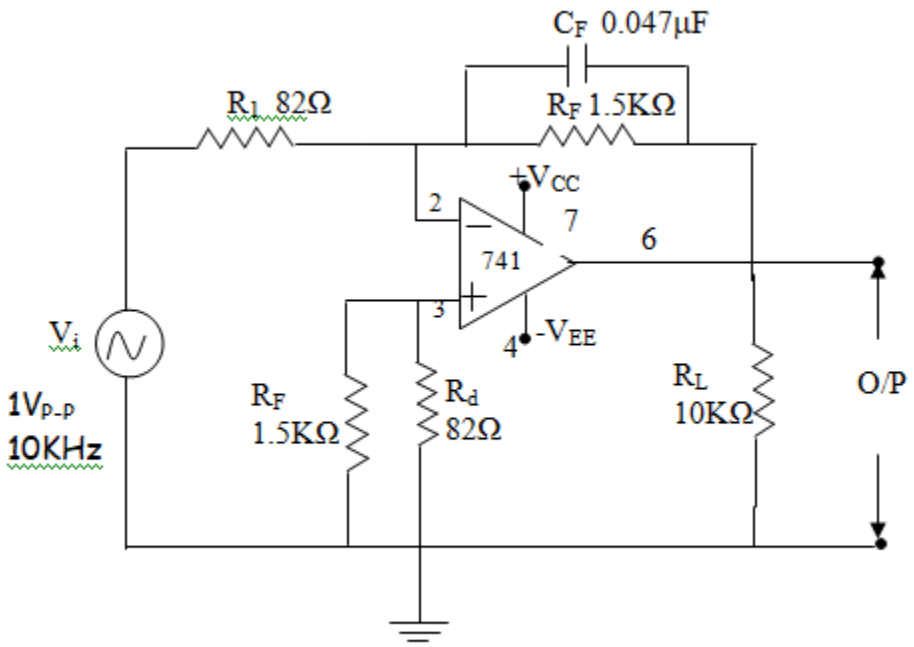


Figure 1.a.

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Differentiator:

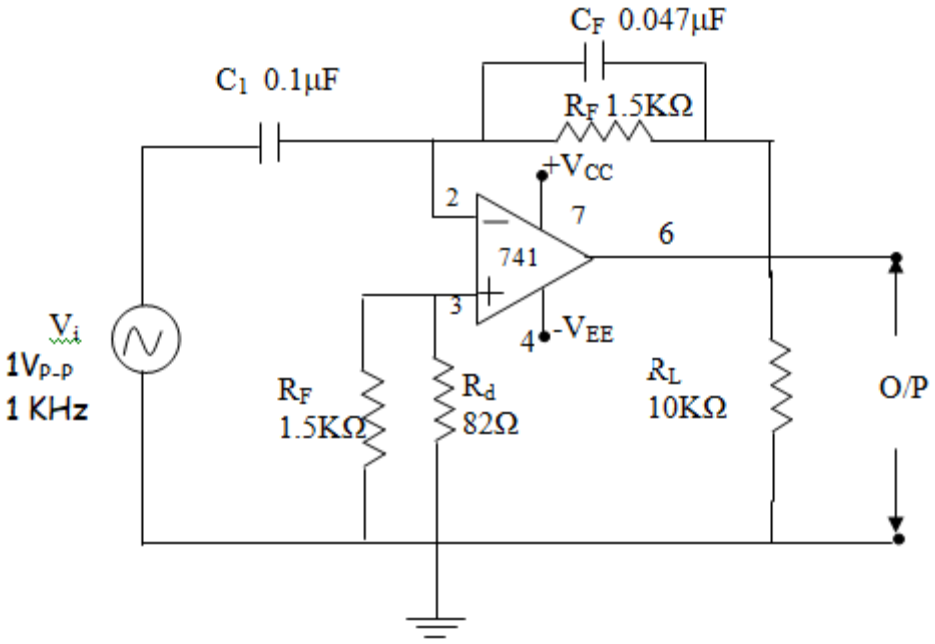

Figure 2.a

THE INTEGRATOR

A circuit in which the output voltage waveform is the integration of the input is called integrator.

$$V_0 = -\frac{1}{R_1 C_f}\int V_{in}\, dt \quad \text{----------(1)}$$

1. When we apply a sine wave the frequency response is as shown in Fig (1.a). The equation (1) indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R_1C_F . For Example if the input is a sine wave output will be a cosine wave or if the input is a square wave, the output will be a triangular wave.
2. When V_{in}= 0 the integrator works as an open – loop amplifier. This is because of the capacitor C_F acts as an open circuit (X_{CF} = infinite) to the input offset voltage V_{in}. In other words, the input offset voltage V_{in} and the part of the input current charging capacitor C_F produce the error voltage at the output of the integrator. To overcome this problem R_F is connected across the feedback capacitor C_F . Thus R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

3. Frequency response (f_b) of integrator at 0 dB is given by $f_b = 1/2\prod R_1C_F$.
4. Both the stability and the low – frequency roll-off problems can be corrected by the addition of a resistors R_F as shown in fig (2.a). The frequency response of practical integrator is as shown in fig (2.c). by a dashed line . In this 'f' is relative operating frequency and for 'f' and f_3 the gain R_F/R_1 is constant. However after f_a the gain decreases at a rate of 20dB/decade. In other words, between f_a and f_b the circuit acts as in integrator.

   The gain-Limiting frequency f_a is given by $f_a = \frac{1}{2\pi R_1 C_1}$.
5. The input signal will be integrated properly if the time period T of the input signal as larger than or equal to $R_F C_F$.

PROCEDURE:

1. Connect the integrator circuit as shown in fig 1.a.
2. Connect the function generator to the input terminals. Apply the input waveform1V sine wave at 10KHz.
3. Connect the C.R.O at the output terminals.
4. Switch ON the trainer and see that the supply LED glows.
5. Observe and note down the output waveforms. (Sample output waveforms are as shown in figures).
6. Fig (1.b) shows the frequency response of sine wave& Square wave inputs.
7. Apply the square wave, and repeat the above steps and observe & record the waveform (Ideal waveform are as shown in fig (1.b).

THE DIFFERENTIATOR:

The differentiator circuit performs the mathematical operation of differentiation. That is the output waveform is the derivative of the input waveform.

i.e., $V_{out} = R_F C_1 \frac{dV_{in}}{dt}$

1. If a sine wave is applied to the input of the differentiator then the output is cosine waveform.
2. The reactance of the circuit (R_F/XC_1) increase with increase in frequency at a rate of 20dB decade. This makes the circuit unstable

3. The input impedance XC_1 decreases with increase in frequency, which makes the circuit very susceptible to high frequency noise.
4. The frequency response of the basic differentiator is shown in figure 1.C. In this fig f_a is the frequency at which the gain is 0 dB.

$$f_a = \frac{1}{2\pi R_F C_1} \text{----------(2)}$$

5. Both the stability and the high – frequency noise problem can be corrected by the addition of two components R_1 and C_F as shown in fig 2.a. The frequency response of which is shown in fig 1.5.c by dashed line from f to $f_a$the gain decrease at 20dB/decade. This 40dB/decade change in gain is caused by the R_1 C_1 and R_F C_F combinations.The gain limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1 C_1} \text{----------(3)}$$

Where $R_1 C_1 = R_F C_F$.

$R_1 C_1$ and $R_F C_F$ help to reduce significantly the effect of high – frequency input, amplifier noise , and offsets. Above all, it makes the circuit more stable by preventing the increase in gain with frequency. General, the value of f_1, and in turn $R_1 C_1$ and $R_F C_F$ should be selected that $f_a = f_b = f_c$ unit gain – bandwidth.

6. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_F C_1$.

PROCEDURE:

1. Connect the differentiator as shown in fig 2.a
2. Connect the function generators to the input terminals, apply input waveform 1V sine wave at 1KHzat the input terminals
3. Connect the C.R.O at the output terminals.
4. Switch ON the trainer and see that the supply LED glows.
5. Observe and record the output frequency of waveforms (Ideal output waveforms are as shown in fig 2.b
6. Fig (2.b) shows the frequency response of sine wave& Square wave inputs.
7. Apply the square wave, and repeat the above steps and observe & record the waveform. The frequency response graph of basic differentiator circuit is also shown in the figure 2.b.

Integrator:

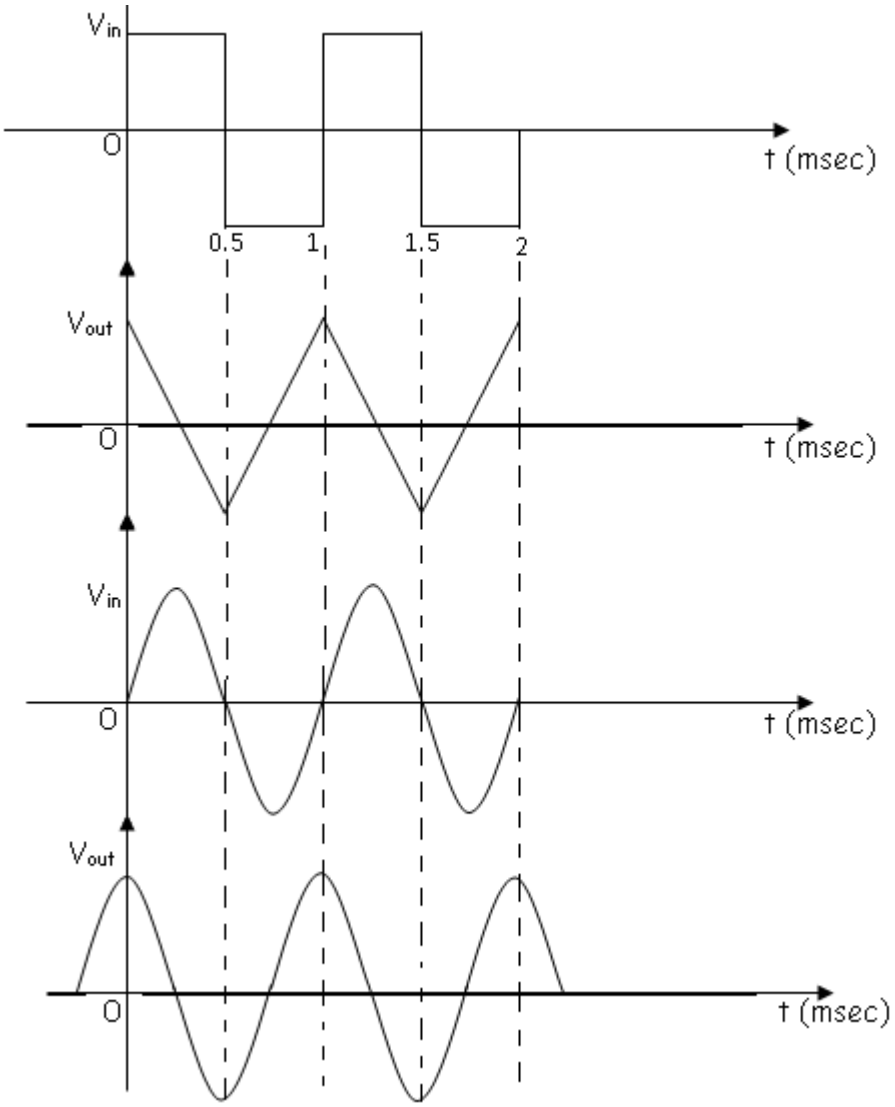

Figure 1.b

Differentiator:

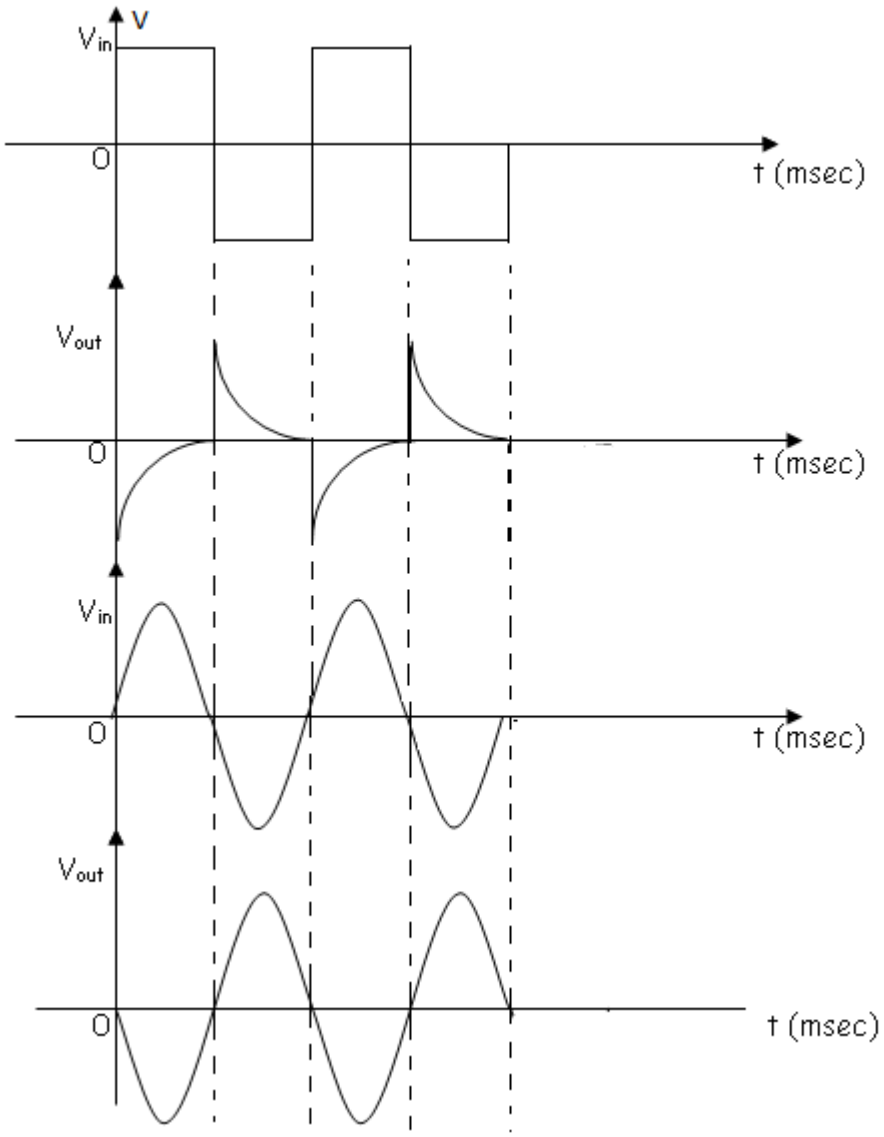

Figure 2.b

RESULT:

Reasoning Questions

1. Show that the output of a differentiator is differential of input.
2. Show that the output of a integrator is integral of input.
3. Mention the difference between practical integrator and ideal Integrator.
4. Sketch the Input and Output waveforms when we apply a 1KHzTriangle wave with peak to peak value of 5V to the Differentiator circuit.
5. Explain the frequency response of an integrator.
6. What type of output waveform is obtained when a triangular wave is applied to integrator circuit and also to Differentiator circuit.
7. A low frequency differentiator is desired for a particular application to perform the operation $V_o(t)=-0.001\ dvi(t)/dt$. Determine the suitable design of differentiator circuit for the periodic signal with a frequency of 1Khz..

INVERTING AMPLIFIER AND NON-INVERTING AMPLIFIER USING OP-AMP 741.

AIM: To find the voltage gain of Inverting and Non- Inverting Amplifier Using IC741 OP-AMP.

COMPONENTS REQUIRED:

Name	Qty
IC 741	1 No
Resistors 1 KΩ,10KΩ ,100KΩ	1 No

EQUIPMENT REQUIRED:

Equipment	Range	Quantity
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1
Bread board		1
Digital multimeter		1
Power supply	(0-30)V	1
Patch Cards		
Connecting Wires		

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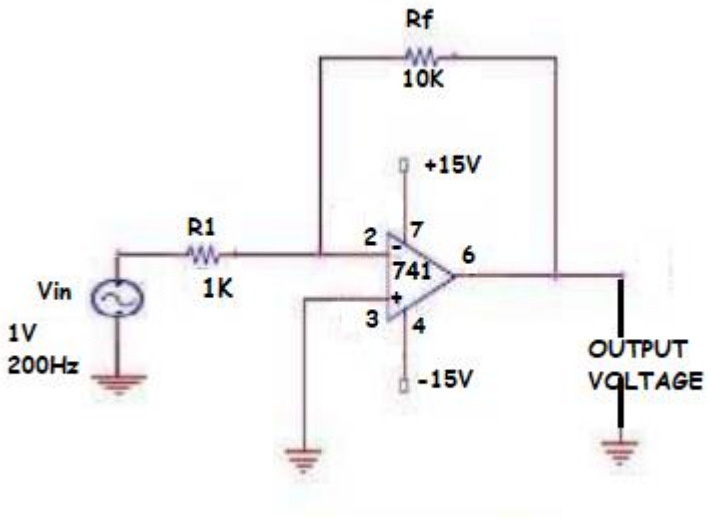
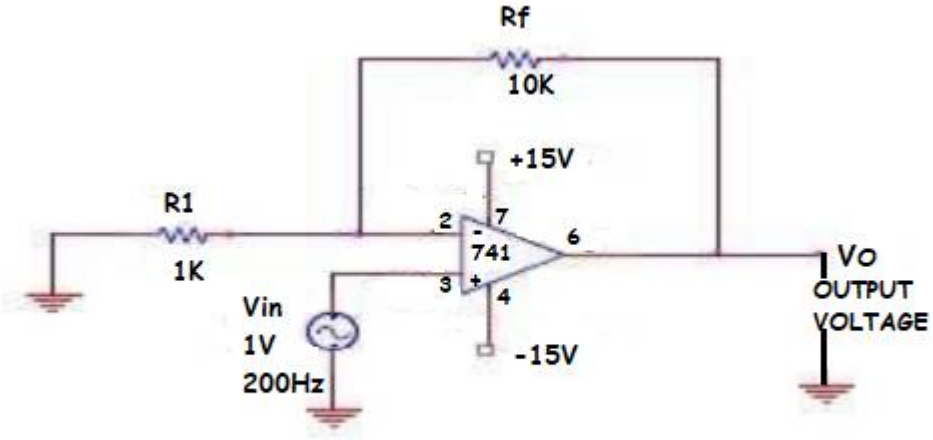
CIRCUIT DIAGRAM:

INVERTING AMPLIFIER:



NON-INVERTING AMPLIFIER:



THEORY:

When the input signal to an op-amp is supplied to the inverting input with non-inverting input at ground, the amplifier operates in the inverting mode that is the output differs in phase by 180 degrees with respect to the input. In an inverting amplifier the gain is given by the relation $A = - R_F / R_1$.

Where R_F and R_1 are the feedback and input resistor respectively. When operated in the non-inverting mode, the input signal is applied to the non-inverting input with the inverting terminal grounded through a resistor. The gain in this case is given by the relation $A = 1 + (R_f / R_1)$

PROCEDURE:

1. Connect the circuit as shown in fig (1)
2. Switch 'ON' the power supply.
3. Apply an input sine wave of 1V p-p, 200Hz from the in-built function generator in the kit to the reference input terminals.
4. Connect the C.R.O at the output terminals.
5. Observe and record the output voltage waveforms.
6. Calculate the Vo of the inverting Amplifier as

$$Vo = -\left(\frac{Rf}{R1}\right) \times Vin$$ and find its gain.

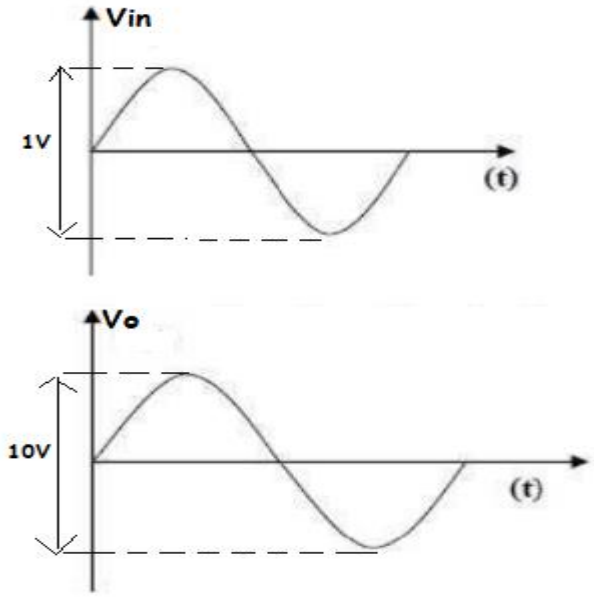
7. Connect the circuit as shown in fig (2).
8. Apply an input sine wave of 1V p-p, 200Hz from the in-built function generator in the kit to the reference input terminals.
9. Connect the CRO at output terminals.
10. Calculate the Vo of the Non-inverting amplifier as

$$Vo = \left(1+\frac{Rf}{R1}\right) \times Vin$$ and find its gain.

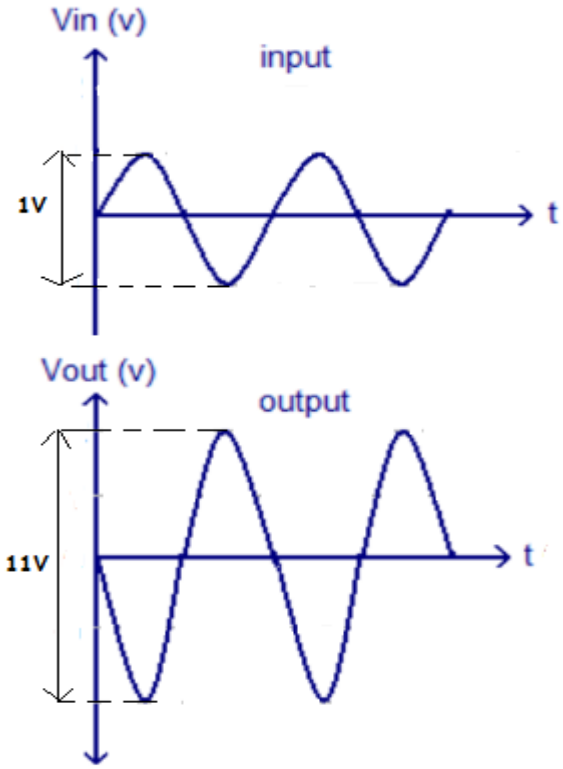
11. Verify the results with theoretical values.
12. Repeat the above steps for input voltages.

WAVEFORMS:

NON-INVERTING AMPLIFIER:



INVERTING AMPLIFIER:



RESULT:

Reasoning Questions

1. Mention the applications of Inverting and non-inverting amplifier.
2. List the ideal and practical values of IC 741 Op-amp
3. Draw the circuit of DC inverting amplifier.
4. Show that the output of inverting amplifier is $V_0 = -(Rf / R1)Vin$
5. What is the phase of the output signal when zero phase signal is applied to inverting and non-inverting amplifier?
6. What is the minimum gain of non-inverting amplifier?
7. Show that the gain of non-inverting amplifier is $A = 1 + (Rf / R1)$
8. Why the input terminals of Op-Amp 741 are called Inverting and Non-Inverting terminals.
9. Give the pin configuration of IC 741 Op-Amp.

DESIGN AN R-2R LADDER DIGITAL TO ANALOG CONVERTER

AIM: To obtain analog output voltages for the digital input data using 4-bit R-2Rtype D/A converter.

APPARATUS:1) 4 – bit D/A converter (R-2R) Trainer Kit.
2) Multimeter
3) Connecting wires

THEORY:

This consists of bridge rectifier followed by capacitor filter and three terminal regulators to provide regulated DC voltages in the circuit i.e, ±5V and 12V @ 150mA each.

D/A Converter:

A block diagram of the DAC 0808 is shown below. Note that in the block diagram are current switches, an R-2R ladder network, a bias circuit and a pair of the transistors that act as a current source. The heart of the DAC is the R-2R ladder.

For an explanation of the operation of an R-2R ladder, refer to figure 1.1, which shows a 4-bit R-2R ladder network for D/A conversion. The switches are connected either to ground (if the particular input bit is a 0) or to the op-amp input, a virtual ground,(if the particular input bit is a 1). For impedances purposes, the base of each 2R resistor is always connected to ground. Thus the impedance seen to the right of each voltage junction (at the top of the network) is R. from basic voltage division; the voltages at junctions to the right of the reference voltage -V are each one-half of the previous voltage. This is the same for the 8-bit DAC 0808 as for this 4-bit example circuit. For the example of figure 1.1, the digital input is 1001. This closes the switches on the MSB and the LSB and opens the other two switches.

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The same current floes at the reference for any switch position; however, the current to the output is a function of which switches are connected to the output and, hence a function of the digital input of the device. In figure 1.1, the total current at the reference voltage is always V/R, but the current to the output is the sum of only the two currents due to the two digital 1 inputs.

Therefore, the current from the output is V/2R + V/(16R) = (9/16) (V/R), which corresponds directly to the 1001 digital input. The op-amp with a feedback resistor $R_f$is a current-voltage converter. If R_f=R (from the resistor ladder) the analog output voltage is R (9/16) V/R = (9/16) V. If the desired output voltage range of the DAC is 5V and the reference voltage is 5V the output of the D/A converter would be (9/16) 5V = 2.81v, which corresponds to the digital value of 1001.

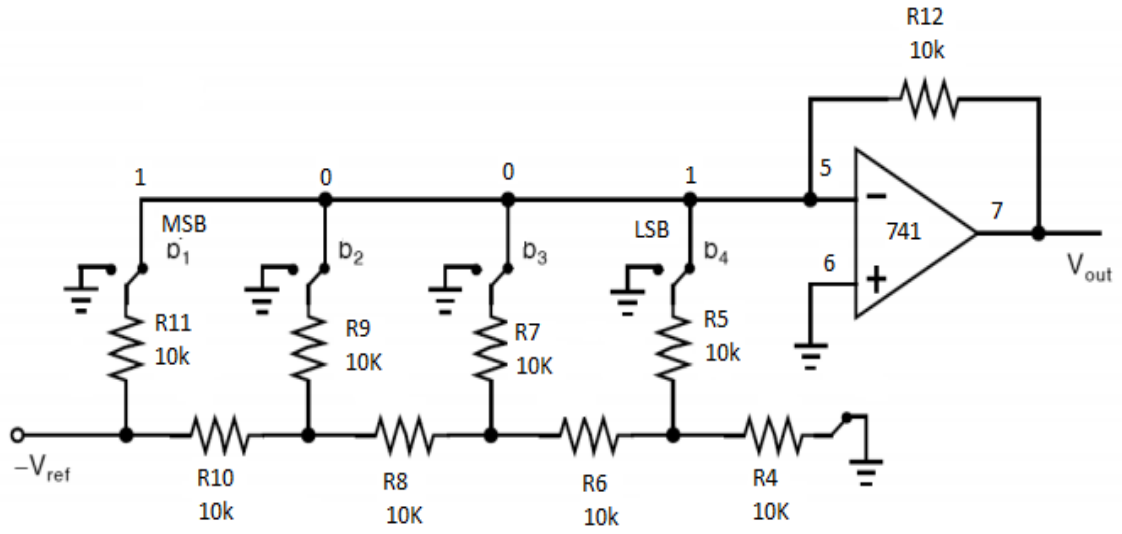

Figure: 1.1

The actual circuit used for D/A converter is shown in figure 1.2; it corresponds very closely to the theoretical circuit discussed. If the value of the 10K resistor attached to pin 14 and the 10K feedback resistor on the op-amp are exactly the same, the D/A conversion will be quite precise.

CIRCUIT DIAGRAM:

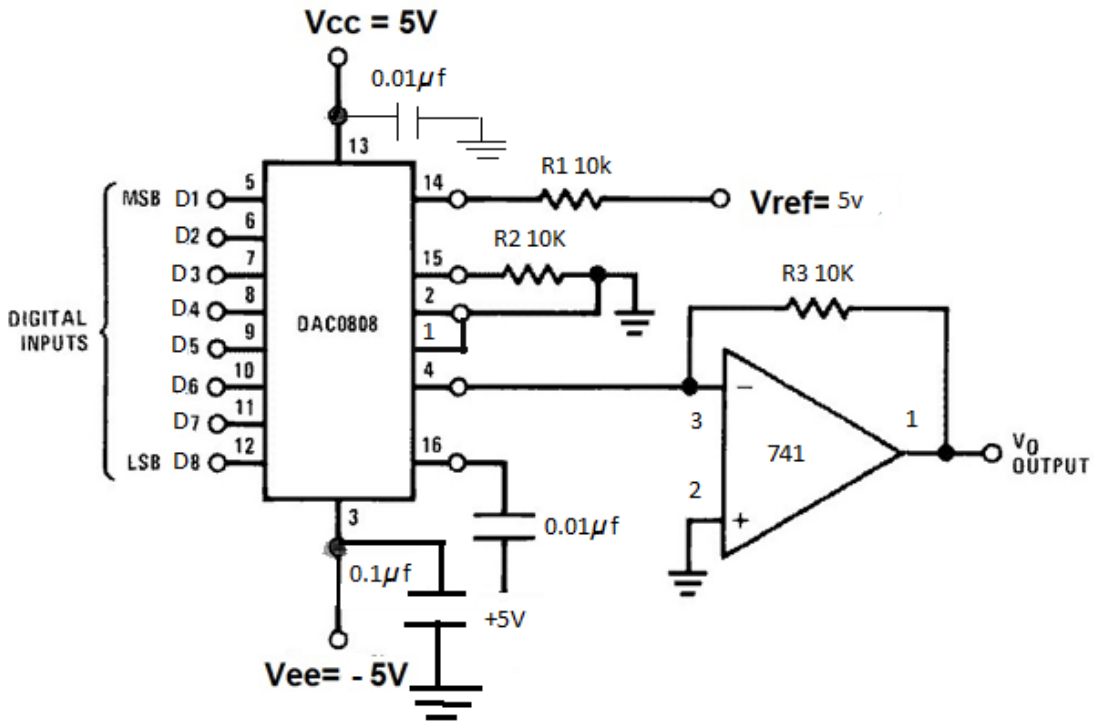

Figure: 1.2

PROCEDURE:

1. Switch on the trainer and study the theory of operation thoroughly.
2. Observe the output voltage for different combinations of digital inputs and compare it with the theoretical value.

Theoretically Vo is given by:

$$V_0 = R_f \left(\frac{D7}{2R}+\frac{D6}{4R}+\frac{D5}{8R}+\frac{D4}{16R}+\frac{D3}{32R}+\frac{D2}{64R}+\frac{D1}{128R}+\frac{D0}{256R}\right)$$

For Example:

Digital input = 10010001

Rf=10K

R=10k

Analog input $=V_0 = 10/10 \left(\frac{5}{2}+\frac{0}{4}+\frac{0}{8}+\frac{5}{16}+\frac{0}{32}+\frac{0}{64}+\frac{0}{128}+\frac{0}{256}\right) = 2.832V$

OBSERVATION TABLE:

Digital I/P data $D_7D_6D_5D_4D_3D_2D_1D_0$	Analog output	
	Theoretical voltage V_0	Practical voltage V_0

RESULT:

Reasoning Questions

1. Derive the expression for the output voltage V_0 of R-2R type D/A converter.
2. What are the advantages of R-2R type D/A converter?
3. Compare R-2R Type with weighted resistor type D/A converter.
4. Mention the applications of D/A converters.
5. Define the terms full-scale voltage and one least-significant bit for D/A converter.
6. Consider the 4-bit D/A converter with V_r=10V,R_f=10KΩ. Determine
   a)Number of possible output levels
   b)Full scale voltage
   c)Value of 1 LSB
7. Determine the output voltage for the following input digital words When 4-bit D/A converter with V_r=10V,R_f=10KΩ is considered
   i) 0001 ii) 0110 iii) 1010
8. What is the difference between Inverted R-2R and Non-Inverted R-2R type D/A converter.

D/A CONVERTER USING BINARY WEIGHTED RESISTORS

AIM:- Digital to analog conversion using Binary weighted resistor method.

APPARATUS:- 1.D/A Converter Trainer kit
2. DMM (digital multi-meter)
3. Required patch chords

CIRCUIT DIAGRAM:

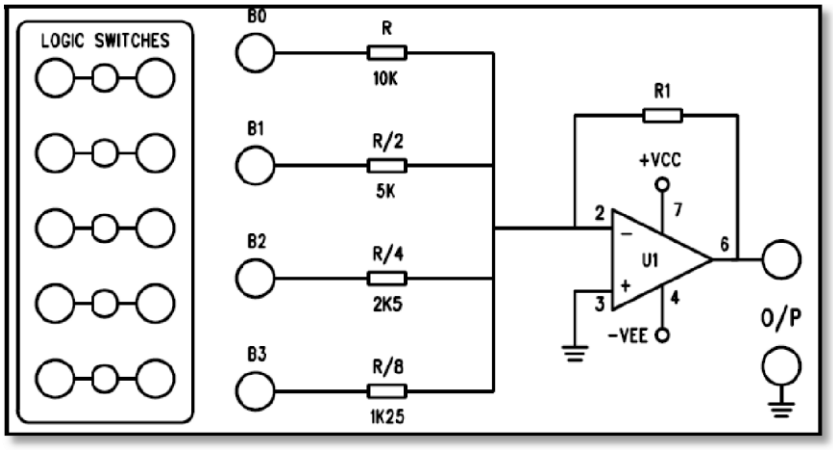

Figure (1) D/A converter using binary weighted resistors

THEORY:-

D/A Converter using an Op-amp and binary weighted resistors. Although in the below figure the op-amp is connected in the inverting mode, it can also connected in the non- inverting mode. Since the number of binary inputs is four. The Converter is called a 4bit (Binary digit) Converter. Because there are 16 (2^4) combination of binary inputs for b0 through b3, an analog output should have 16 possible corresponding values. In Figure four switches (b0 to b3) are used to simulate the binary inputs; in practice, a4-bit binary counter such as the 7493 may be used instead. When Switch b0 is closed (Connected to +5V), the voltage across R is 5V because $V_2=V_1=$ OV. Therefore, the current through R is 5V/10 KΩ=0.5mA.

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However, the input bias current I_B is negligible; hence the current through feedback Resistor Rf Is also 0-5mA, Which in turn Produces an output voltage of – (1KΩ) (0.5mA) =- 0.5V. Note that the op-amp is working as a current-to-voltage converter. Now suppose that switch b1 is closed and b0 is open. This action connects R/2 to the positive supply of +5V, causing twice as much current (1mA) to flow thorough Rf, Which in the turn doubles the output voltage. Thus the output voltage V_0 is -1V when switch b1 is closed. Similarly, if both switches b0 and b1 are closed, the current through Rf will be 1.5mA, which will be converted to an output voltage of – (1KΩ) (1.5mA) =-1.5V.

Thus, depending on whether switches b0 to b3 are open or closed, the binary – Weighted currents will be set up in input resistors. The sum of these currents is equal to the current through Rf, which in turn is converted to a proportional output voltage. When all the switches are closed, obviously the output will be maximum. The output voltage equation id given by

$$V_o = -Rf \times Vcc \times \frac{Bo}{R} + \frac{B1}{R/2} + \frac{B2}{R/4} + \frac{B3}{R/8}$$

Where each the inputs b3, b2, b1 and b0 may either be high (+5V) or low (0V), the figure2 shows analog outputs versus possible combinations of inputs. The output is a negative going staircase with 15 steps of -0.5 each. In practice, however, the steps may be not all be the same is because of the variations in the logic high voltage levels.

PROCEDURE: -

1) Connect the patch chords from Logic Switches to B0, B1, B2, and B3.
2) Connect the DMM (digital multi-meter) at the output side with respective polarity.
3) Connect the Power card to the main supply.
4) Switch on the trainer and apply the binary inputs as given in the table.
5) Note down the values of the DMM (digital multi-meter).

CALCULATIONS:-

Example:-

Assume B0=1, B1=0, B2=0, B3=0 and Vcc=5V, Rf=1KΩ

Substitute the above values in the formula

$$Vo = -Rf \times Vcc \times \left(\frac{B0}{R} + \frac{B1}{R/2} + \frac{B2}{R/4} + \frac{B3}{R/8}\right)$$

$$Vo = -1k\Omega \times 5 \times \left(\frac{1}{10k\Omega} + \frac{0}{5k\Omega} + \frac{0}{2.5k\Omega} + \frac{0}{1.25k\Omega}\right)$$

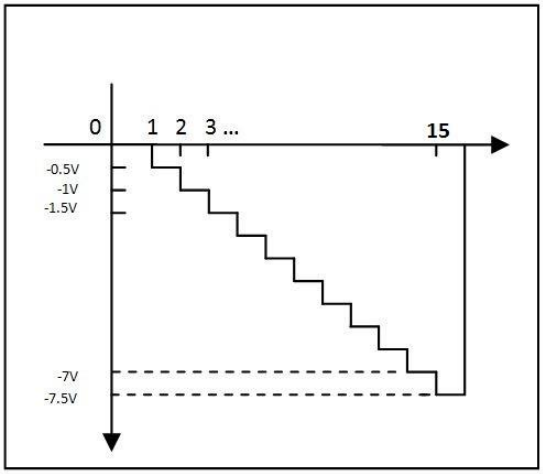
$$Vo = 1K\Omega \times 5 \times (1/10\ K\Omega)$$

$$Vo = -0.5V$$

OBSERVATION TABLE:-

Inputs				Theoretical	Practical
B3	B2	B1	B0		

EXPECTED GRAPH:-



RESULT:

Reasoning questions

1. How many resistors are required in 12 bit-weighted resistors DAC?
2. Mention different techniques for D/A conversion.
3. What is the main disadvantage of weighted resistor DAC over others?
4. Derive V_0 of 4-bit D/A converter.
5. Define the terms full-scale voltage and one least-significant bit for a D/A converter.

MONOSTABLE MULTIVIBRATOR USING 555 TIMER

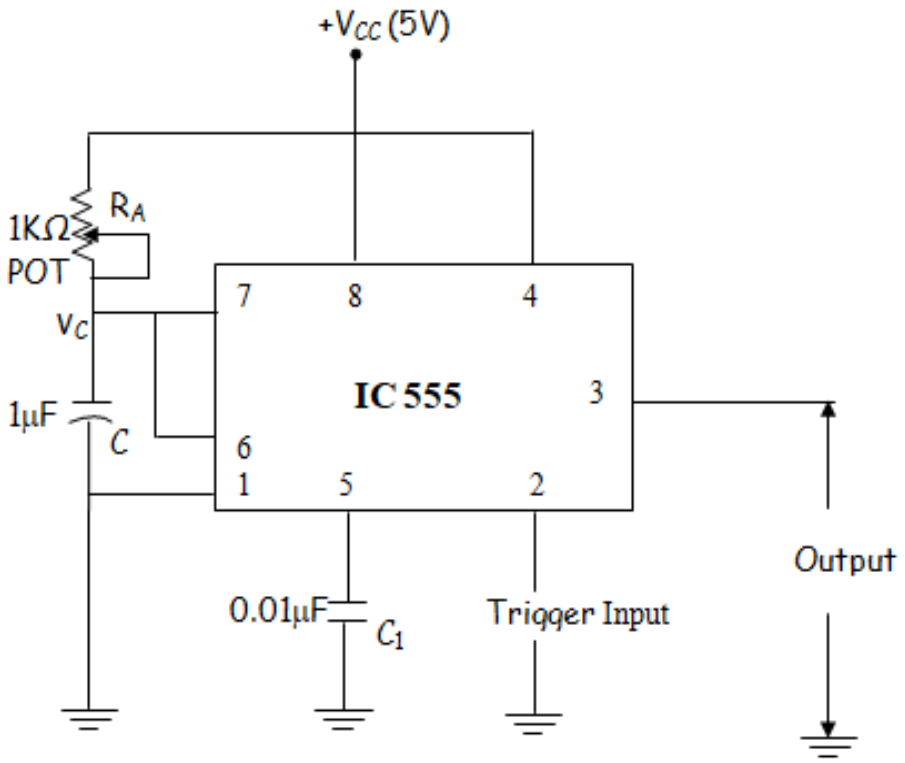
AIM:

1. To study and design 555 timer as a Monostable multivibrator.
2. Calculate the frequency of oscillations & time period of output waveform.

EQUIPMENT REQUIRED:

1. 555 Timer Trainer Kit.
2. 20MHz C.R.O
3. 1MHz Function generator
4. Multimeter
5. Connecting patch chords.

CIRCUIT DIAGRAM:



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INTRODUCTION:

The 555 Timer is used in number of applications; it can be used as monostable, astable multivibrators, DC to DC converters, digital logic probes, analogy frequency voltage regulators and time delay circuits.

The IC 555 timer is 8-pin IC and it can operate in free- running (Astable MV) mode or in one-shot (Monostable MV) mode. Pin configuration is as shown fig (1). It can produce accurate and highly stable time delays or oscillations.

THEORY:

Monostable can also called as One-shot Multivibarator fig (1) shows the Monostable Multivibrator. When the output is low, the circuit is in stable state, Transistor Q1 is ON and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin-2, transistor Q1 is turned OFF, which releases short circuit across the external capacitor and drives the output High. The capacitor C now starts charging up toward Vcc through R_A. However, when the voltage across the external capacitor equals 2/3 Vcc comparator-1's (C_1) output switches from low to high, which is turn drives the output to its low state via the output of the flip flop turns transistor Q1 ON, and hence, capacitor C rapidly discharges through the transistor. The output of the Monostable remains low until a trigger pulse is again applied. Then the cycle repeats.

The Fig (2) shows the trigger input and output voltages, and capacitor voltage waveforms. Pulse width of the trigger input must be smaller than the expected pulse width of the output waveforms. Trigger pulse must be a negative- going input signal with amplitude larger than 1/3 Vcc.

The time during which the output remains high is given by

$$t_p = 1.1 R_A C$$

Once triggered, the circuit's output will remain in the high state until the set time t_p elapses. The output will not change its state even if an input trigger is applied again during this time interval t_p.

PROCEDURE:

1. Connect the 555 timer as monostable mode as shown in fig (1).
2. Connect the C.R.O at the output terminals.
3. Apply external trigger at the trigger input terminal and give supply to trainer.
4. Record and observe the waveforms at the output terminals and also across the capacitor.
5. Verify with the sample output waveforms as shown in fig (2)
6. Calculate the pulse width, time period of pulse (Tp) theoretically and verify with practical values.
7. Now change R_A value and observe out pulse width Tp and verify it theoretically.

$$Tp = 1.1\ R_A\ C_A$$

WAVEFORMS:

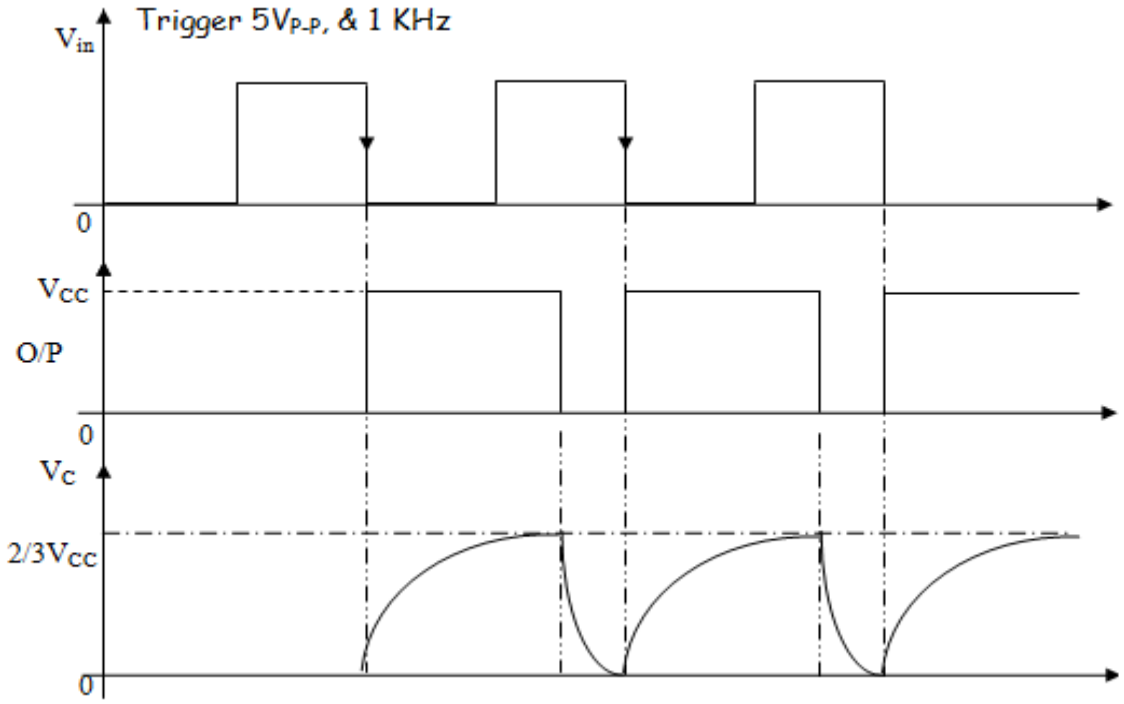

FIG -2

RESULT:

Reasoning Questions

1. List the important features of the 555 Timer.
2. Define Duty cycle.
3. What are the modes of operation of Timer and explain the differences between two operating modes of the 555 Timer.
4. The Monostable multivibrator circuit is to be used as a divided by 2 network. The frequency of the input trigger signal is 2 KHz. If the value of C=0.01 μF, What should be the value of R_A (Let t_p =1.2T)
5. Consider the Monostable multivibrator with R=3KΩ and C=0.0068μF. Determine the pulse width.
6. Design a Monostable multivibrator to produce an output pulse 2msec wide.
7. What is the function of control input (pin5) of 555 timer?
8. List the applications of 555 timer in monostable mode
9. Why do we use negative trigger for monostable operation?
10. Explain the trigger circuit used for monostable multivibrator?

ASTABLE MULTIVIBRATOR USING 555 TIMER

AIM:

1. To study and design 555 timer as a Astable multivibrator.
2. Calculate the frequency of oscillations & time period of output waveform.

EQUIPMENT REQUIRED:

1. 555 Timer Trainer Kit.
2. 20MHz C.R.O
3. Multimeter
4. Connecting patch chords.

CIRCUIT DIAGRAM:

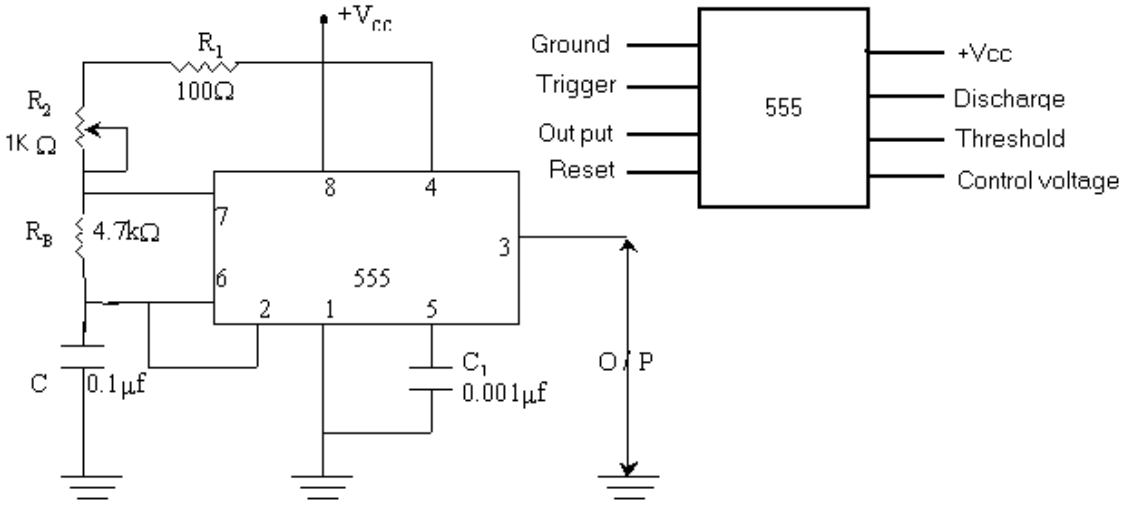

Fig. 1

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INTRODUCTION:

The 555 Timer is used in number of applications; it can be used as monostable, astable multivibrators, DC to DC converters, digital logic probes, analogy frequency voltage regulators and time delay circuits.

The IC 555 timer is 8-pin IC and it can operate in free- running (Astable MV) mode or in one-shot (Monostable MV) mode. Pin configuration is as shown fig (1). It can produce accurate and highly stable time delays or oscillations.

THEORY: Astable Multivibrator often called a free-running Multivibrator. External Trigger input is not required to operate the 555 as an Astable Configuration. However, the time during which the output is either high or low is determined by two external components Resistor & Capacitor.

Fig (1) shows the 555 as Astable Multivibrator. Initially, when the output is high, capacitor C starts charging towards Vcc through resistor R_a and R_b. As soon as voltage across the capacitor equals to 2/3 Vcc, comparator-1 triggers the flip-flop, and the output is low. Now capacitor discharges through R_b and transistor Q_1. When the voltage across capacitor c equals to 1/3Vcc, comparator-2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage waveforms are as shown in fig (2).

In this way capacitor periodically charges 7 discharges between 2/3Vcc and 1/3Vcc respectively.

The time during which the capacitor charges from 1/3Vcc to 2/3 Vcc is equal to the time, the output is high and is given by

$$t_c = 0.69(R_a + R_b)\, c$$

The time during which the capacitor discharges from 2/3 Vcc to 1/3Vcc is equal to the time, the output is low and is given by

$$t_d = 0.69(R_b)\, c$$

The Total Time period of the pulse is the sum of charge time and discharge time, time period is given by

$$T = t_c + t_d$$

$= 0.69(Ra + 2Rb)\ c$

This, in turn gives the frequency of oscillation as given below

$F = 1/T = 1.45/(Ra + 2Rb)\ c$

DUTY CYCLE: This term is in conjunction with Astable Multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage.

$\%\text{Duty cycle} = t_c/T * 100$

$= (Ra + Rb/Ra + 2Rb)*100$

PROCEDURE:

1. Connect the 555 timer as Astable mode as shown in fig (1).
2. Connect the C.R.O at the output terminals.
3. Give supply to trainer kit.
4. Record and observe the waveforms at the output terminals and also across the capacitor.
5. Verify with the sample output waveforms as shown in fig (2)
6. Calculate the Tc, Td, time period of pulse (Tp) and duty cycle percentage theoretically and verify with practical values.
7. Find the charging time t_c discharging time t_d and totals time period T from the output waveform.
8. Verify these values with theoretical values and calculate the % of the duty cycle.

Where $T_c = 0.69\ (R_B + R_A)C$

$R_A = R_2 + R_1$

$T_d = 0.69\ R_B C$

$T = Tc + T_d$

$\%\text{ of DC} = \frac{T_d}{T} * 100$

WAVEFORMS:

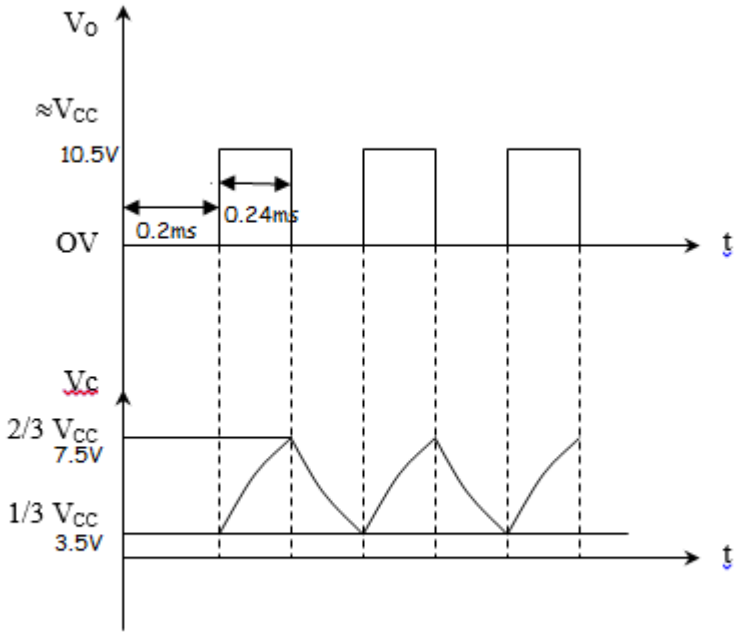

Fig. 2

RESULT:

Reasoning Questions

1. List the important features of the IC555 Timer.

2. Define Duty cycle.

3. What are the modes of operation of Timer and explain the difference between two operating modes of the 555 Timer.

4. Consider the Astable multivibrator with R_A=10KΩ,R_B=200KΩ and C=0.1μF. Determine
   a) High state interval b) Low state interval
   c) Period d) Frequency e) Duty cycle.

5. Design an Astable 555 timer circuit to produce a 2 KHz square wave With a duty cycle of 70%, Select C=0.1μF.

6. What is the function of control input (pin5) of 555 timer?

7. Compare the time period 'T' of the Astable multivibrator using IC 555 timer and op-amp IC741.

8. List the applications of 555 timer in astable mode.

9. Derive the time period T of the Astable multivibrator.

10. Why do we connect pin 4 of IC 555 timer to supply pin when it is not used.