

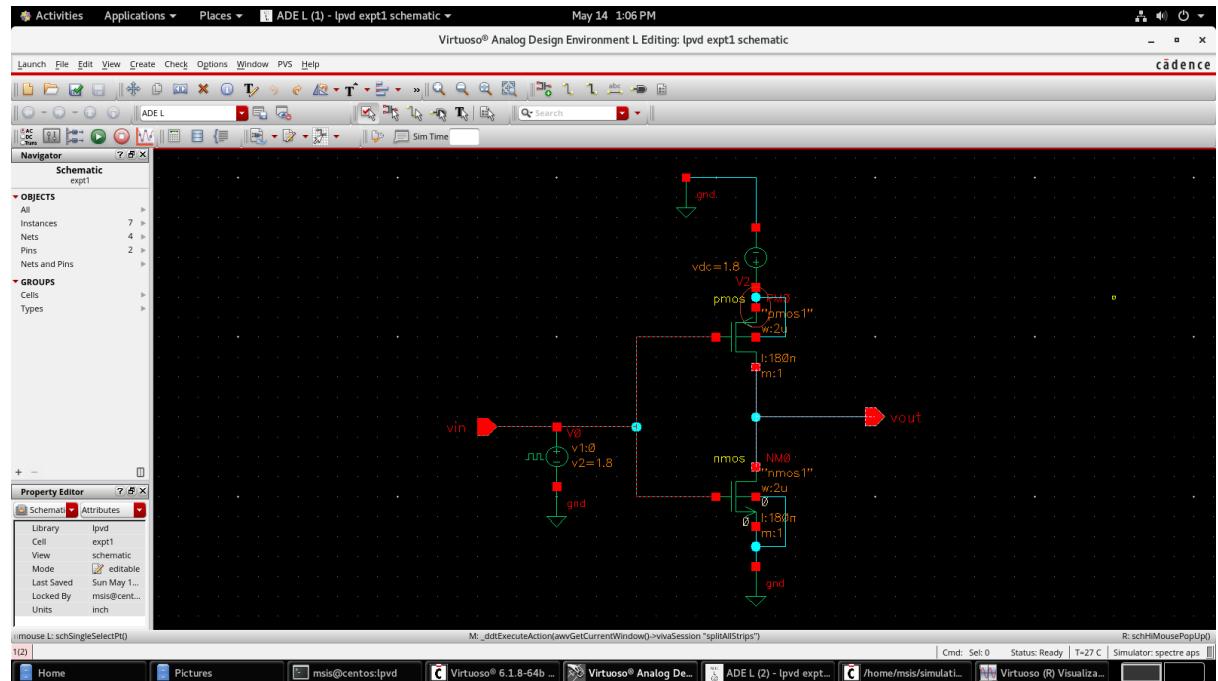
# LPVD Lab Assignment

Megha Shenoy - 221038021

## Experiment1:

Plot I<sub>sc</sub> for inverters by choosing suitable C, L and W/L ratio's for the MOS transistors.

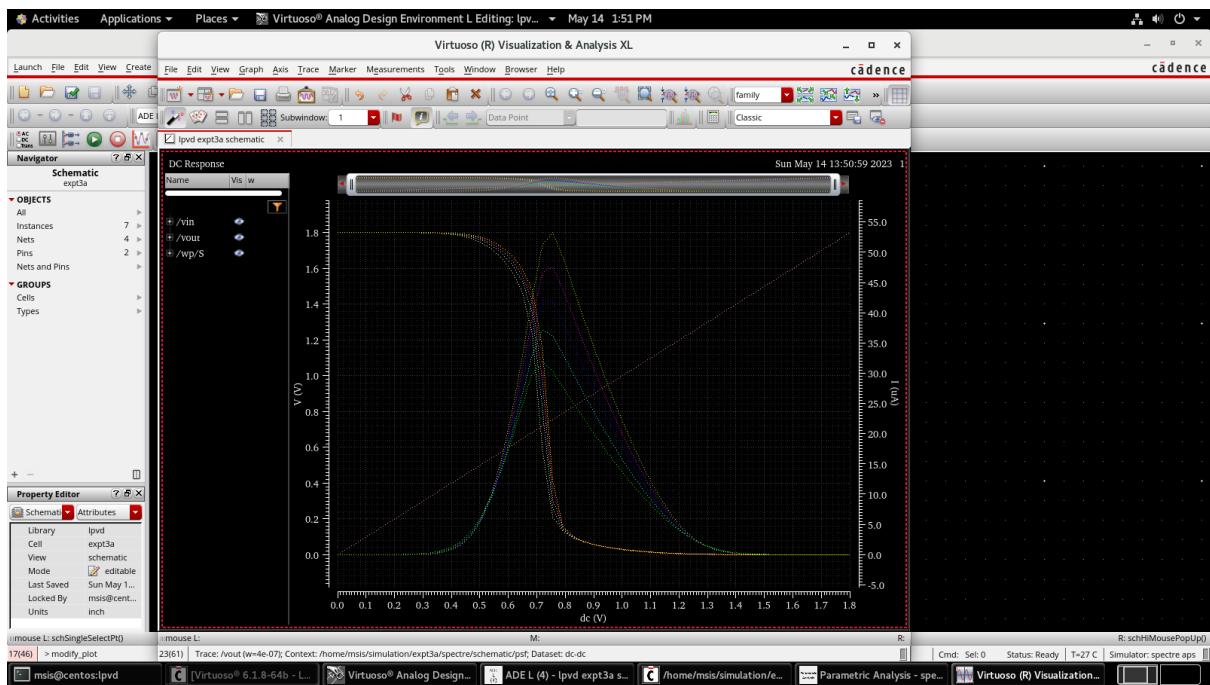
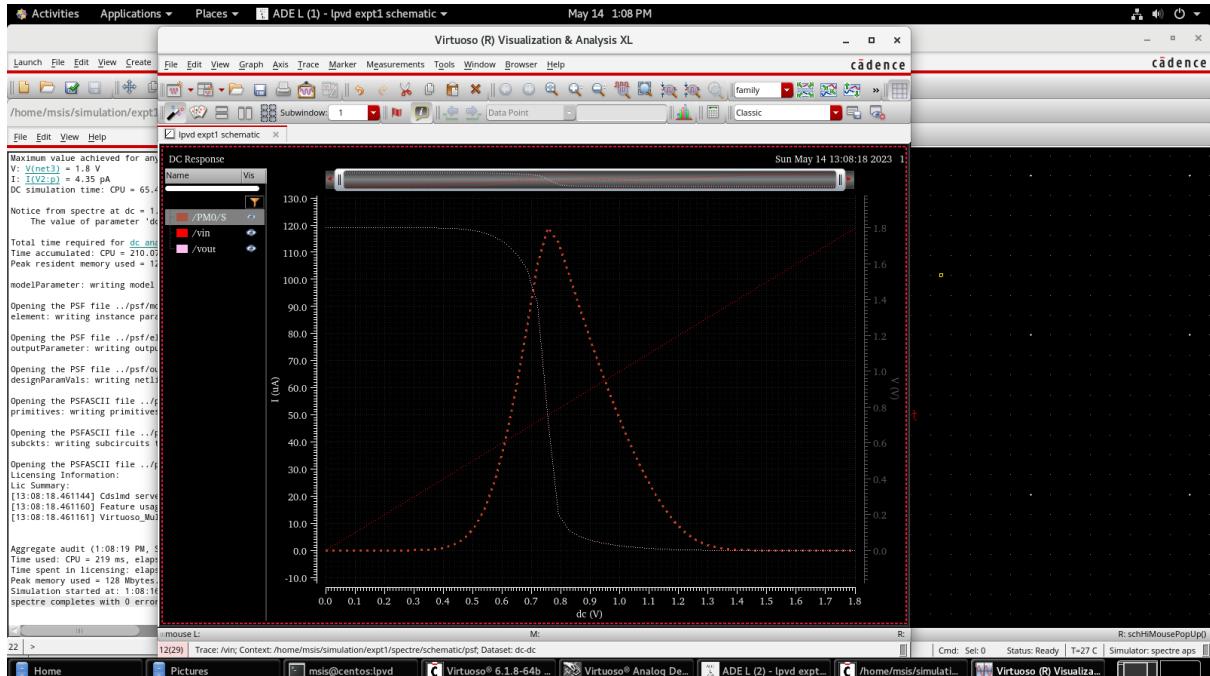
### Schematic



### Transient Analysis



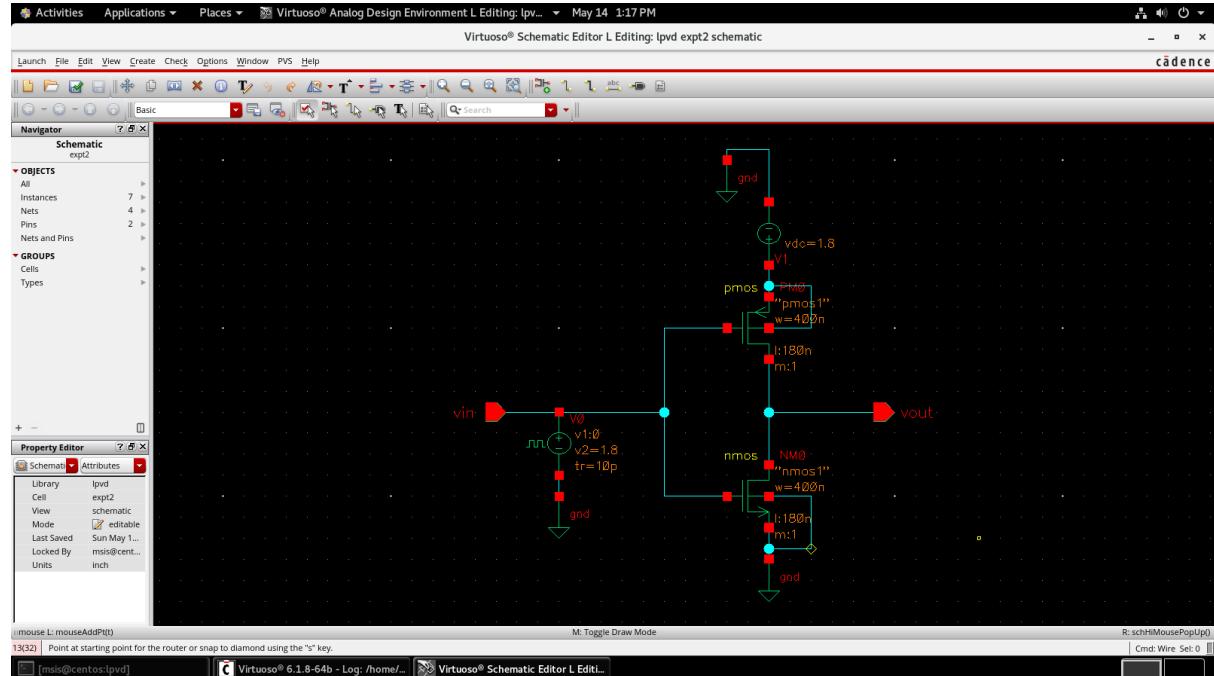
## DC Analysis



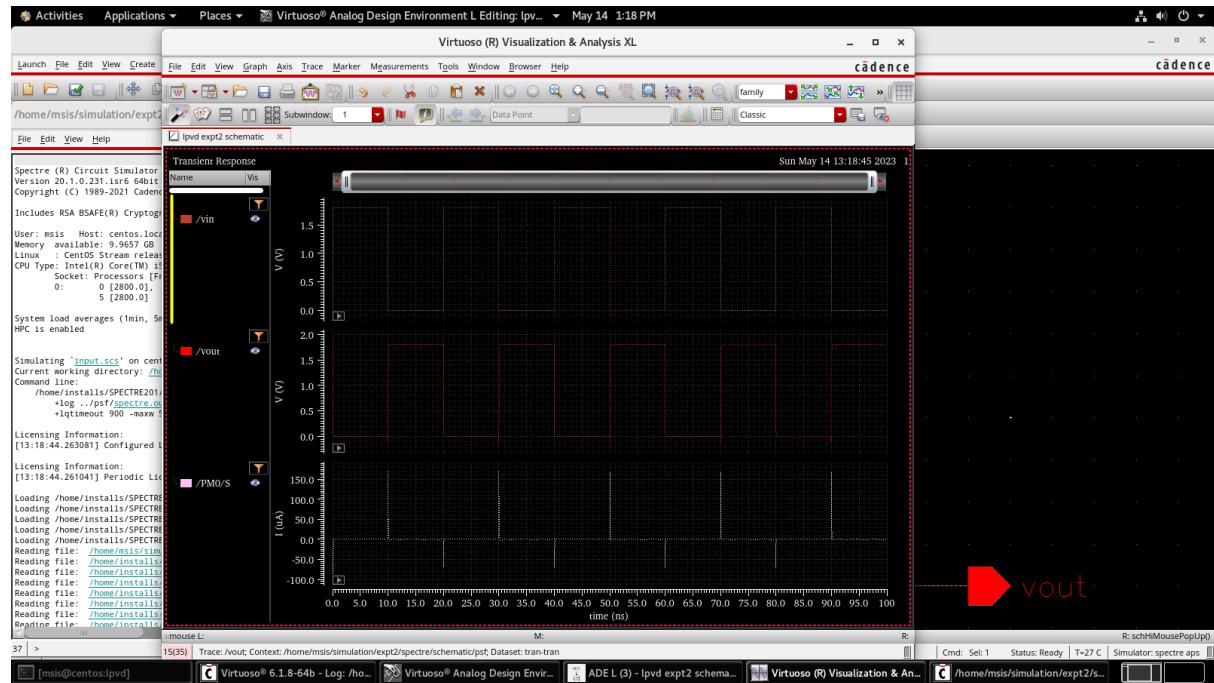
## Experiment2:

Plot leakage currents of minimum sized NMOS and PMOS transistors in 180nm.

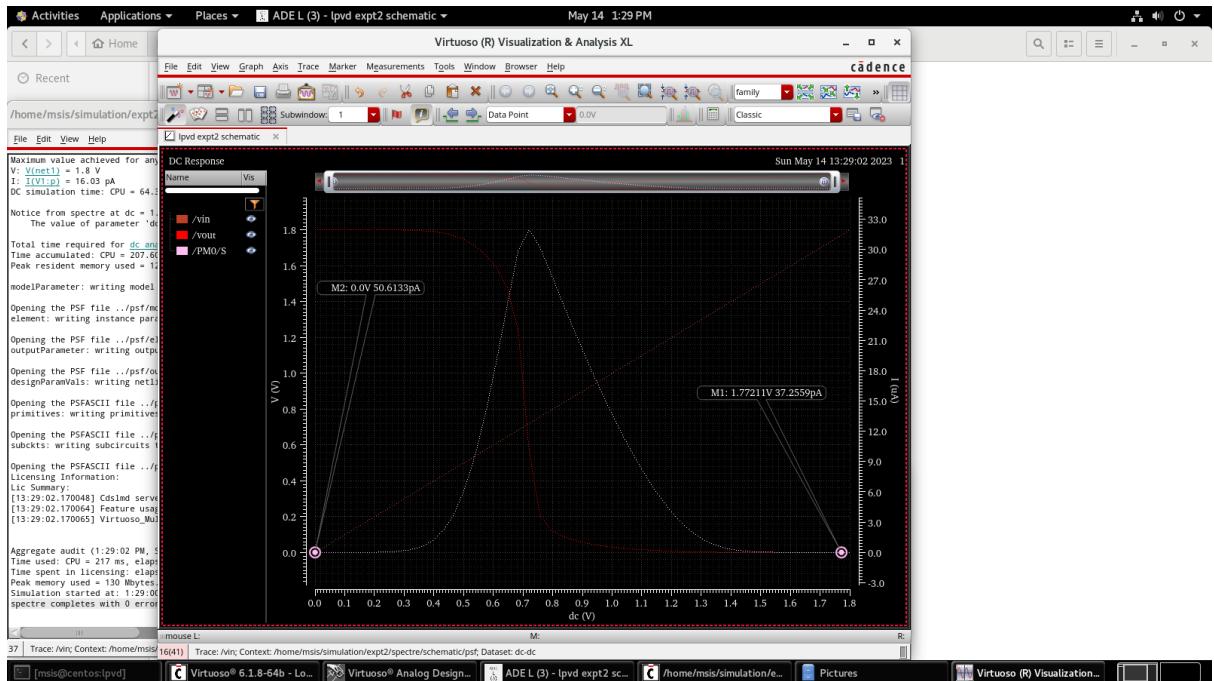
### Schematic



### Transient Analysis



## DC Analysis

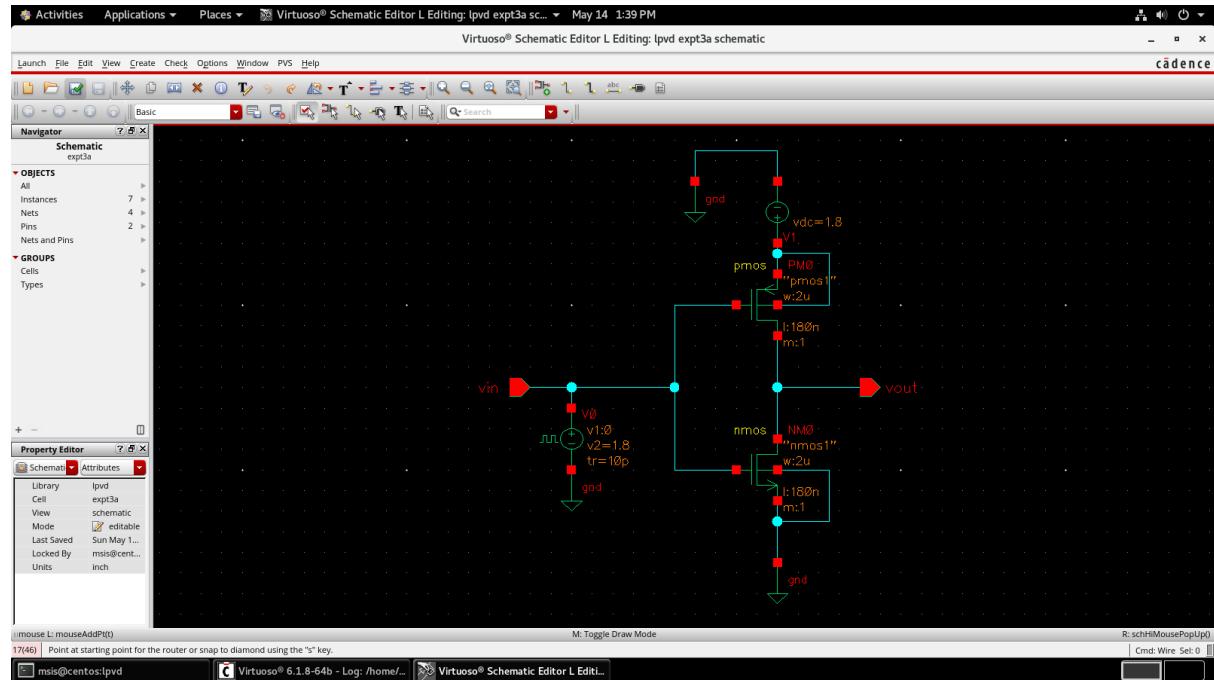


### Experiment3:

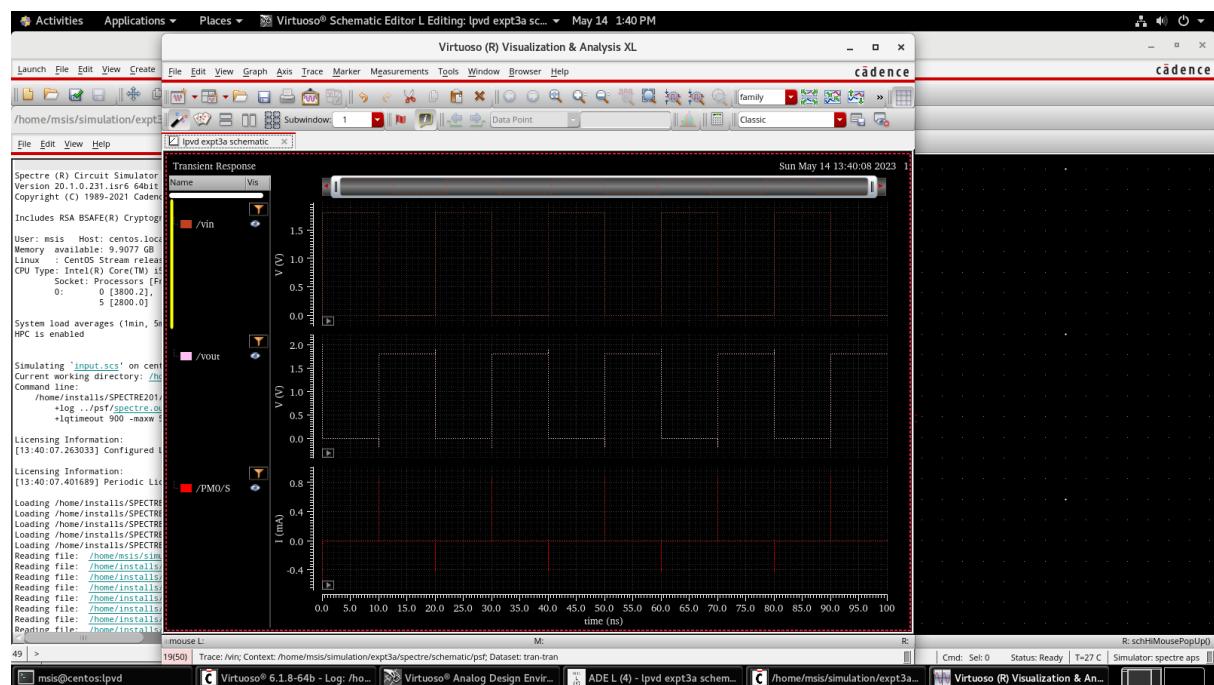
Natural stacking –check function and leakage current (I<sub>sub</sub>) of

#### a)Inverter

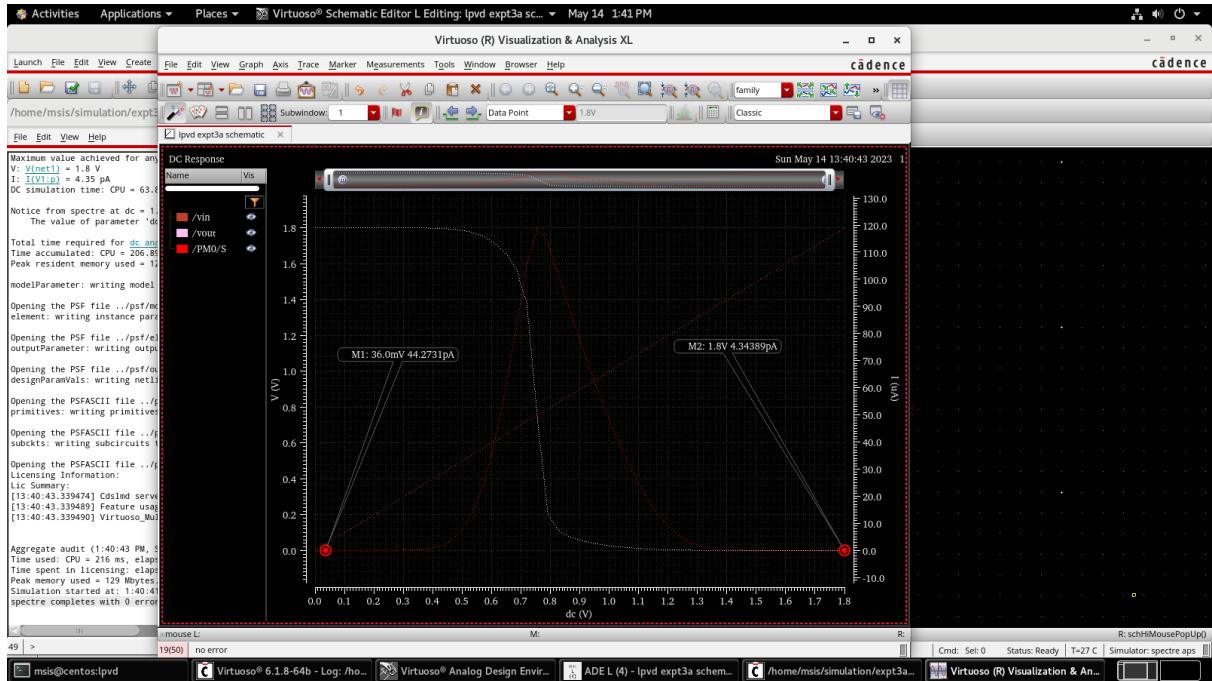
##### Schematic



#### Transient Analysis

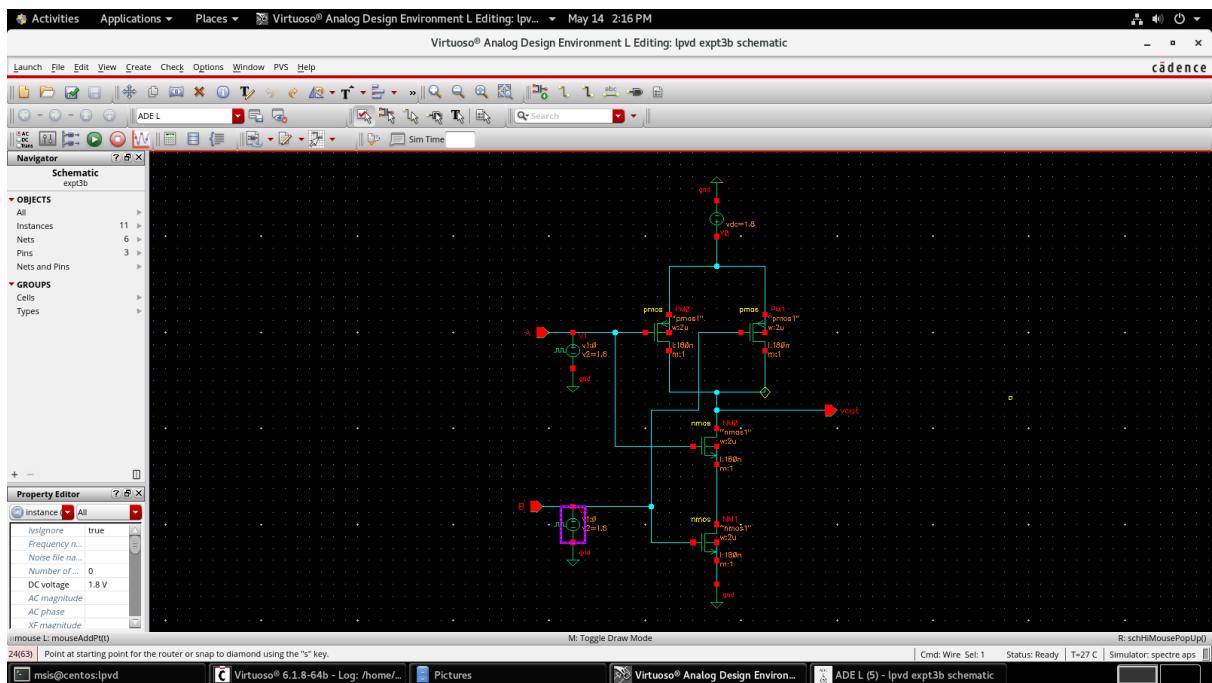


## DC Analysis

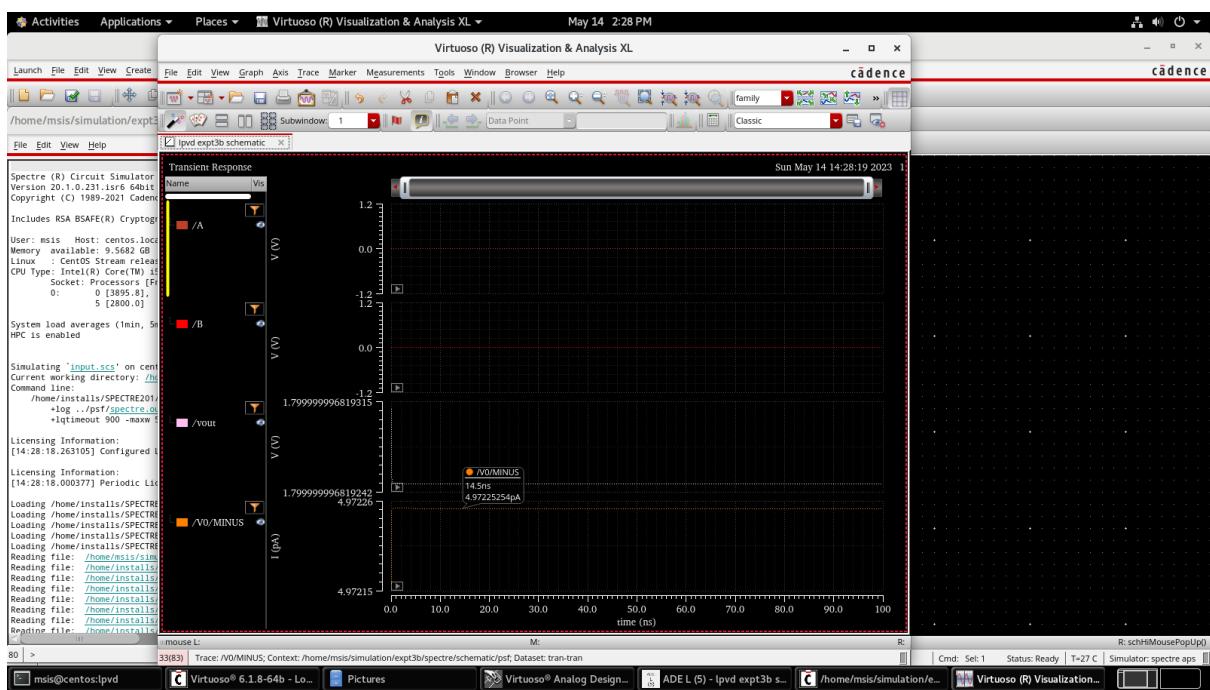


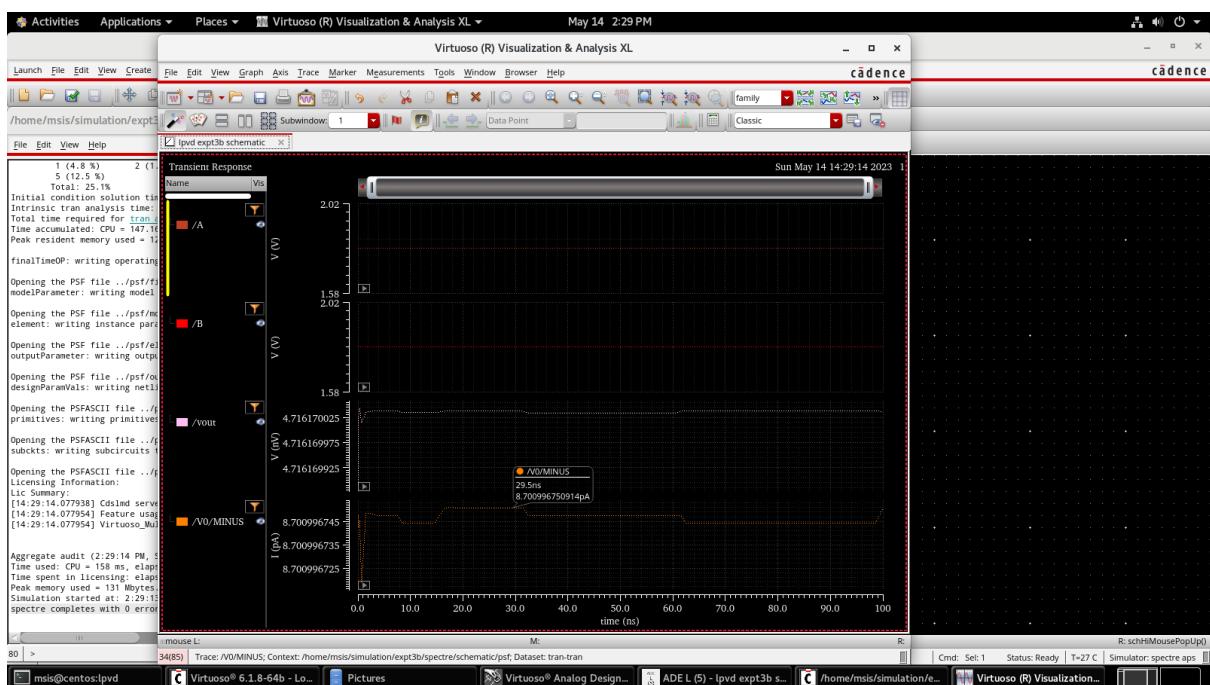
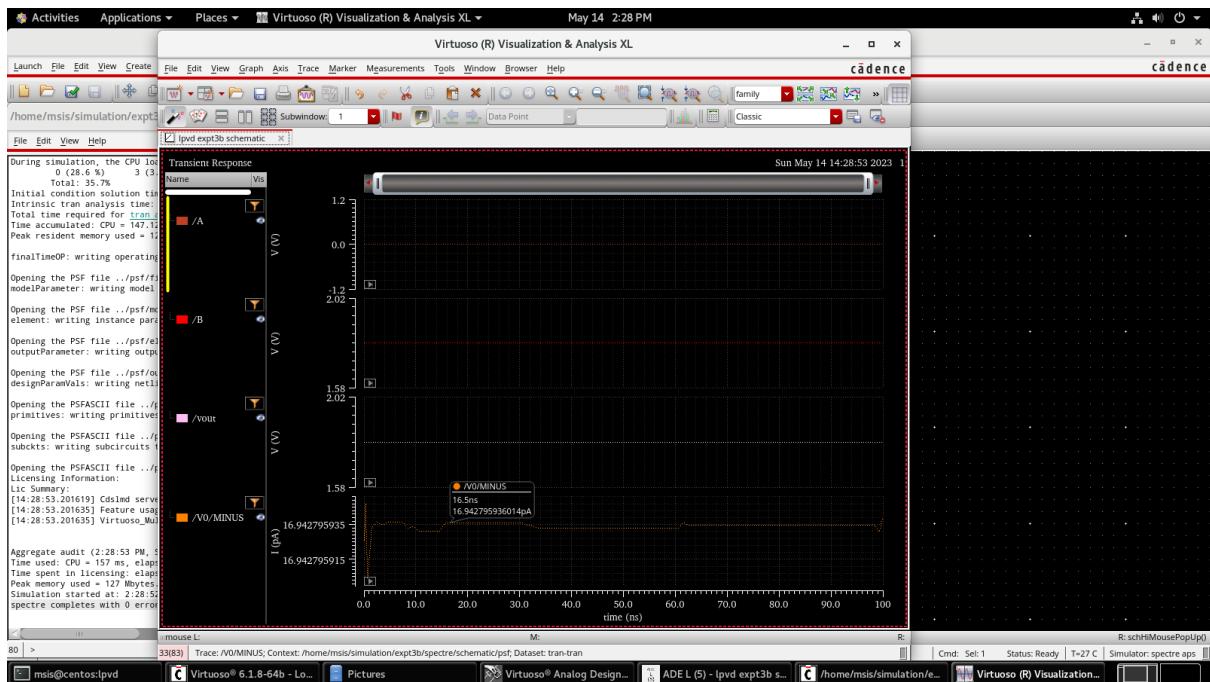
b)2 input NAND gate for various input combinations.

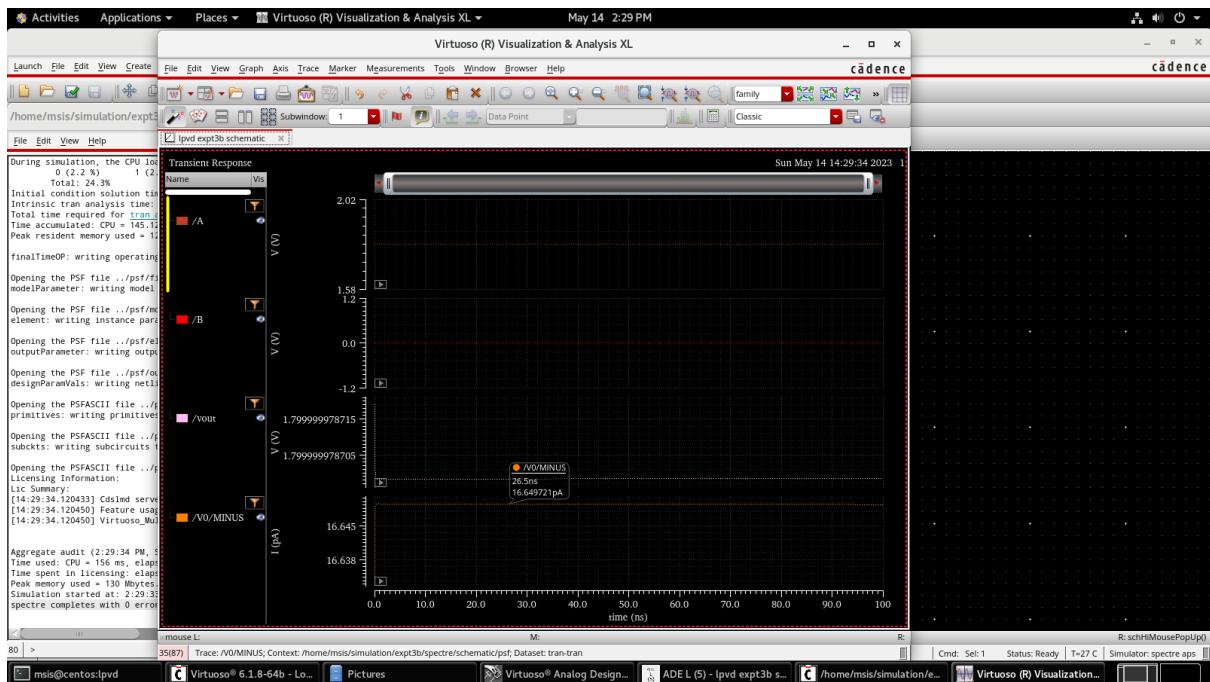
### Schematic



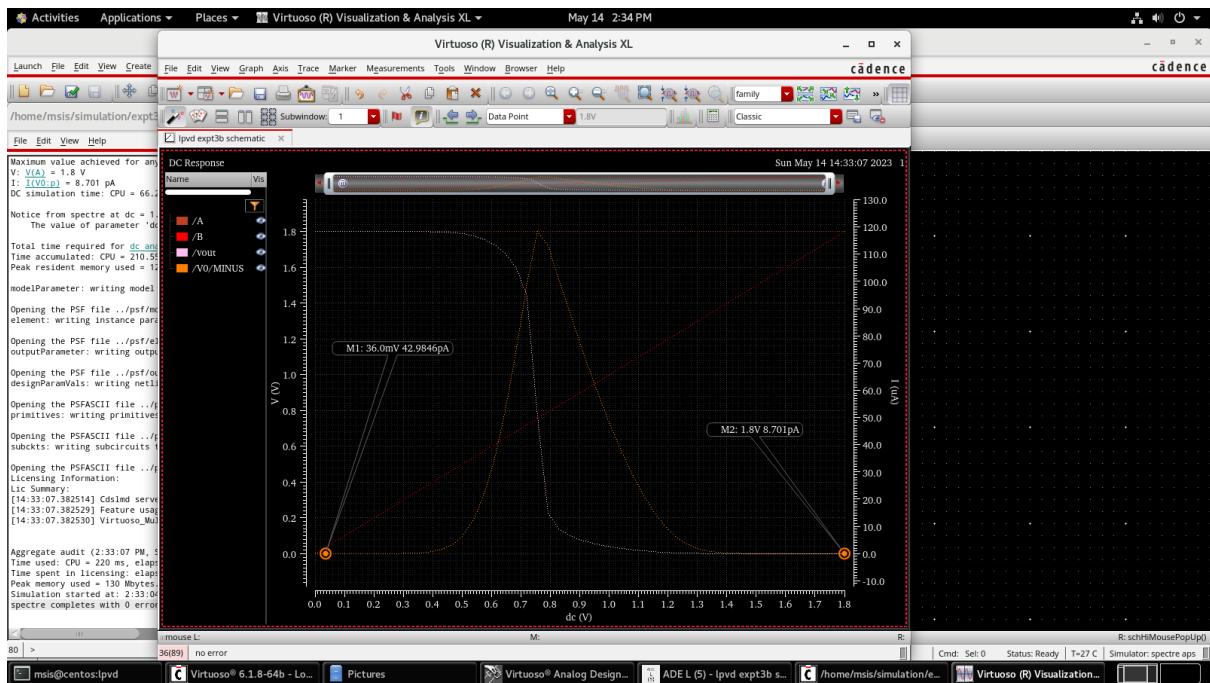
## Transient Analysis







## DC Analysis

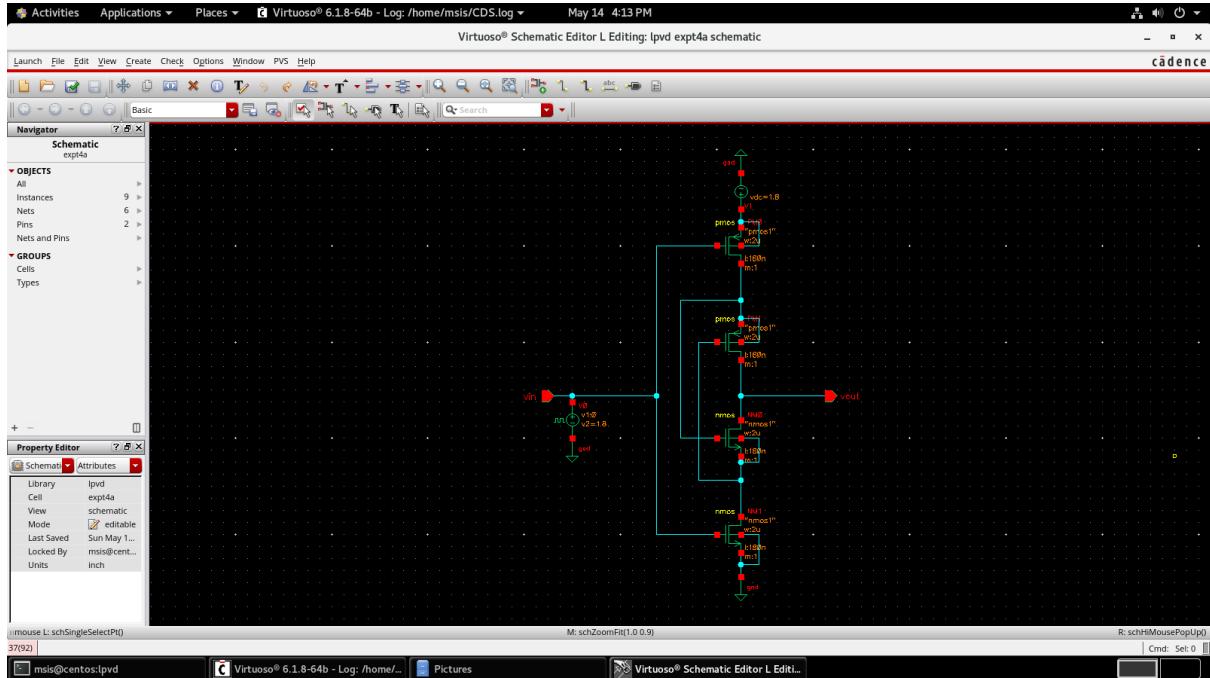


## Experiment4:

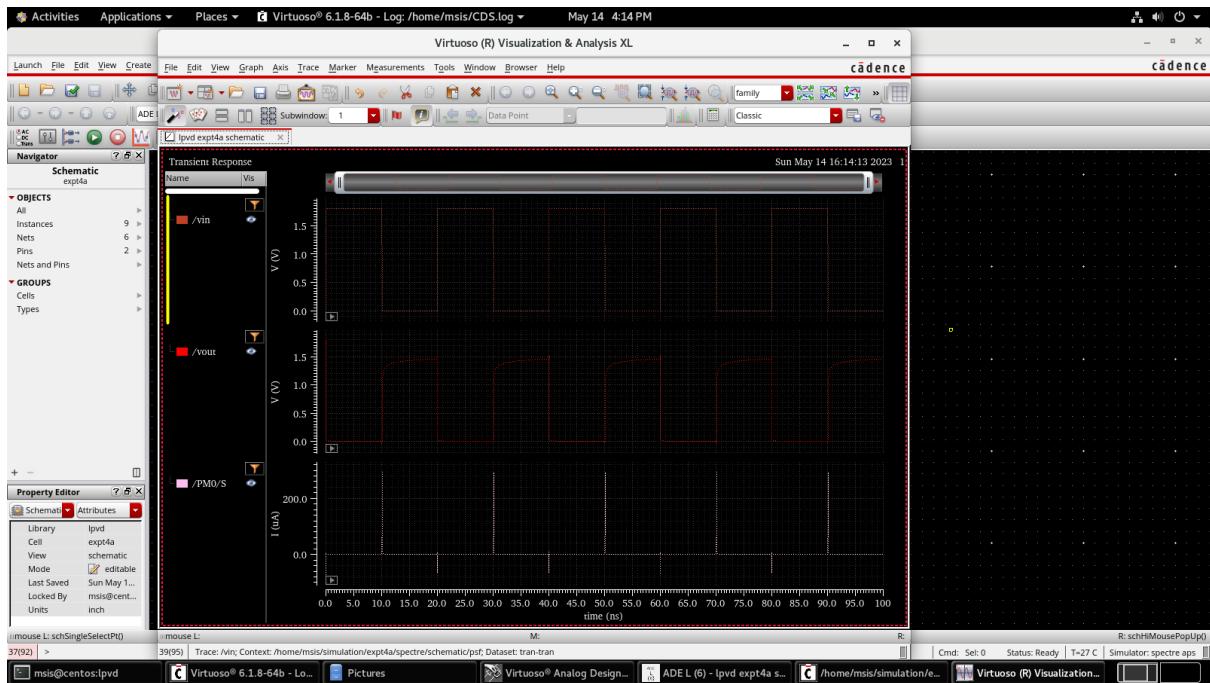
Artificial stacking – simulate function and leakage reduction compared to regular gate for

### a) LECTOR inverter

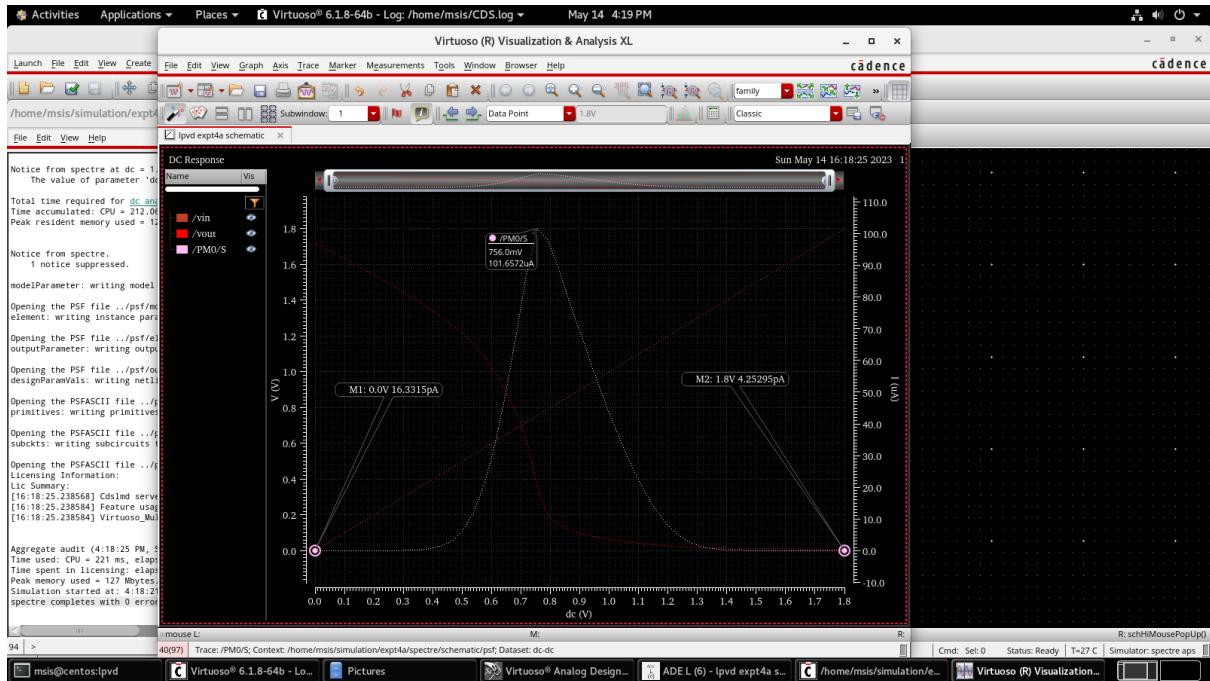
#### Schematic



#### Transient Analysis

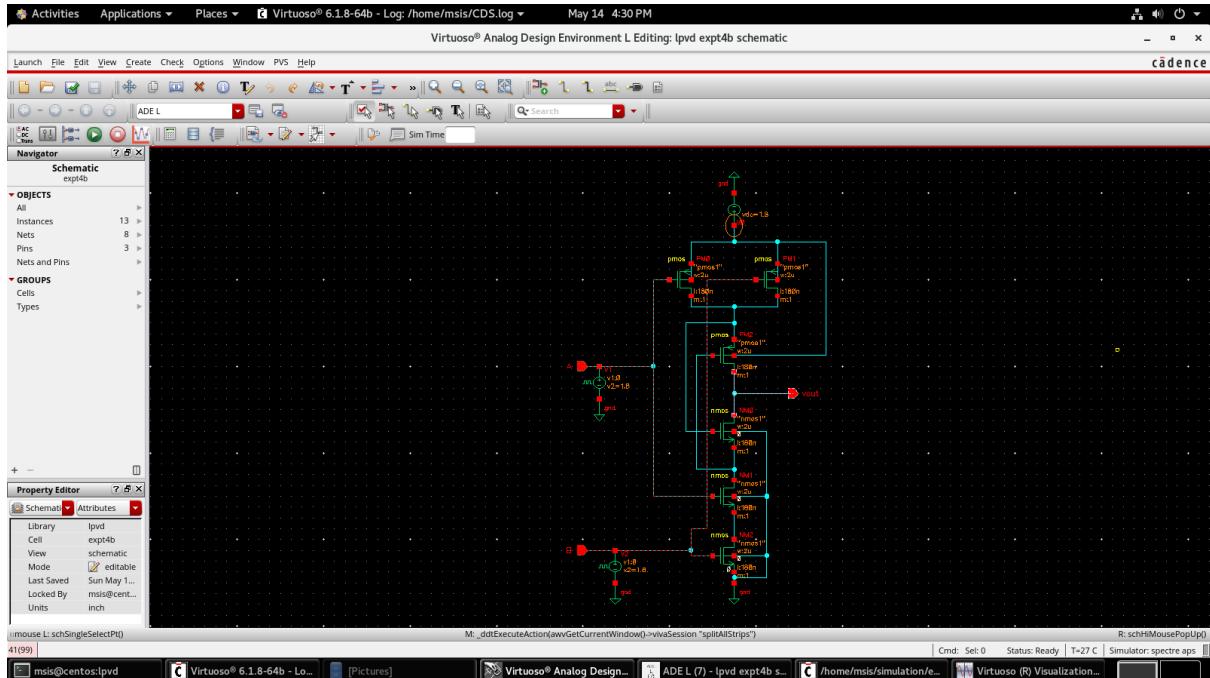


## DC Analysis

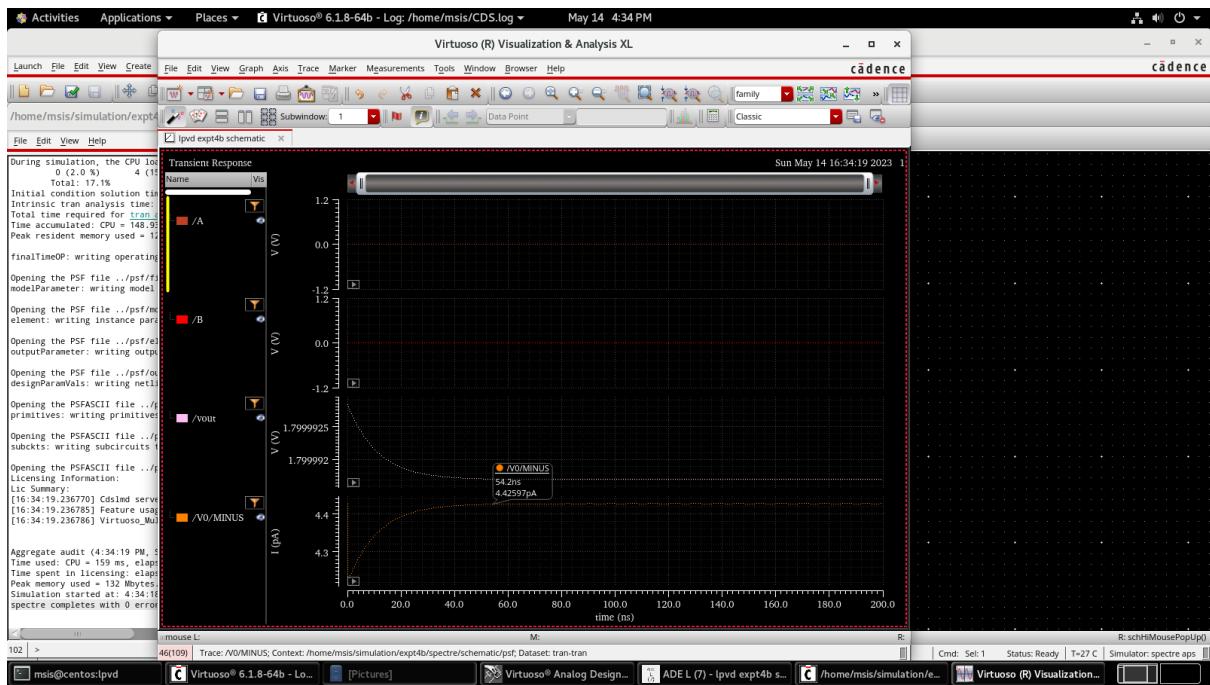


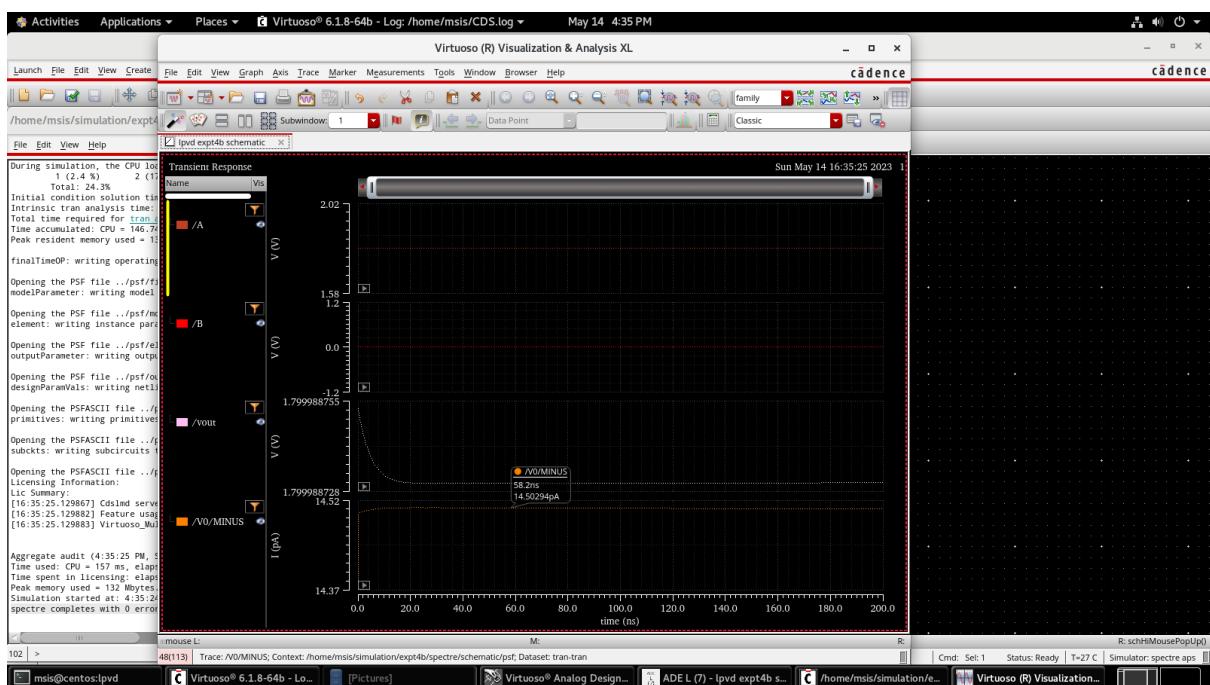
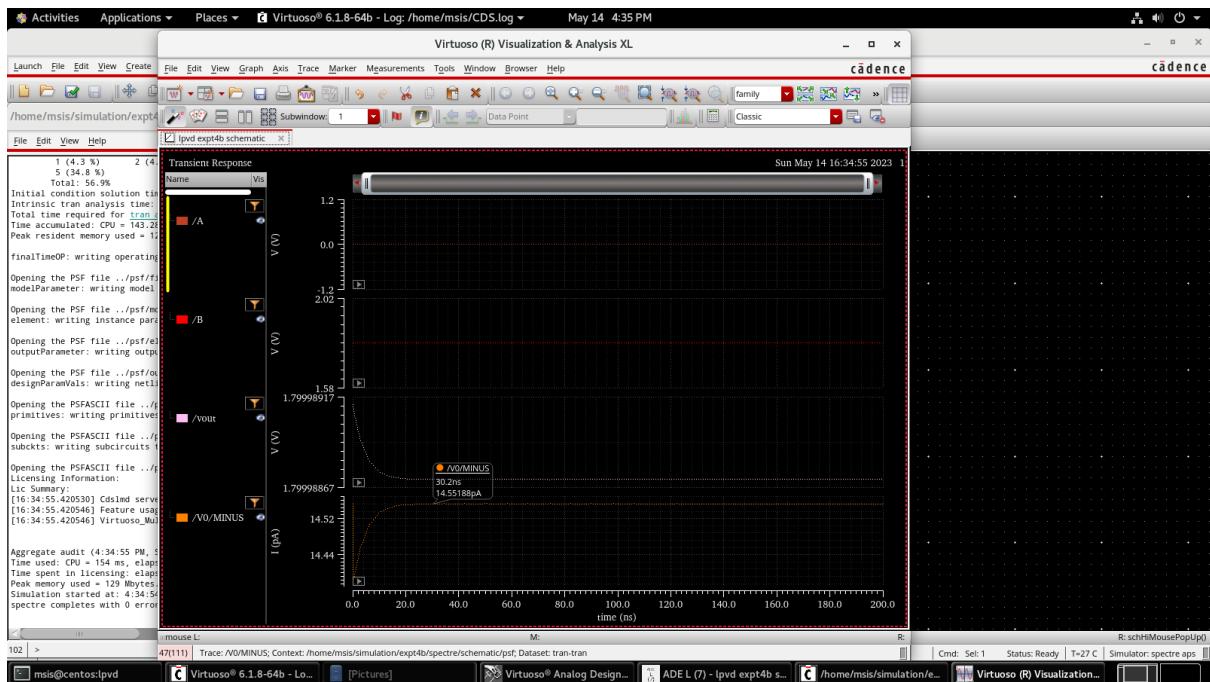
b) LECTOR 2 input NAND gate

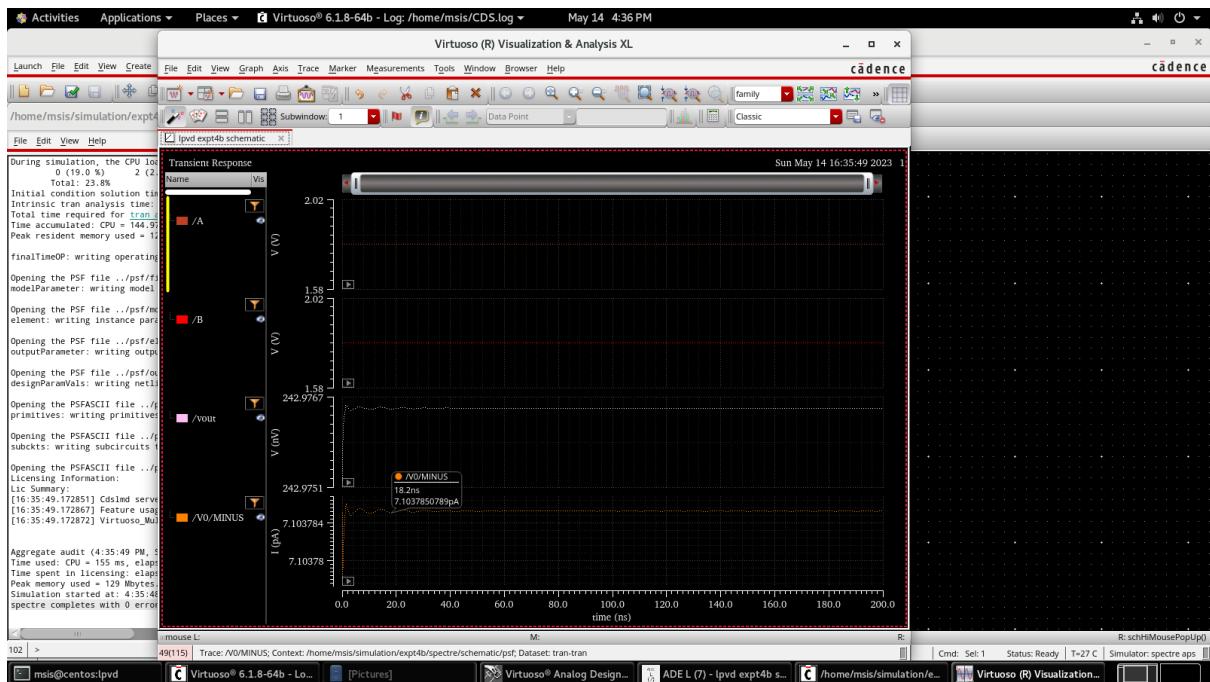
### Schematic



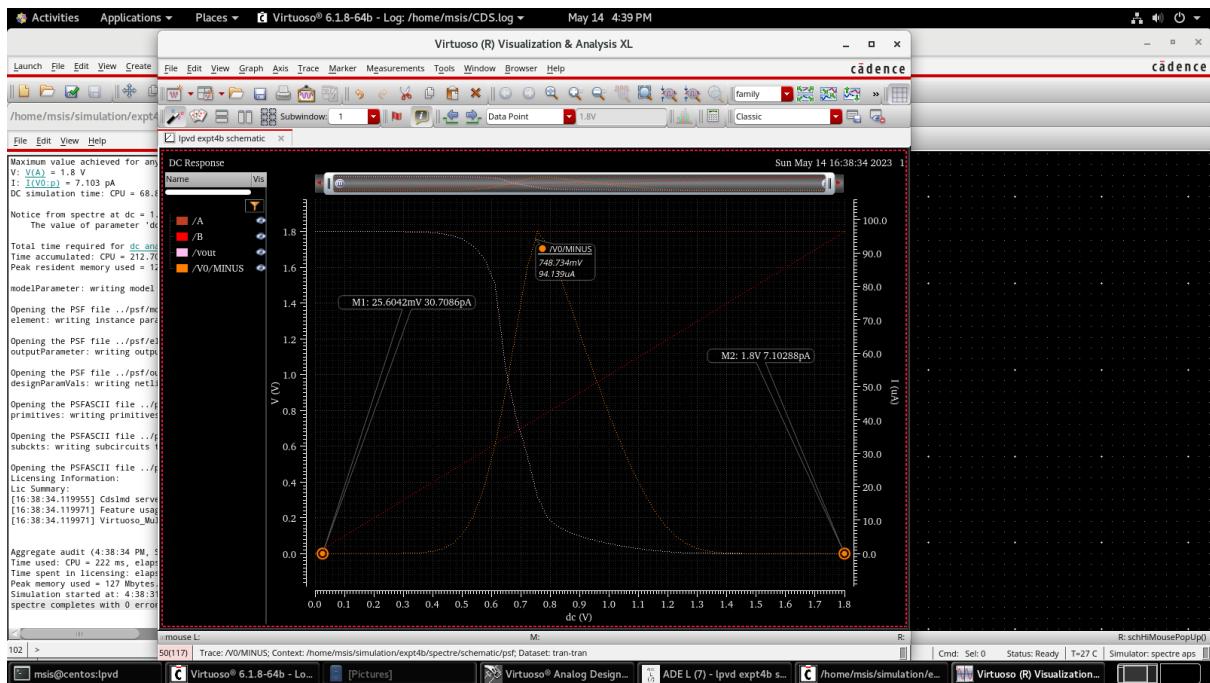
## Transient Analysis

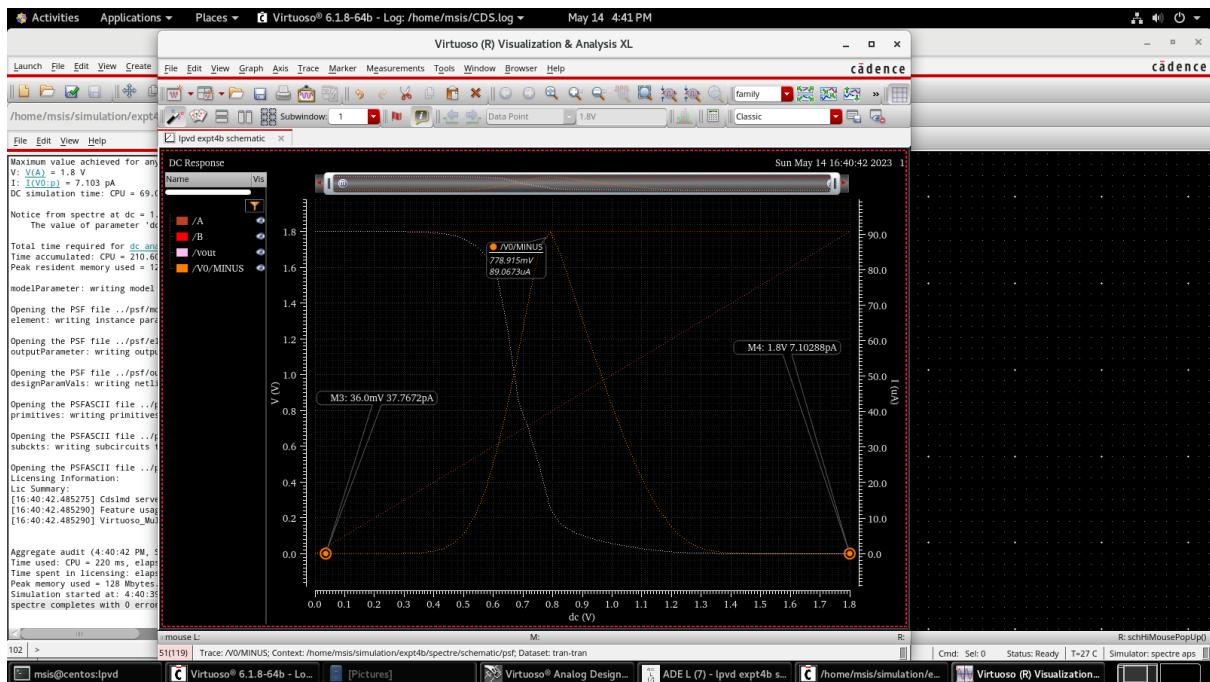






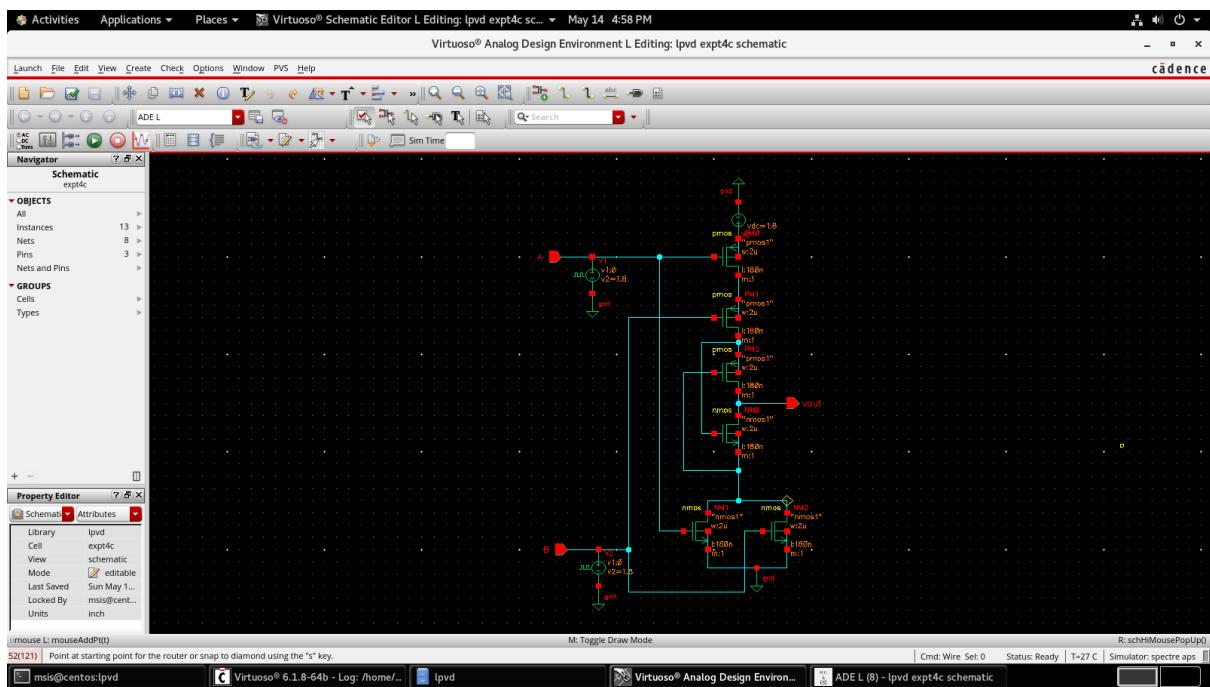
## DC Analysis



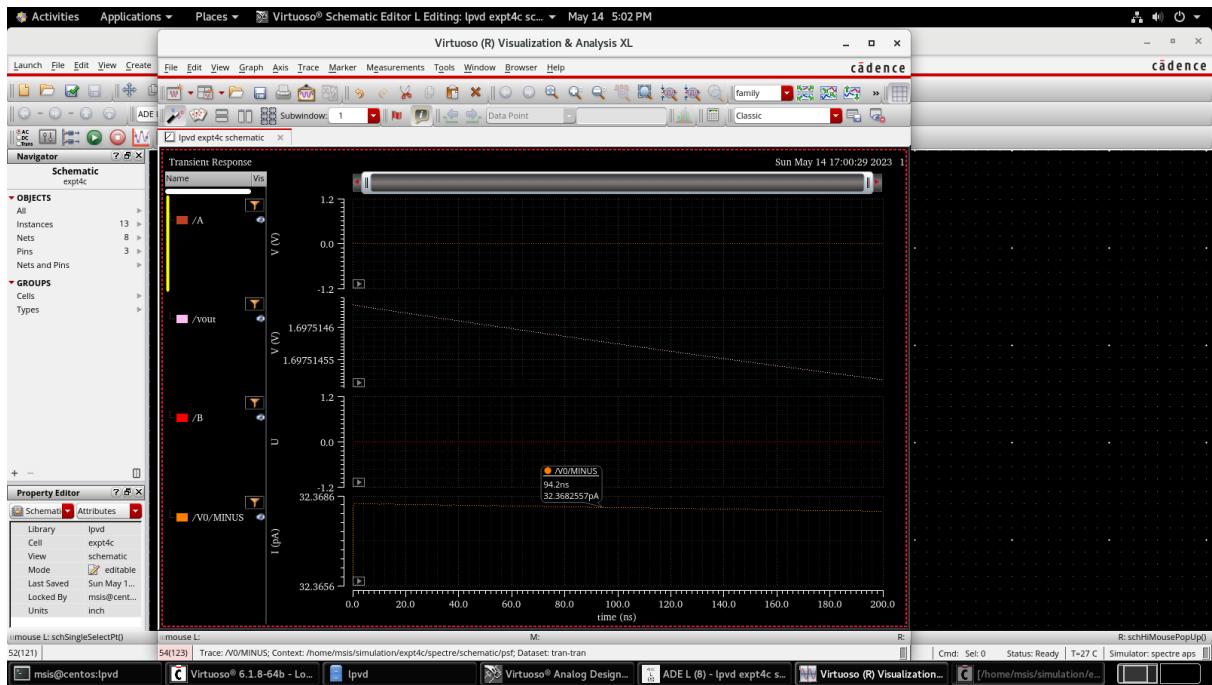


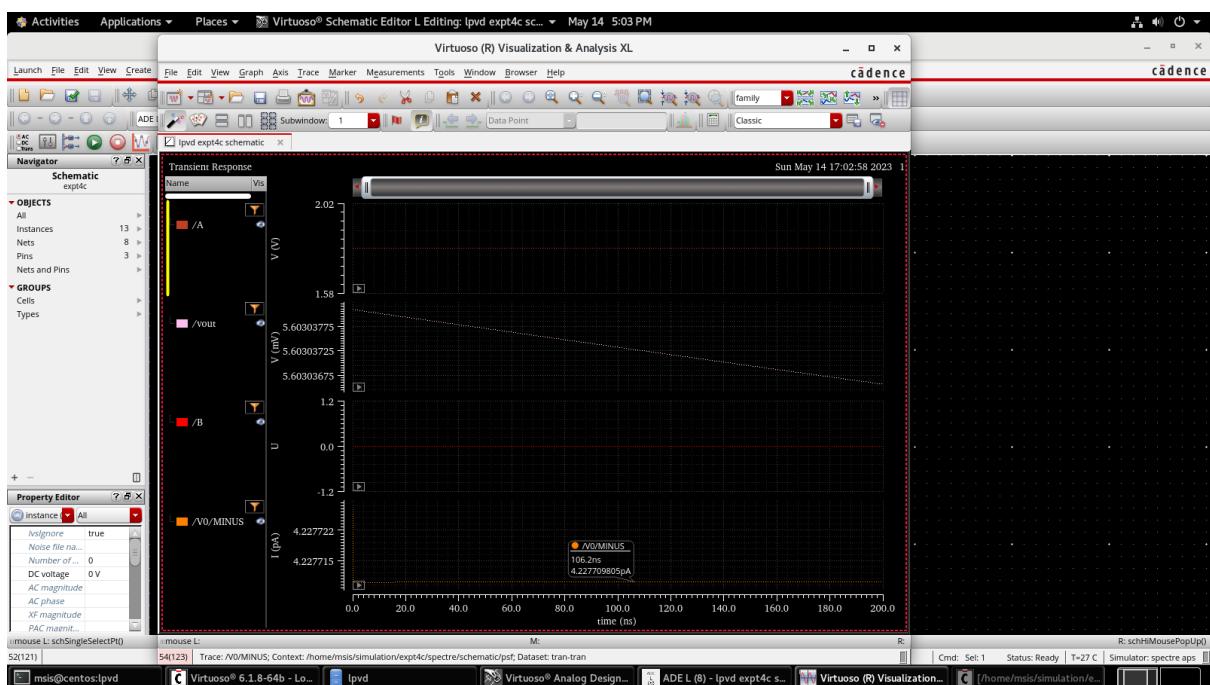
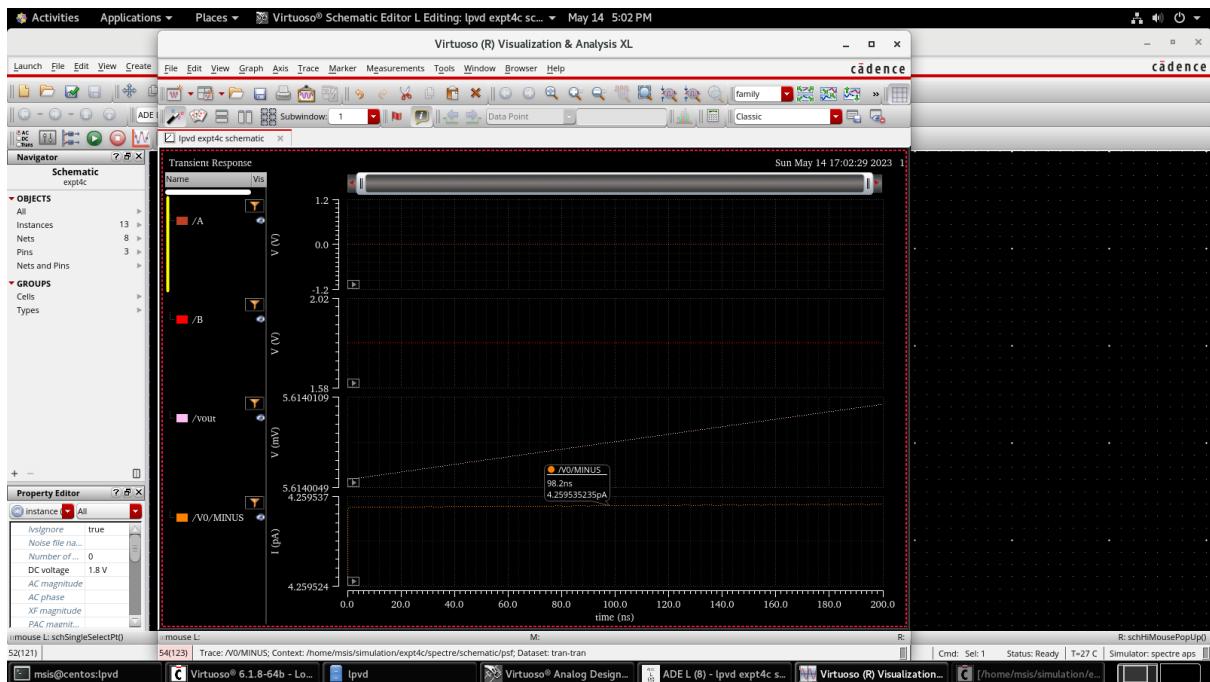
c) LECTOR 2 input NOR gate

### Schematic

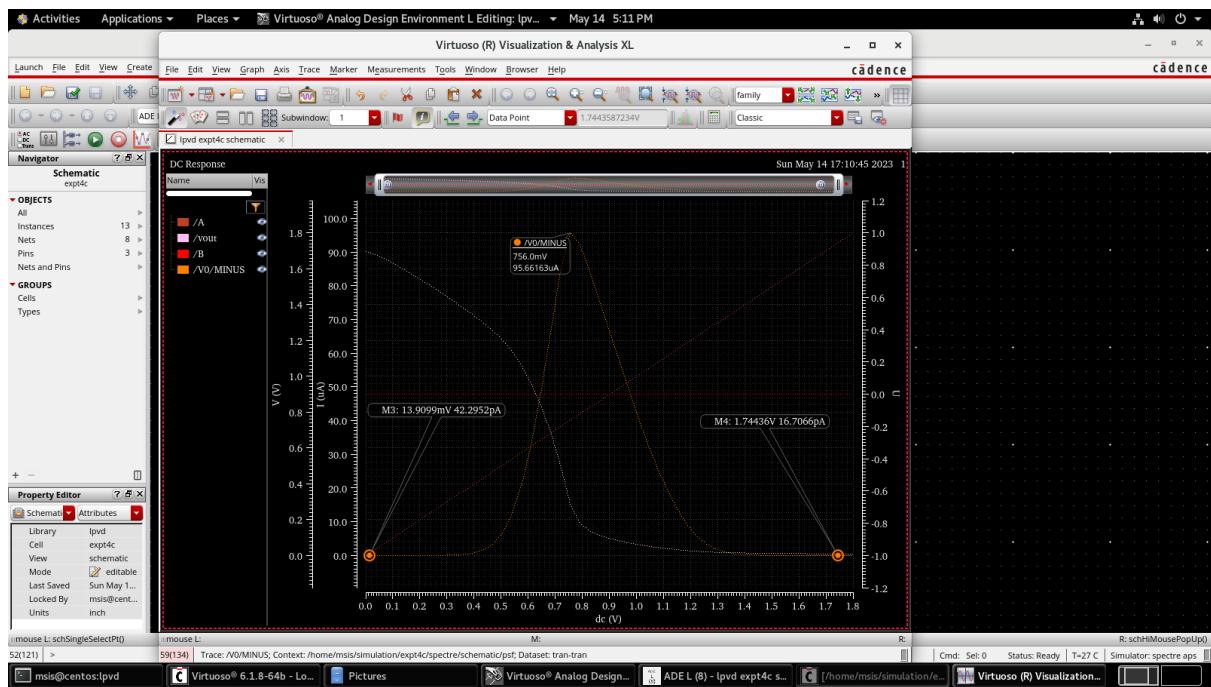
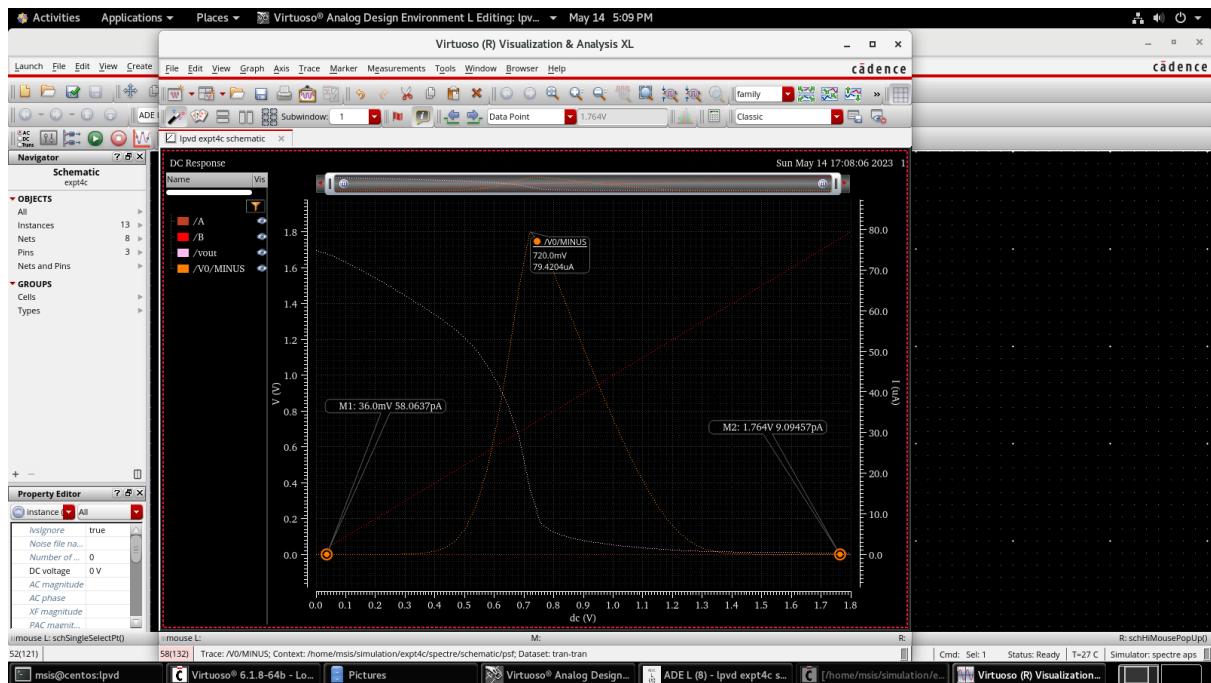


## Transient Analysis





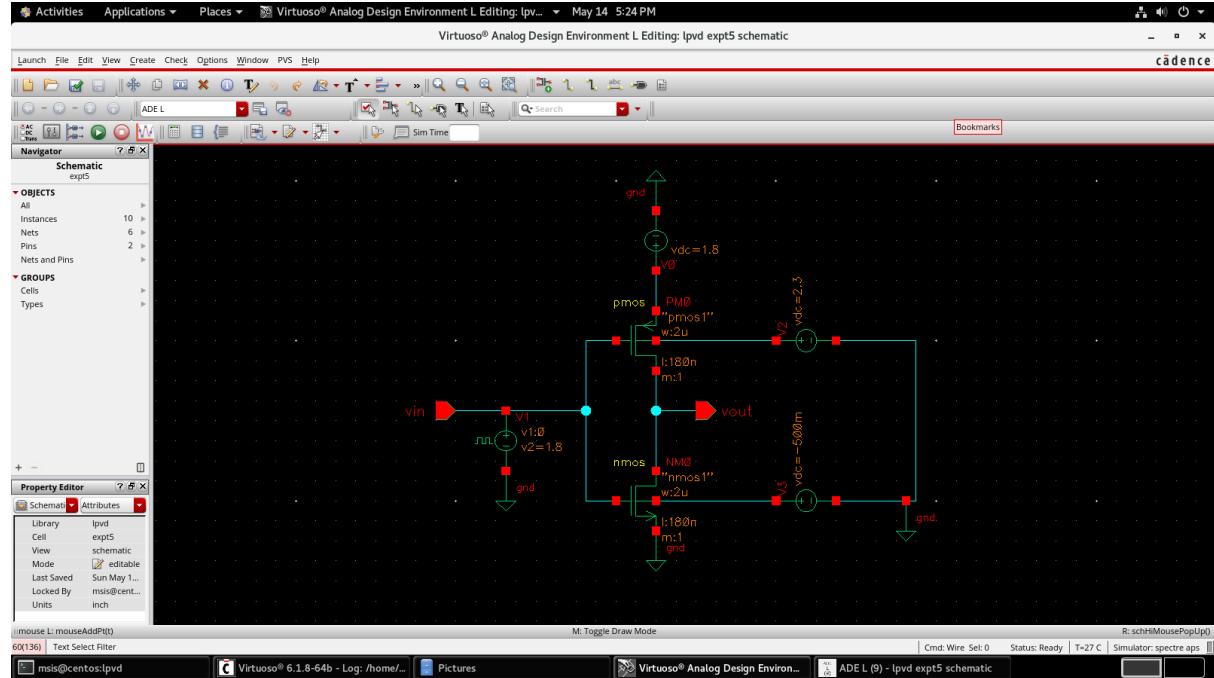
## DC Analysis



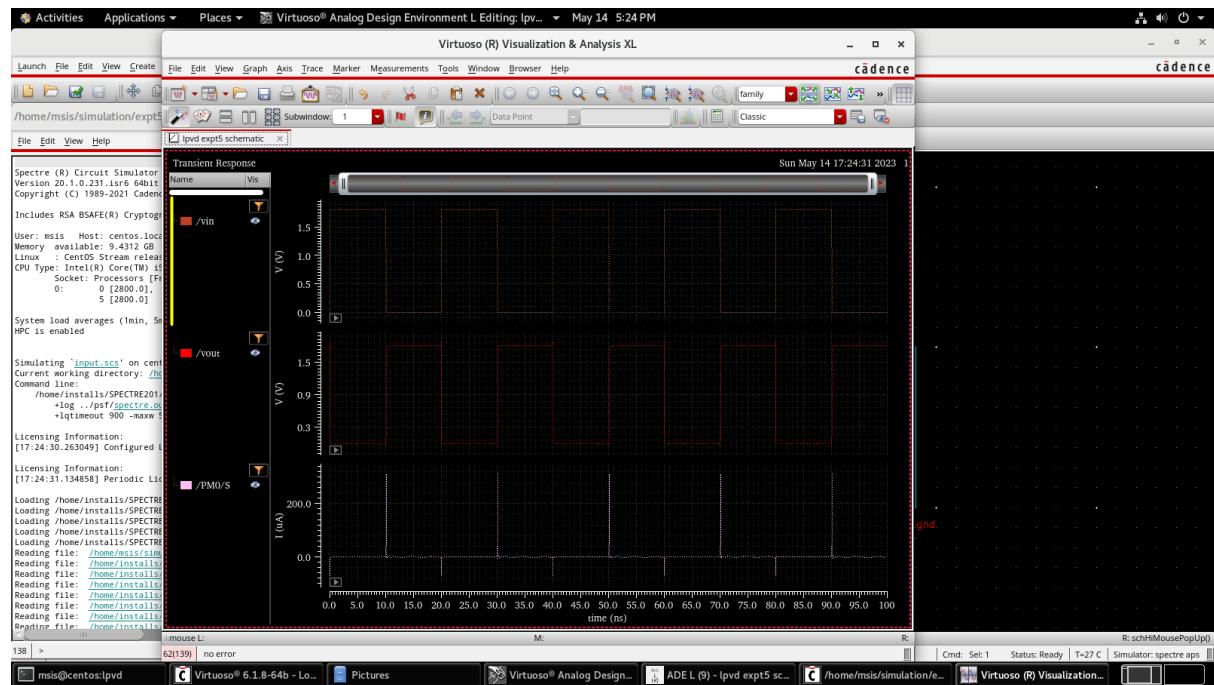
## Experiment5:

Multiple body biases - implement for inverter/NAND gate - check leakage for different Vsb

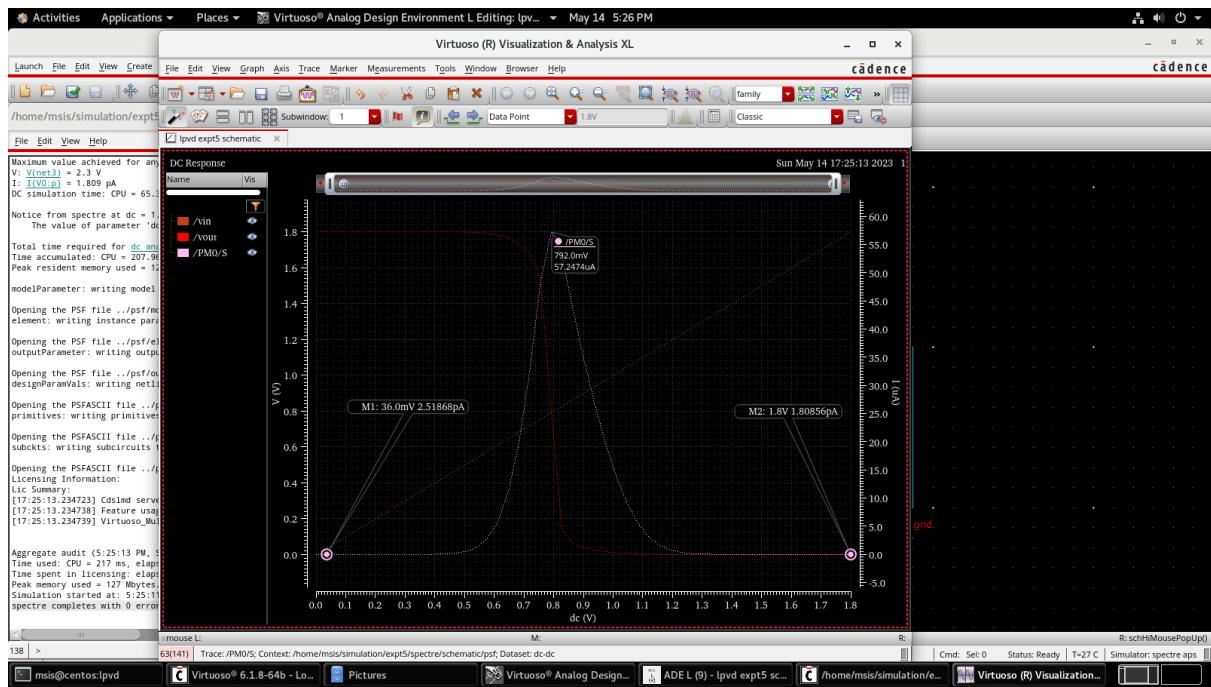
### Schematic



### Transient Analysis



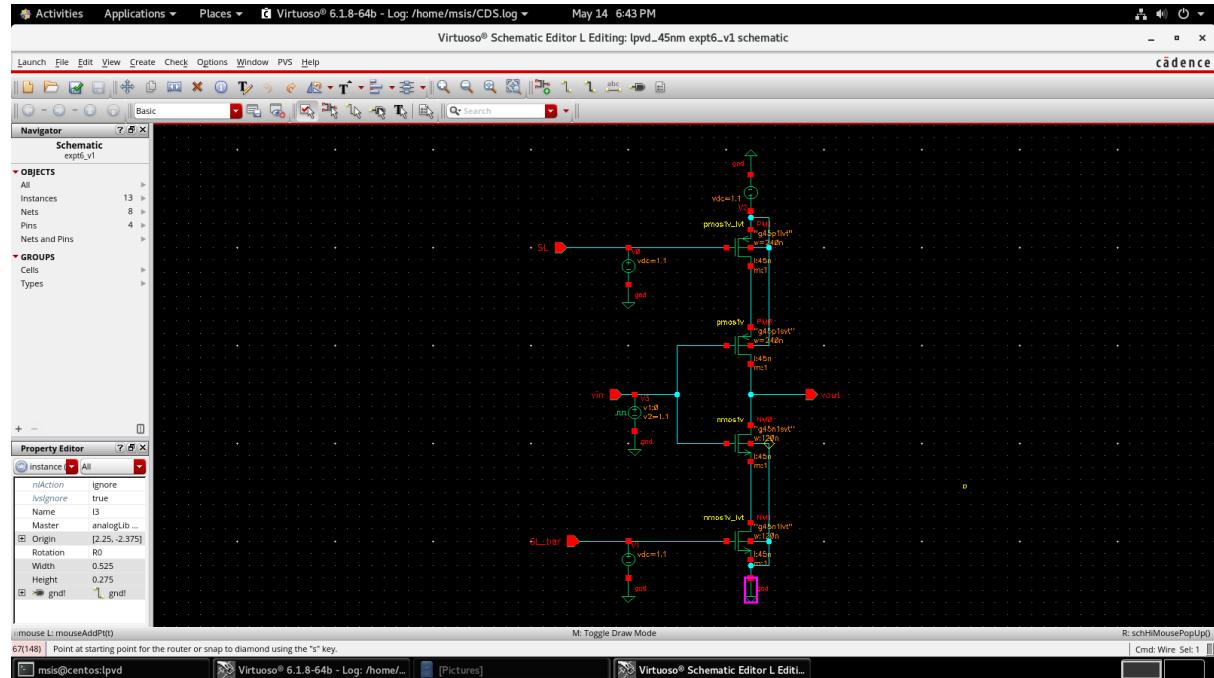
## DC Analysis



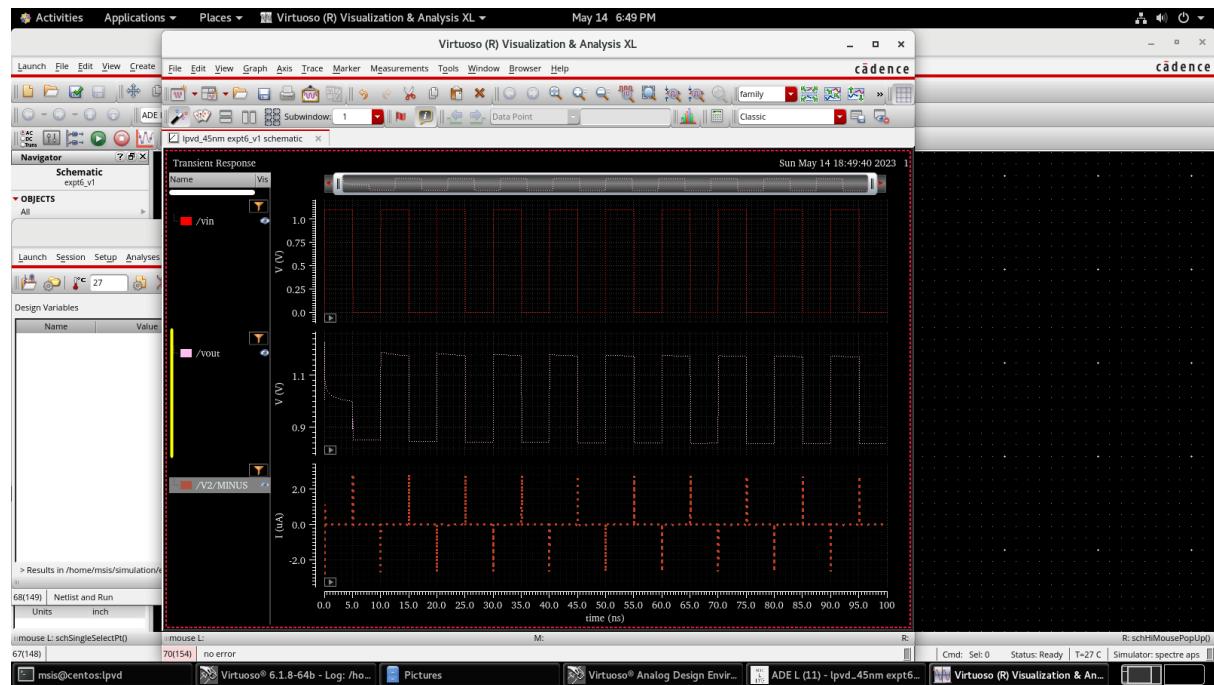
## Experiment6:

Super-cut off CMOS(SCCMOS) -check leakage for different gate biases in inverter/NAND gate.

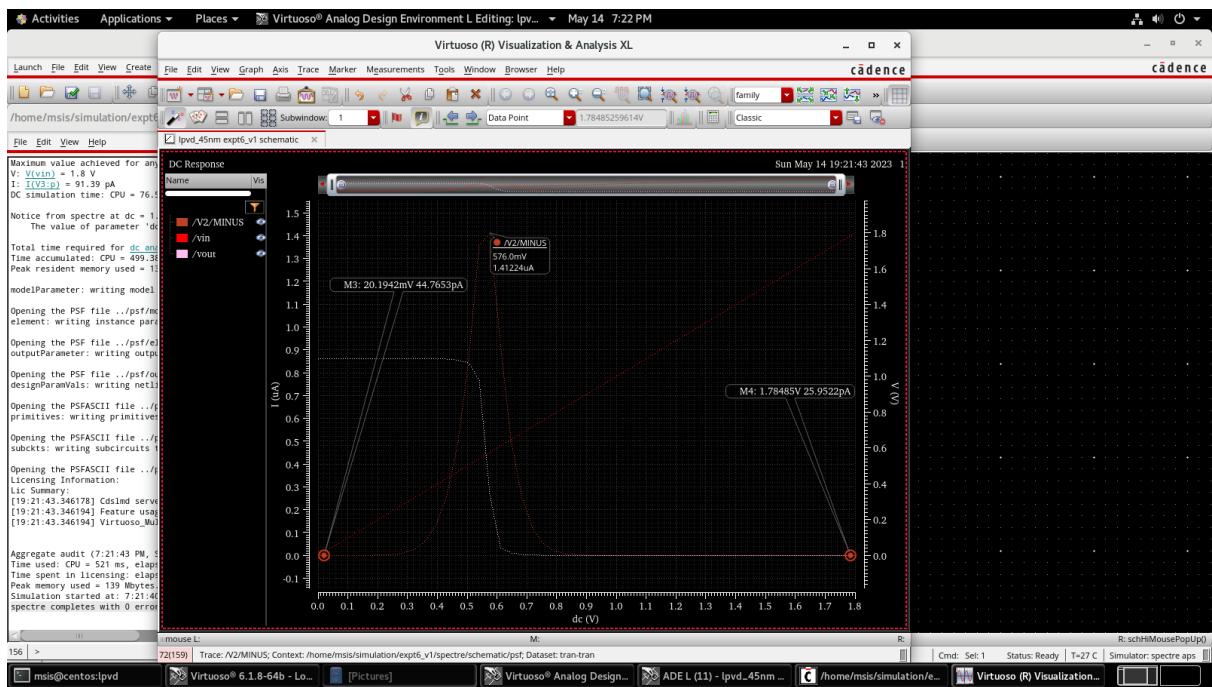
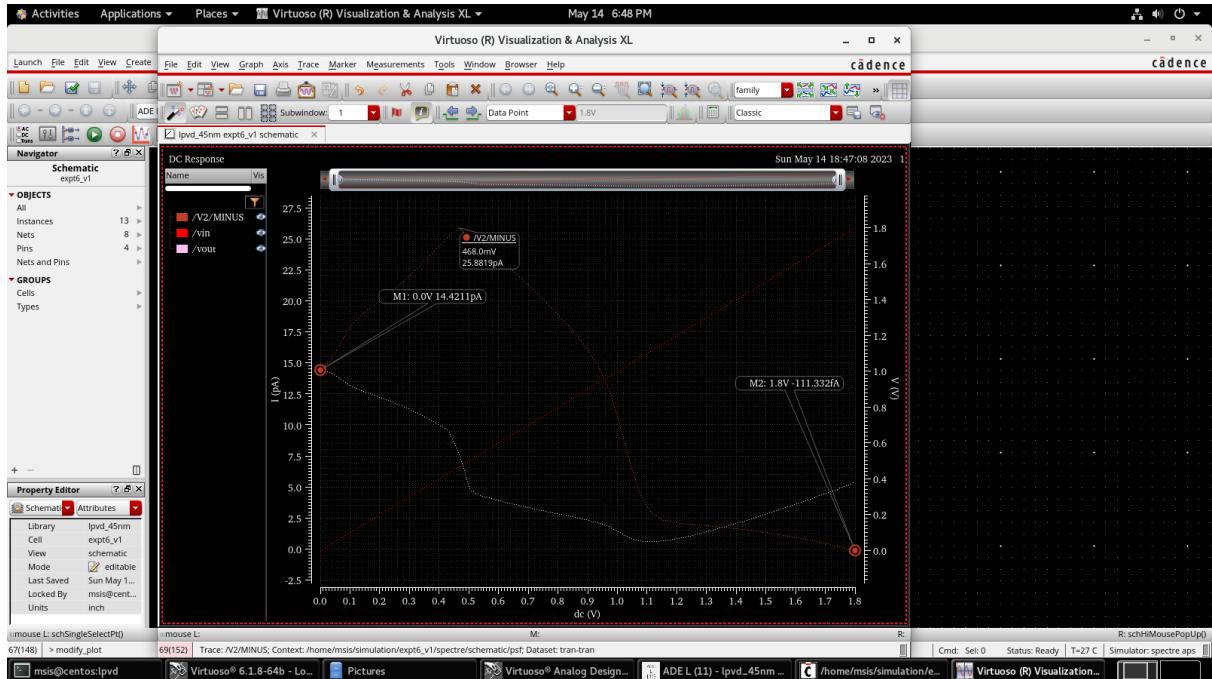
### Schematic

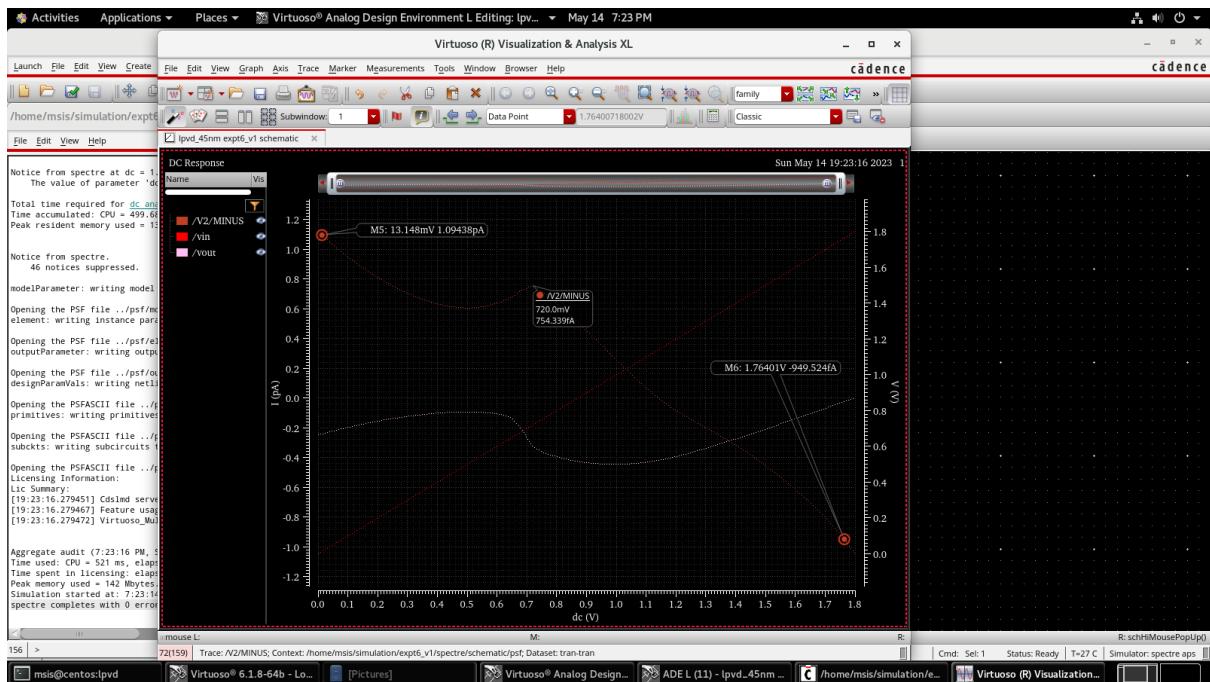


### Transient Analysis



## DC Analysis



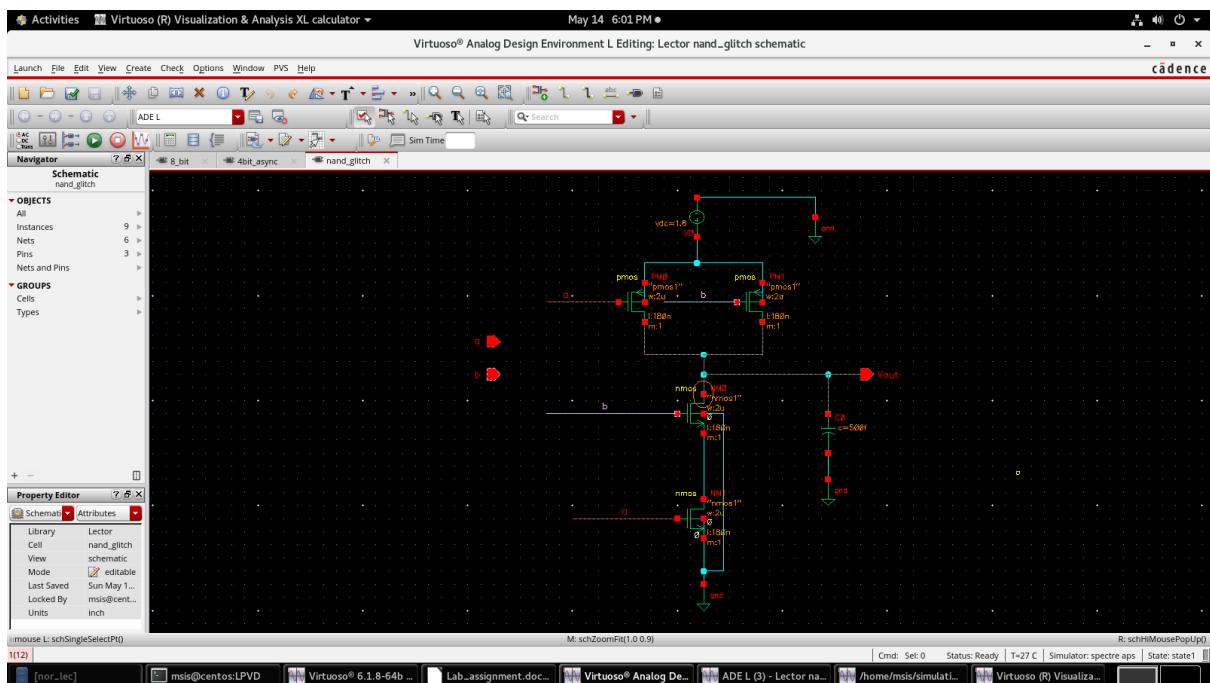


## Experiment7:

Plot glitch waveforms/power for a NAND gate, w.r.t. skew  $\tau$  showing its dependency on the following.

- Output load
- Input pattern
- Input slope

## Schematic



## Transient Analysis

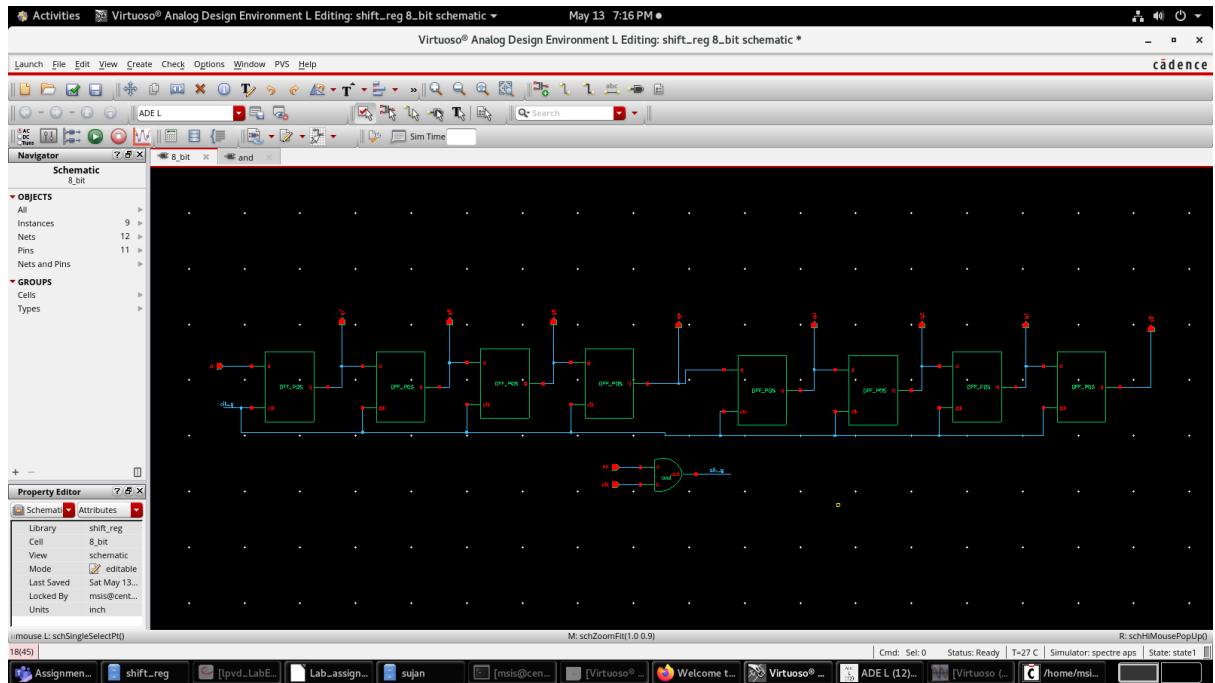


## Experiment8:

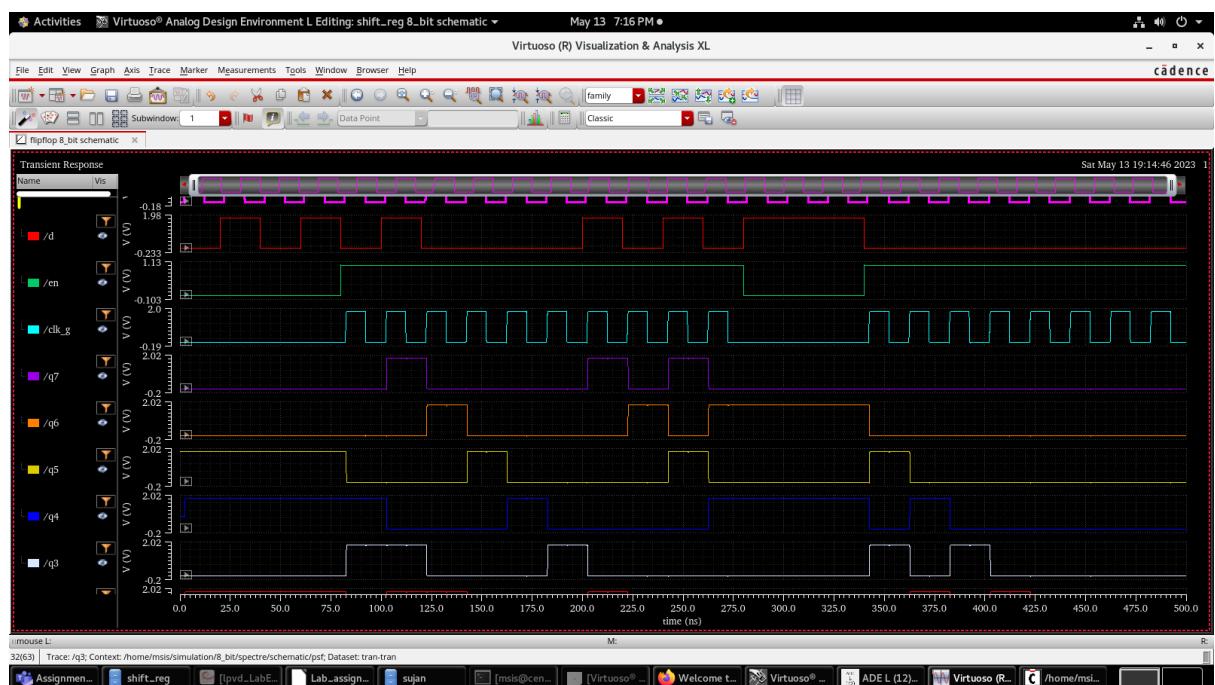
Design and simulate latch based clock gating circuits for the following blocks:

a) 8 bit shift register

### Schematic



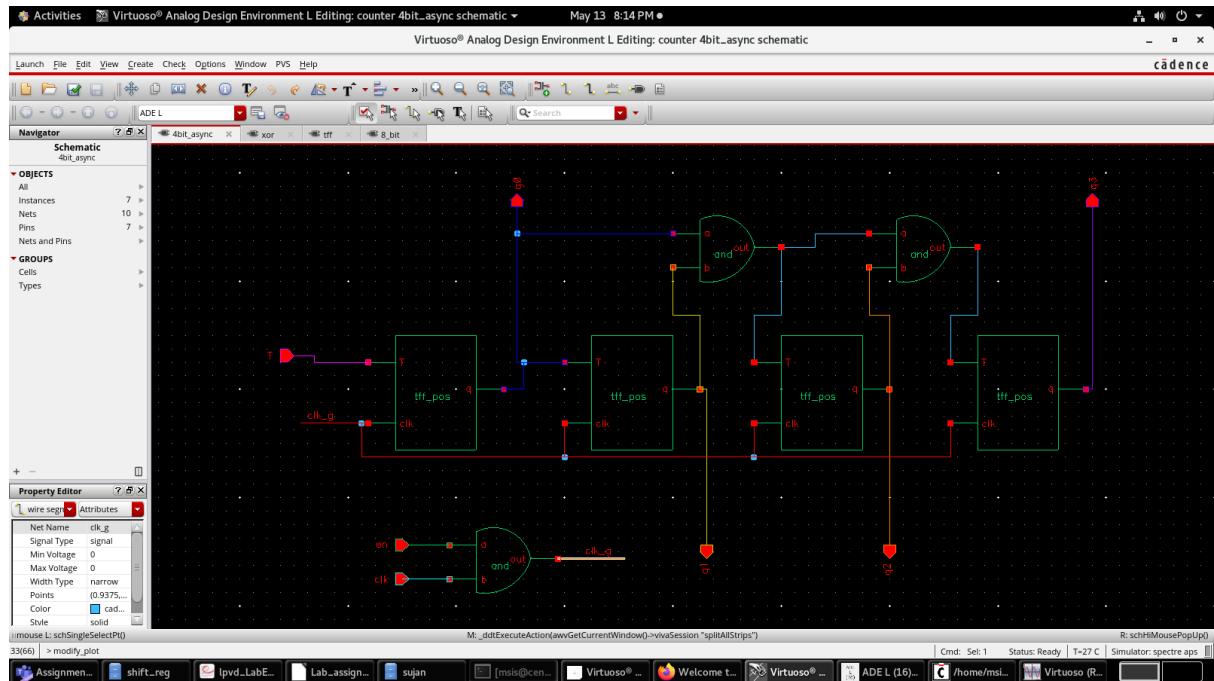
### Transient Analysis



Clock is gated using en signal along with and gate. Only when en is HIGH, clock is enabled.

### b) 4 bit synchronous counter

#### Schematic



#### Transient Analysis

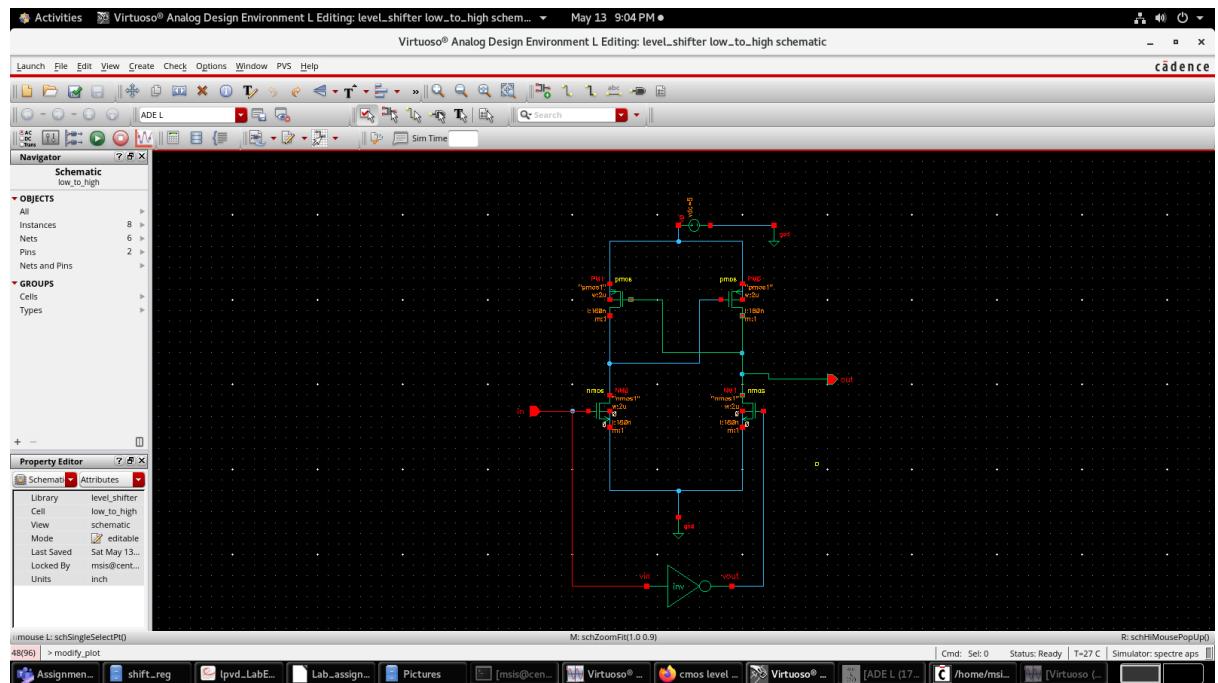


### Experiment9:

Design the following Level shifter circuits. Assume your own VDDH and VDDL values.

a) Low to High voltage(VDDH=5v,VDDL=1.8v)

#### Schematic

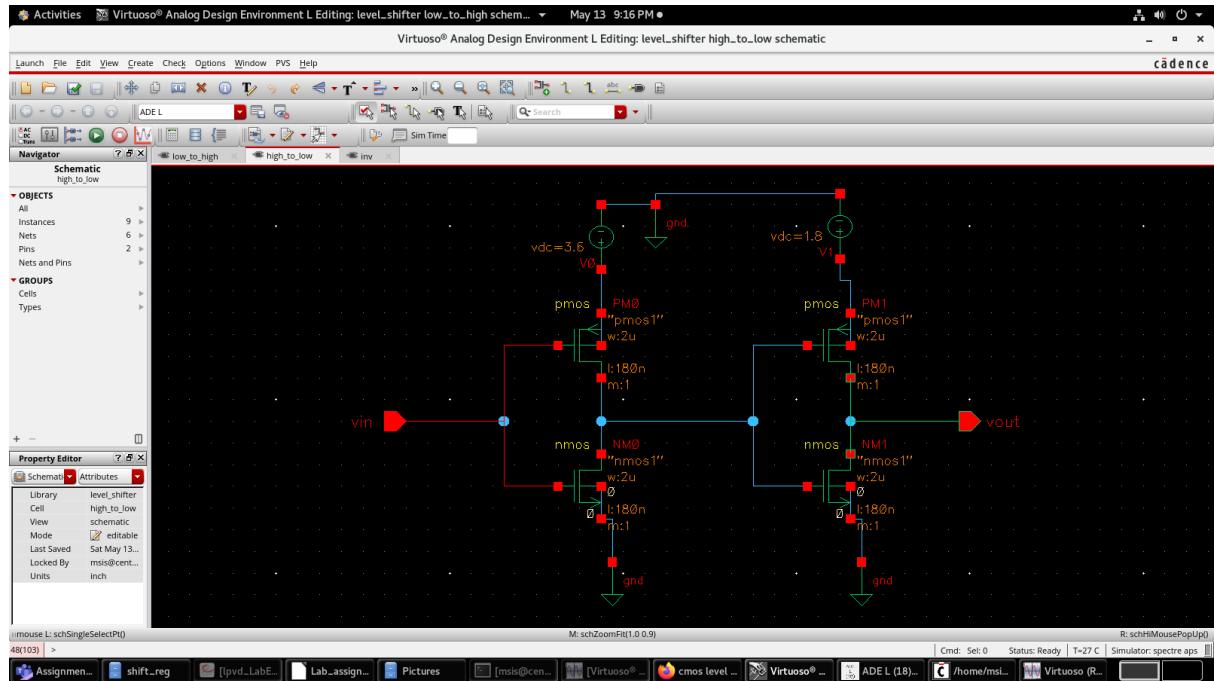


#### Transient Analysis



## b) High to low voltage

Schematic



Transient Analysis

