## Design of Differential Amplifier

**Objective:**
Design a differential amplifier circuit using 180nm CMOS technology. The amplifier should meet the following specifications:
Gain: Differential voltage gain of at least 50 dB.
Common-Mode Rejection Ratio (CMRR): Greater than 60 dB.
Power Supply: Single-ended +1.8V and ground.

**Instructions:**
Design the schematic for the differential amplifier using CMOS transistors and passive components.
Choose appropriate transistor sizes and biasing techniques to achieve the desired gain and CMRR.
Implement measures such as current mirrors or active loads to enhance CMRR.

Given Data:

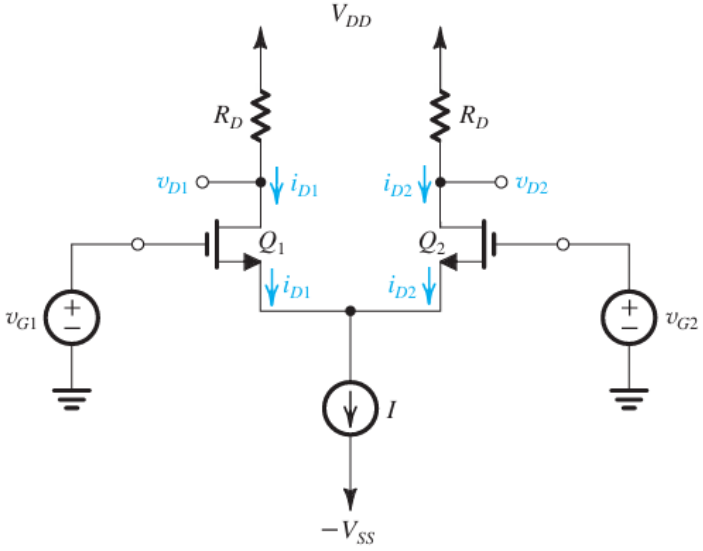
**Voltage Gain**
Av = 50 dB
$50 = 20 \log_{10} (Av)$
$Av = 10^{(50/20)}$
Av = 316.227
**Av = 316**

**Common Mode Rejection Ratio**
CMRR = 60 dB
$60 = 20 \log_{10} (CMRR)$
$CMRR = 10^{(60/20)}$
CMRR = 1000
**CMRR = 1000**

Assumptions:

VD = 1V
VG = 0.6V
VTH = 0.45V
Kn = 200 µA/V$^2$
I = 100 µA
L = 1 µm

# 1. Simple MOS Differential Pair with Resistor Load



Fix the value of VD by setting appropriate value for RD.

The voltage at the drain terminal is given by.

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$$

Select RD = 1K

1 = 1.8 – (ID/2) * 1K

0.8 = (ID/2) * 1K

1.6 = ID * 1K

**ID = 1.6m**

Calculate the value of Gm:

$$|\mathbf{A_v}| = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} \times R_D$$

i.e. Av = Gm * RD

316 = Gm * 1K

**Gm = 316m**

Calculate the Value of W:

$$\mathbf{G_m} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$(316m)^2$ = 200µ (W/L) 1.6m

99.856m = 320n (W/L)

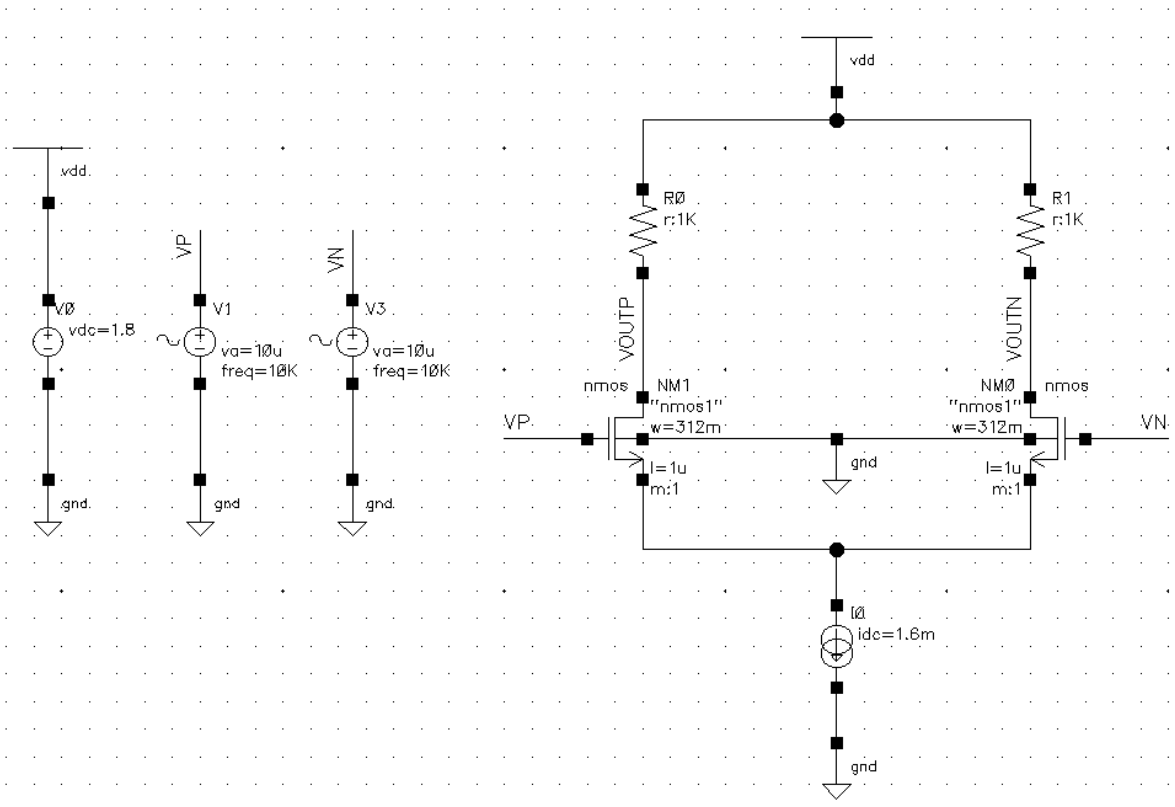
W/L = 312050

If L = 1 µ

**W = 312050u = 312m**

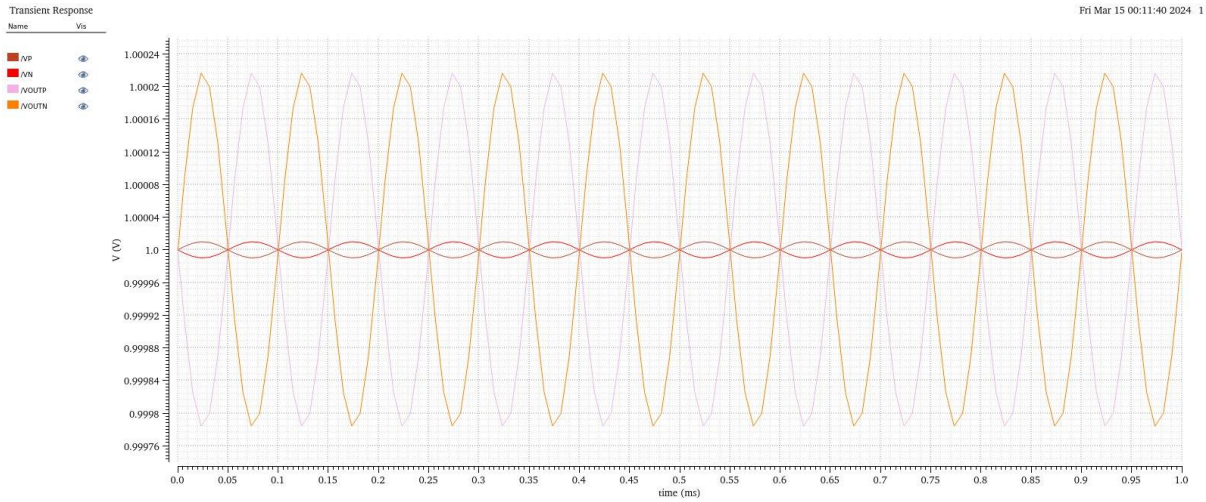
For 50 dB gain the value of transistor width is not practical for single stage amplifier.

Still, it can be simulated to verify the results.




Run DC analysis and verify the DC operating points.

Run Transient Analysis and calculate the gain.



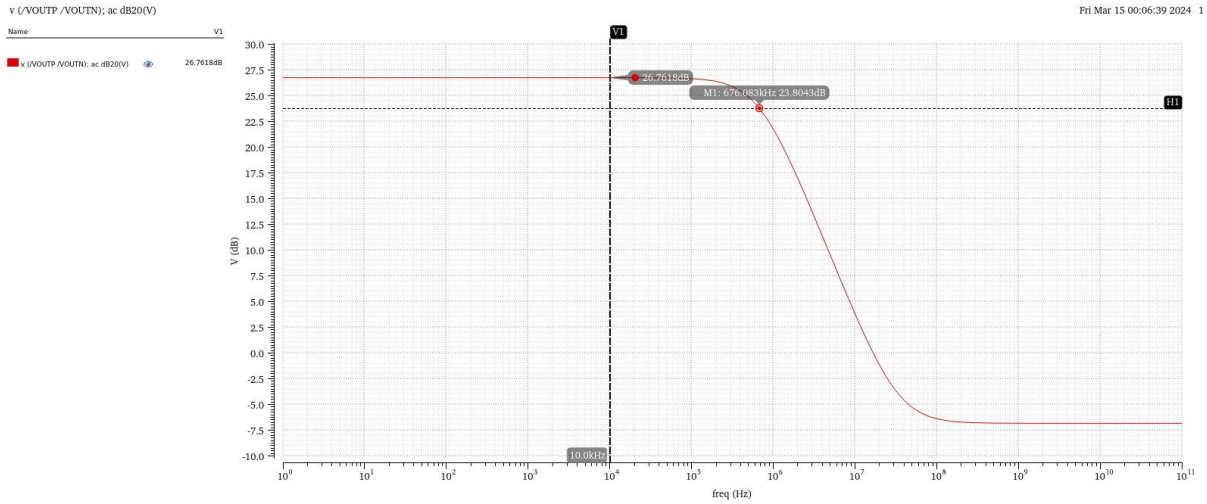

VP = 20uV peak to peak

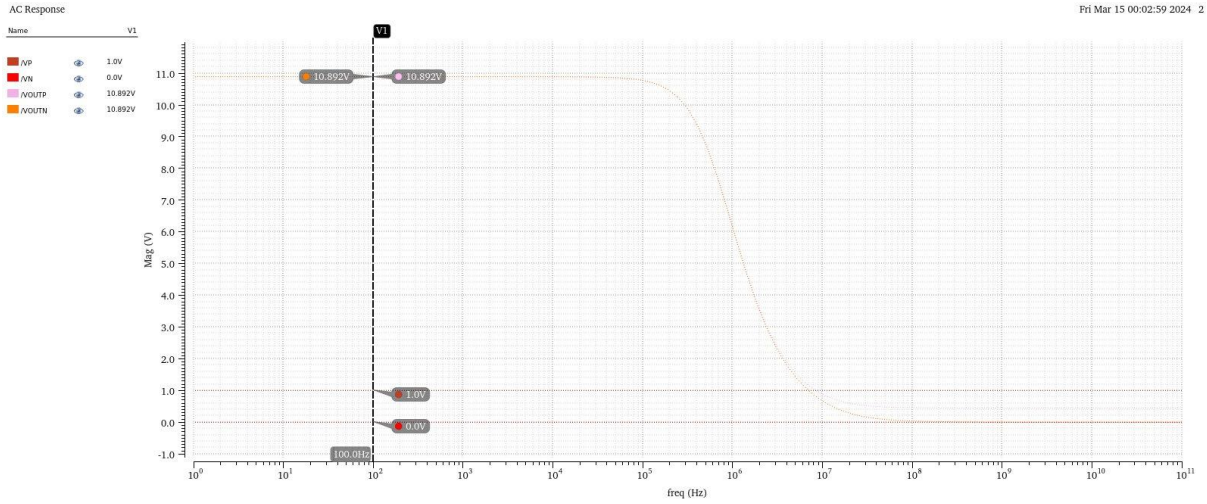
VN = 20uV peak to peak

VOUTP = 432uV peak to peak

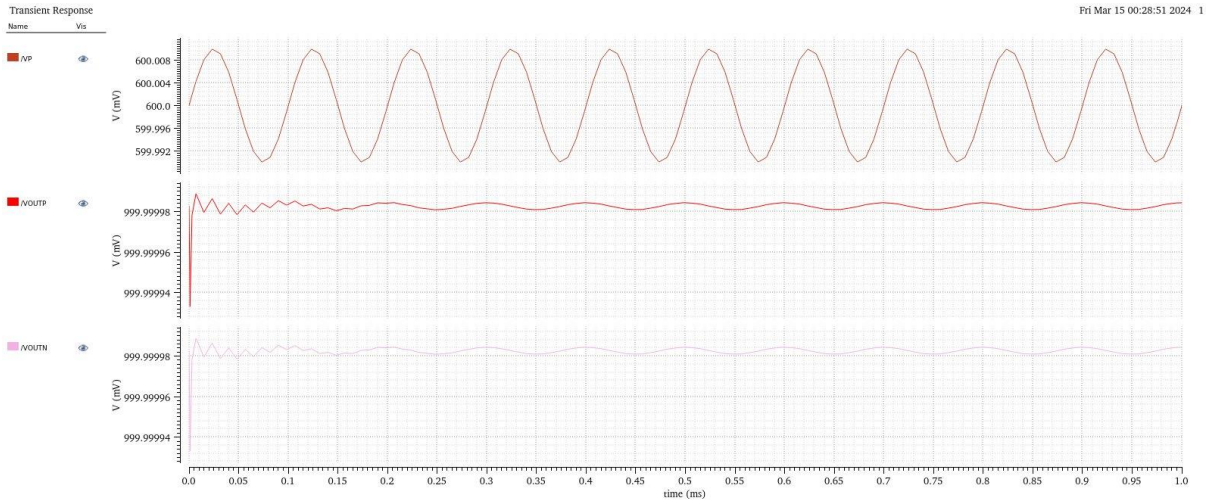
Differential Gain = 21.6 v/v = **26.68 dB**

Run AC analysis and plot gain.




Apply Common mode input voltage and run transient analysis.

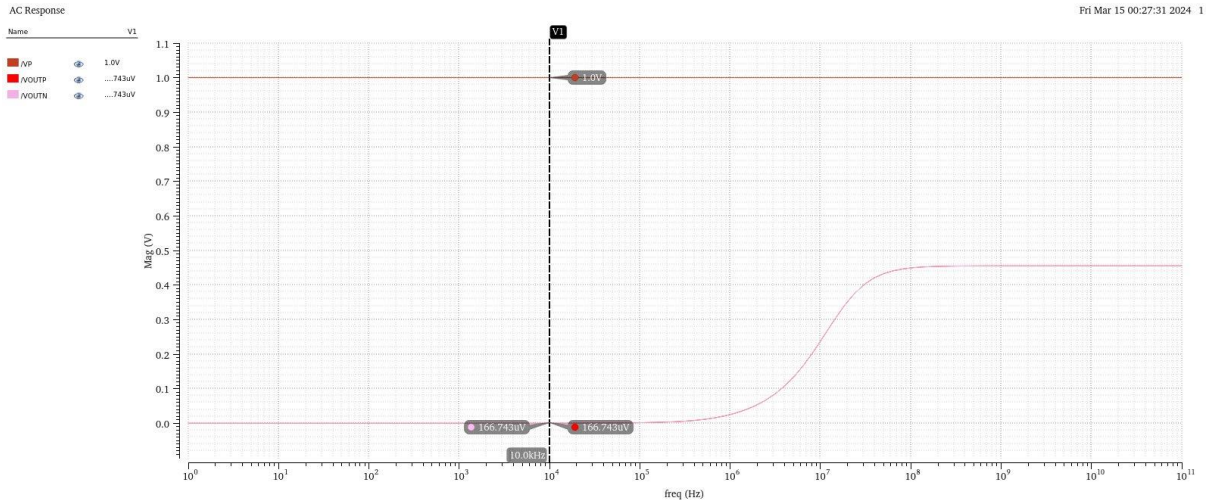


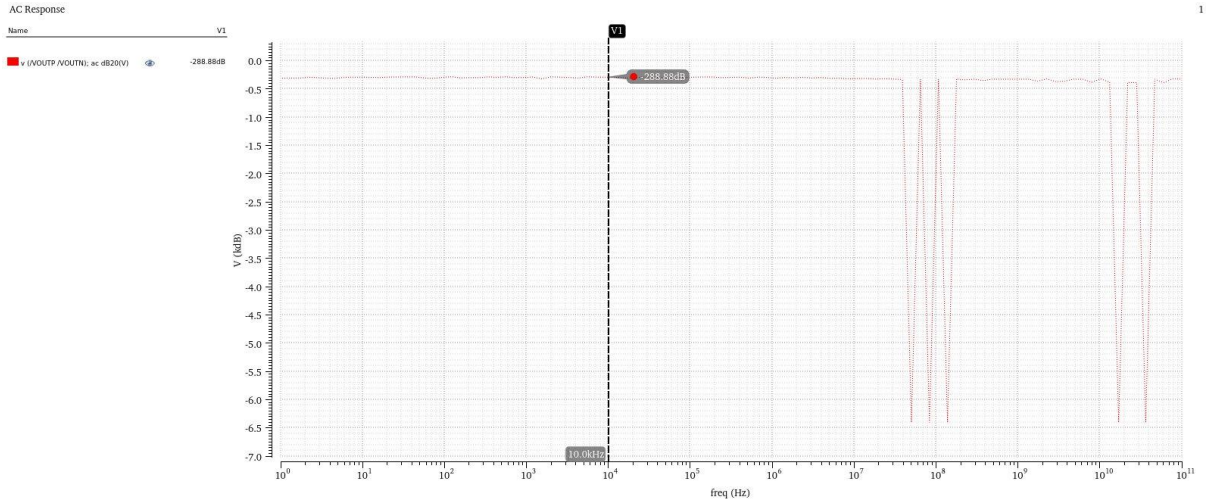

VP = VN = 20uV peak to peak

VOUTP = 53uV peak to peak

Common Mode Gain = 2.65 v/v = **8.46 dB**

Apply Common mode input voltage and run AC analysis.




Observations:

| | Theoretical | Practical |
|---|---|---|
| gm | 316m | 23.7131m |
| IDS | 800m | 800.488m |
| Ad | 50 dB | 26.7618 dB |
| Ac | 0 | -288.88 dB |
| CMRR | 60 dB | 315 dB |

As the theoretical and practical values of gm show huge deviation required gain cannot achieved using single stage differential amplifier.

Hence two stage differential amplifier must be designed to achieve required gain.

Design First stage differential amplifier to have a gain of 20 dB and design a second stage common source amplifier to provide additional gain.

# 2. First Stage Differential Amplifier with Resistor Load

**Voltage Gain**
Av = 20 dB
$20 = 20 \log_{10} (Av)$
$Av = 10^{(20/20)}$
**Av = 10 V/V**

Fix the value of VD to 1V by setting appropriate value for RD.

The voltage at the drain terminal is given by.

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D$$

Select ID to be 100µA

1 = 1.8 – (100µ/2) * RD

0.8 = (100µ/2) * RD

**RD = 16K**

Calculate the value of Gm:

$$|\mathbf{A_v}| = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} \times R_D$$

i.e. Av = Gm * RD

10 = Gm * 16K

**Gm = 625µ**

Calculate the Value of W:

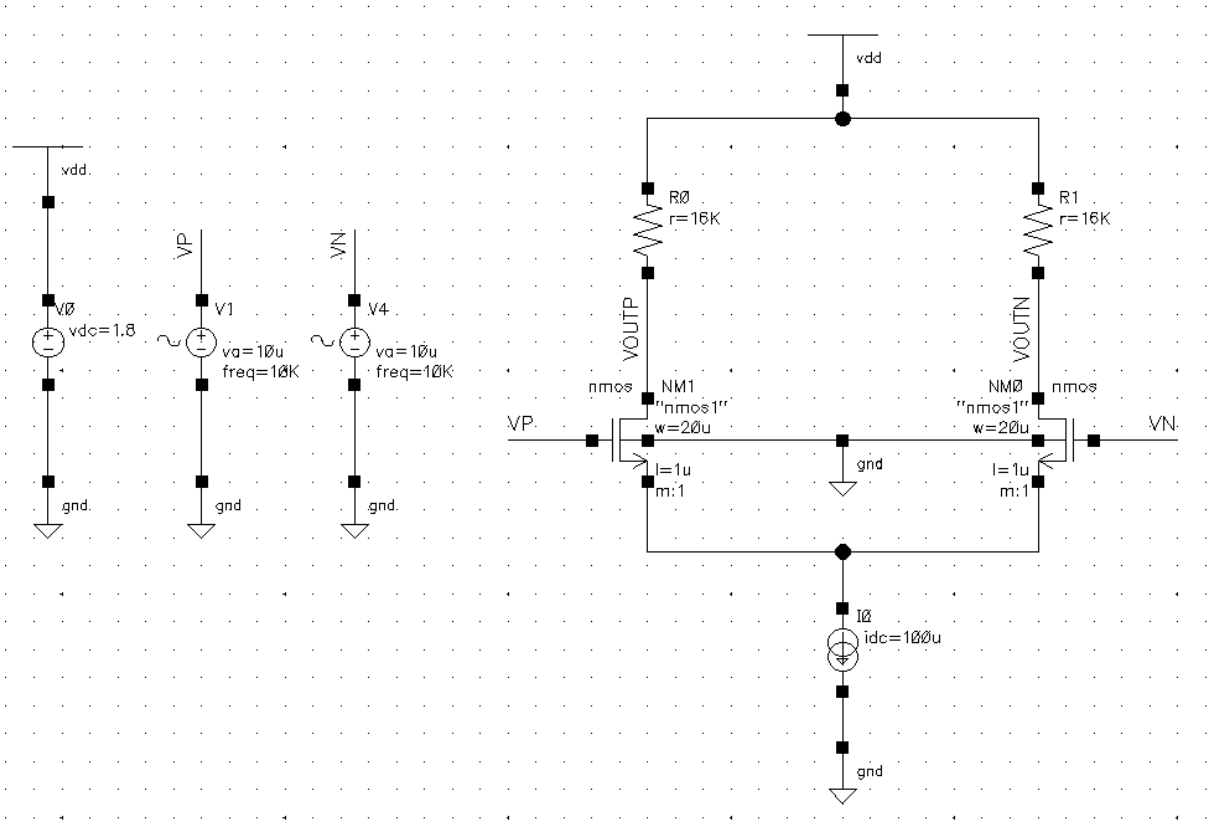
$$\mathbf{G_m} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$(625\mu)^2 = 200\mu\ (W/L)\ 100\mu$

W/L = 19.53125

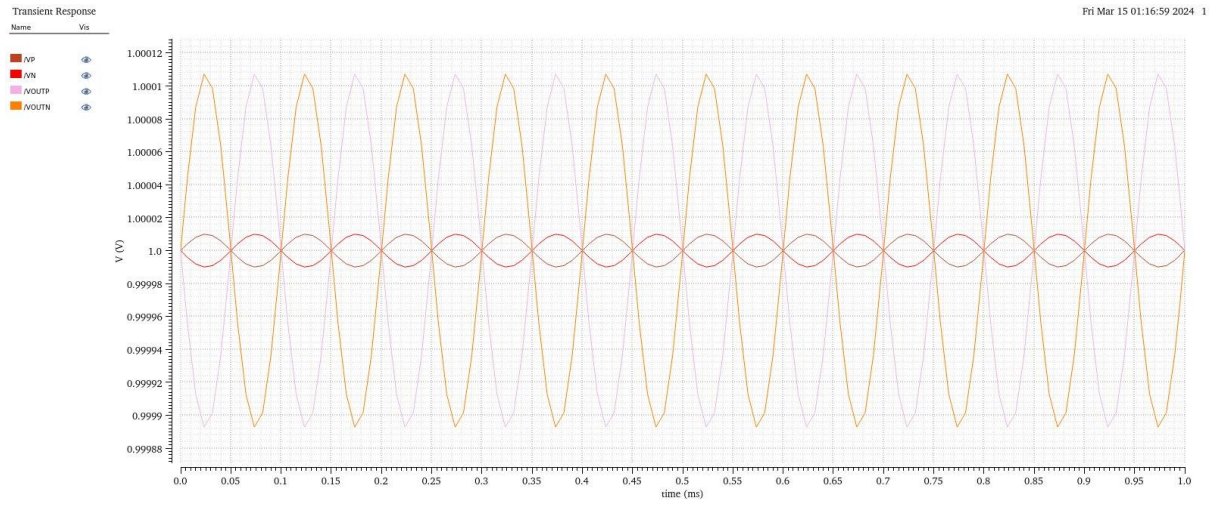
If L = 1 µ

W = 19.53125µ = **20 µ**




Run DC analysis and verify the DC operating points.

Run Transient Analysis and calculate the gain.



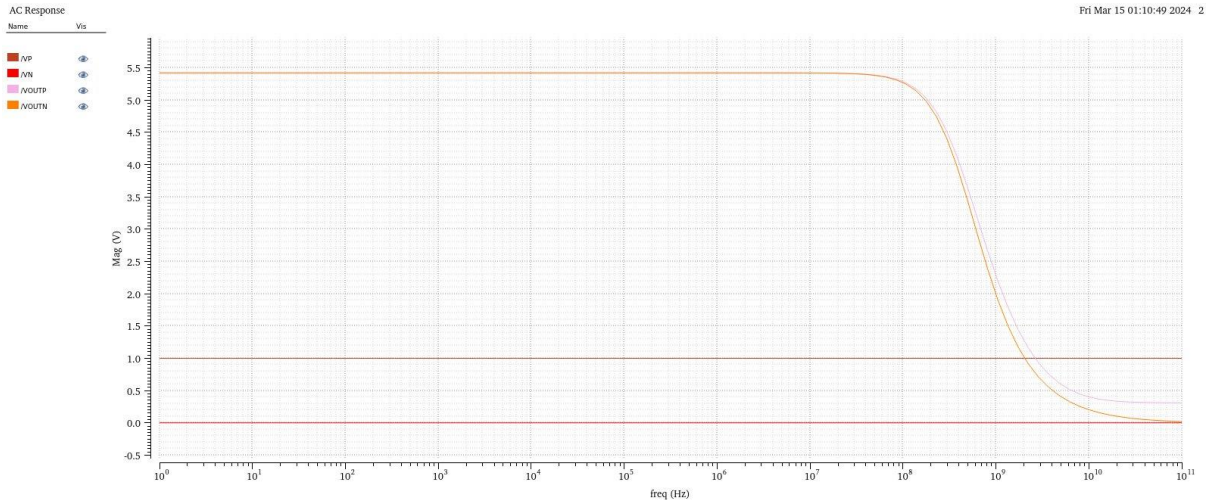

VP = 20uV peak to peak

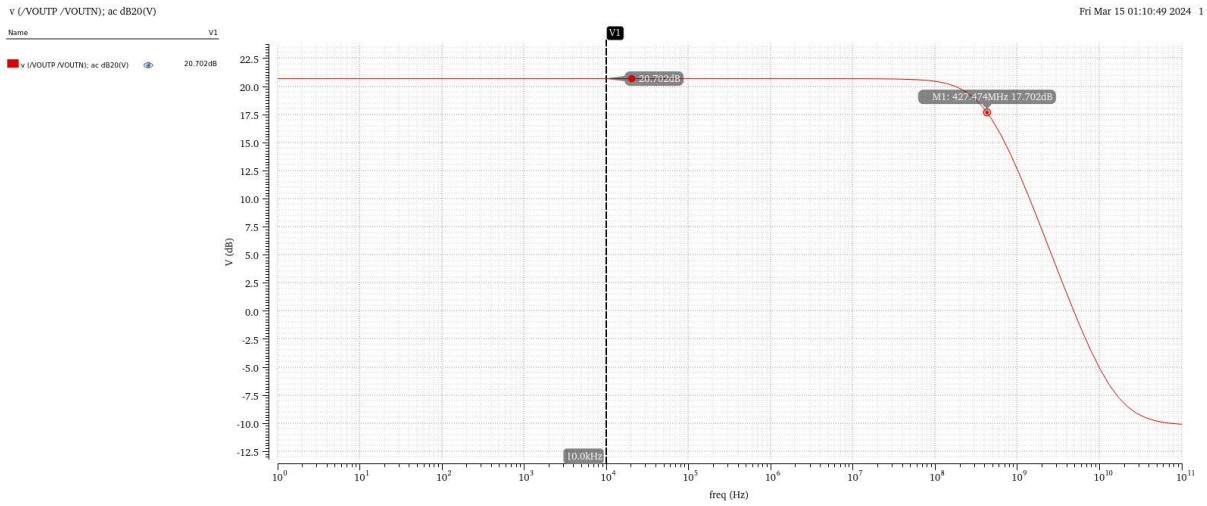
VN = 20uV peak to peak

VOUTP = 214uV peak to peak

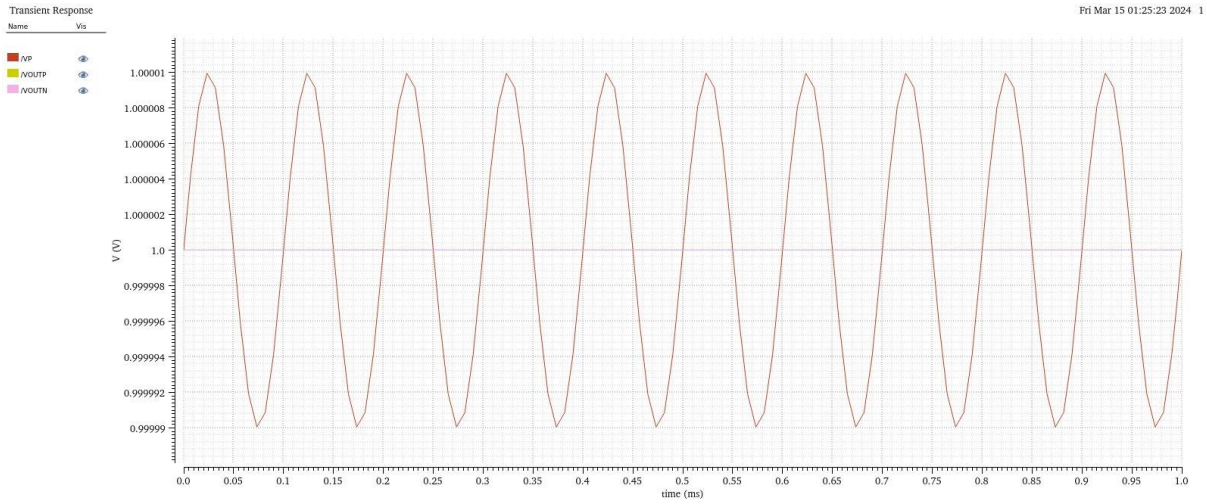
Differential Gain = 10.7 v/v = **20.58 dB**

Run AC analysis and plot gain.




Apply Common mode input voltage and run transient analysis.

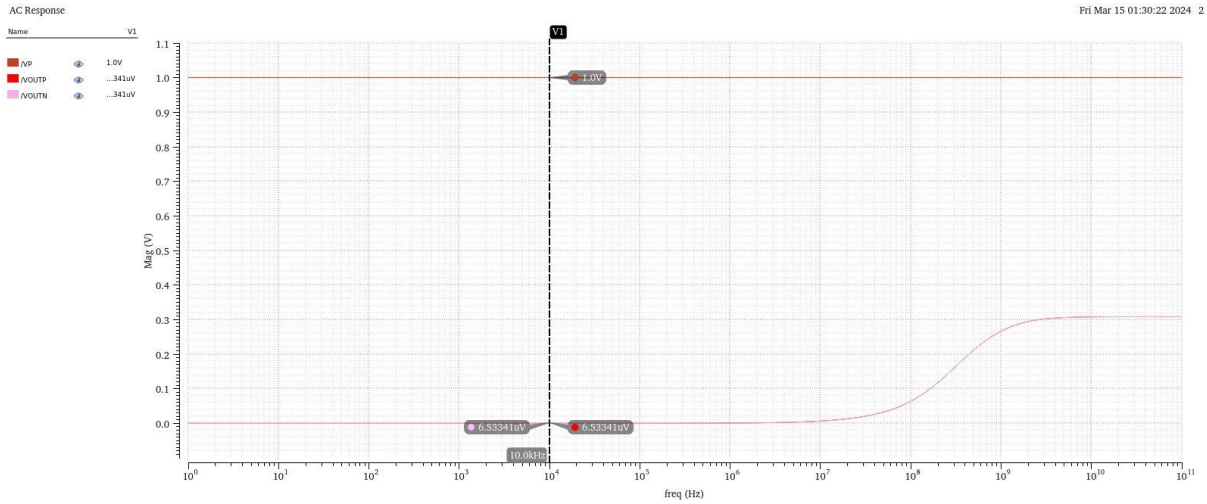


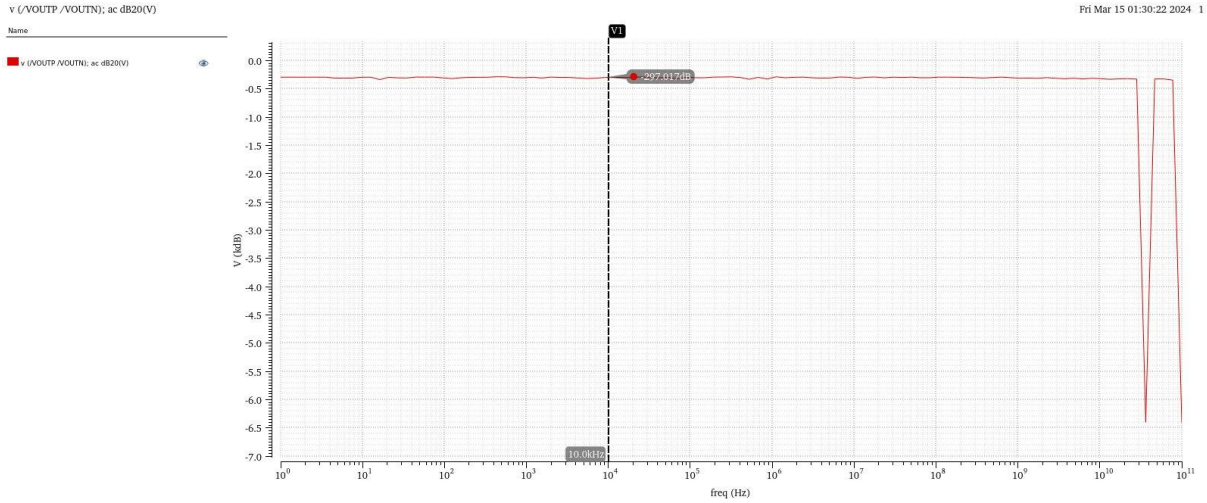

VP = VN = 20uV peak to peak

VOUTP = 3nV peak to peak

Common Mode Gain = 0.00015 v/v = **-76.47 dB**

Apply Common mode input voltage and run AC analysis.




Observations:

| | Theoretical | Practical |
|---|---|---|
| gm | 625µ | 702.922µ |
| IDS | 50 µ | 50.0005 µ |
| Ad | 20 dB | 20.702 dB |
| Ac | 0 | -288.88 dB |
| CMRR | 60 dB | 317 dB |

# 3. Differential Amplifier with Active Load

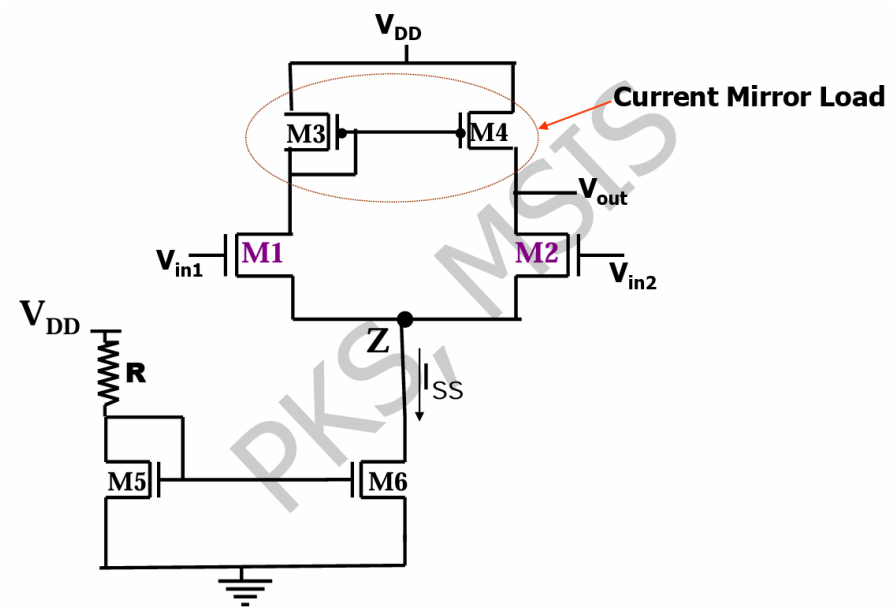
**Voltage Gain**

Av = 20 dB

$20 = 20 \log_{10} (Av)$

$Av = 10^{(20/20)}$

**Av = 10 V/V**




Let current ISS be 100µA. Let VGS = 0.6V

Calculate the value of R.

R = (VDD - VGS -VSS) / ISS

R = (1.8 – 0.6)/ 100µ

**R = 12K**

Calculate the W of the transistors M5 and M6.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Let L = 1µ

100µ = ½ (200µ) * (W/1µ) * (0.6 – 0.45)^2

W = 88.88µ

**W5 = W6 = 88µ**

Calculate the W of the transistors M3 and M4.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Let L = 1µ, Kp = 40µ

Current through each branch is ID = 50µA

50µ = ½ (40µ) * (W/1µ) * (0.8 – 0.45)^2

W = 20.04µ

**W3 = W4 = 20µ**

Calculate the W of the transistors M1 and M2.

$$A_v = \frac{2\sqrt{\beta}}{(\lambda_2+\lambda_4)\sqrt{I_{SS}}}$$

ISS = 100µ, Assume λ = 5m, Kn = 200µ

50 = (2 sqrt(0.5 * 200µ * (W/L))) / ((5m + 5m) * sqrt(100µ))

50 = (2 sqrt(0.5 * 200µ * (W/L))) / 100µ

25 * 100µ = sqrt(0.5 * 200µ * (W/L))

$(2.5m)^2$ = 100µ * (W/L)

W/L = 0.0625

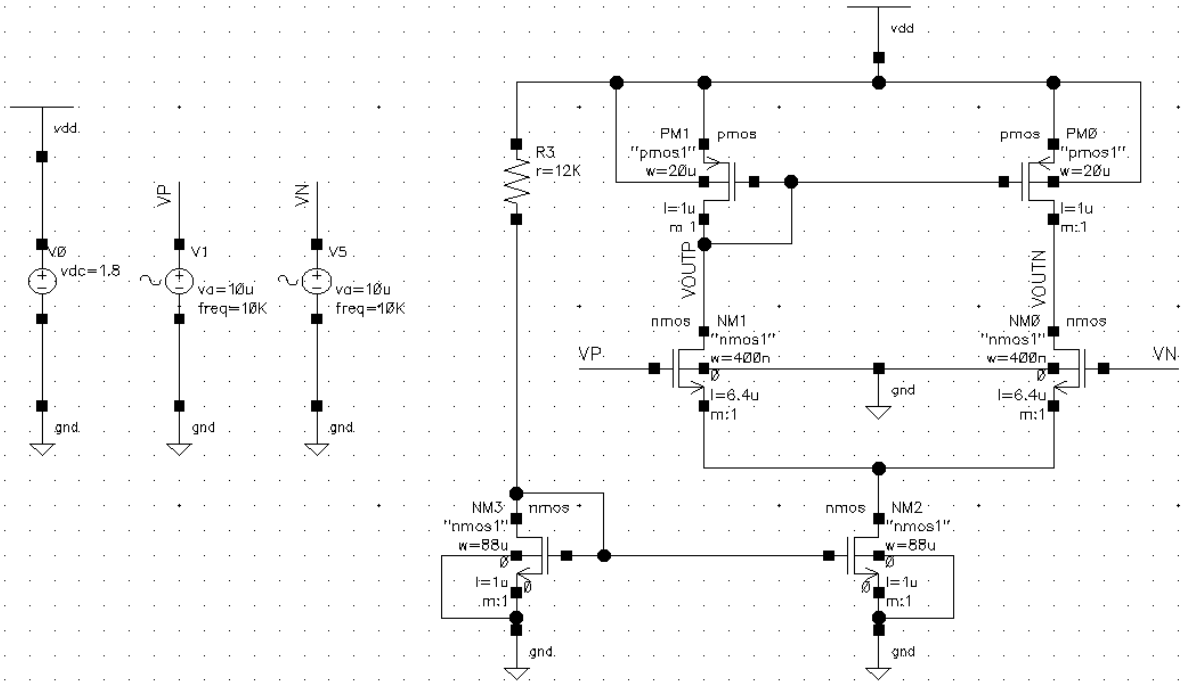
Minimum Possible W = 400n, Minimum Possible L = 180n

If W = 400n

L = 6.4µ

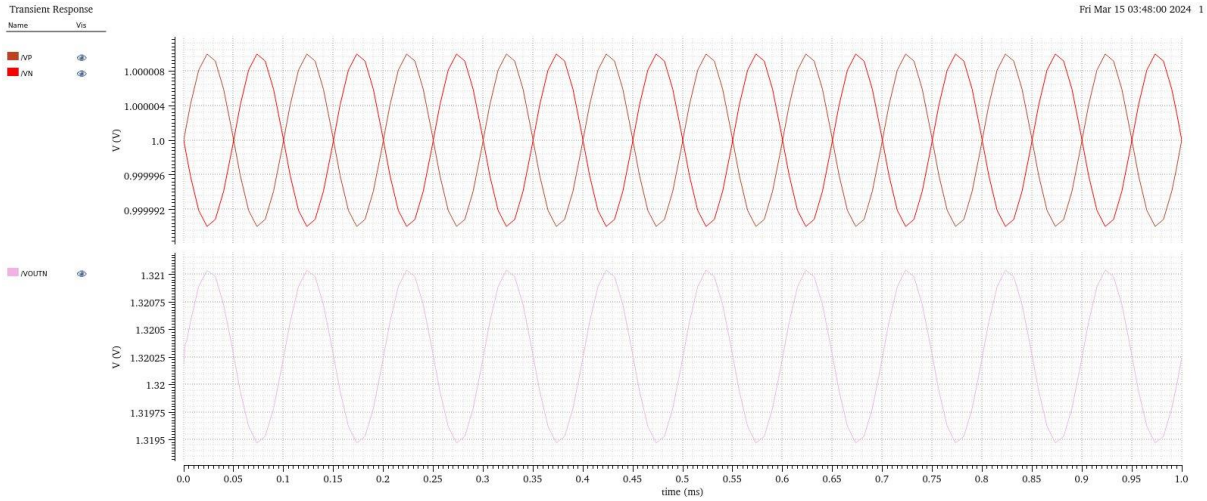
**L1 = L2 = 6.4µ**

**W1 = W2 = 400n**




Run DC analysis and verify the DC operating points.

Run Transient Analysis and calculate the gain.



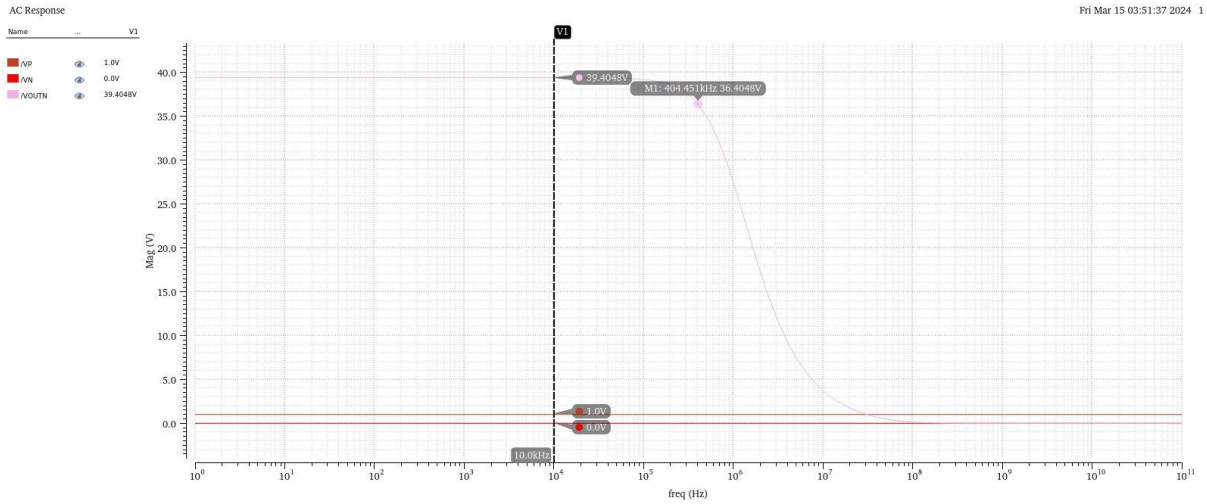

VP = 20uV peak to peak

VN = 20uV peak to peak

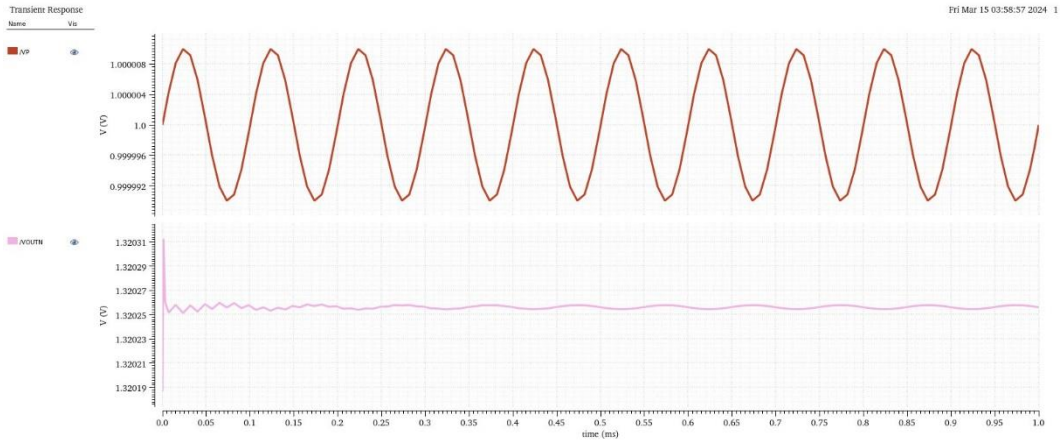
VOUTP = 1.571mV peak to peak

Differential Gain = 78.55 v/v = **37.9 dB**

Run AC analysis and plot gain.




Apply Common mode input voltage and run transient analysis.

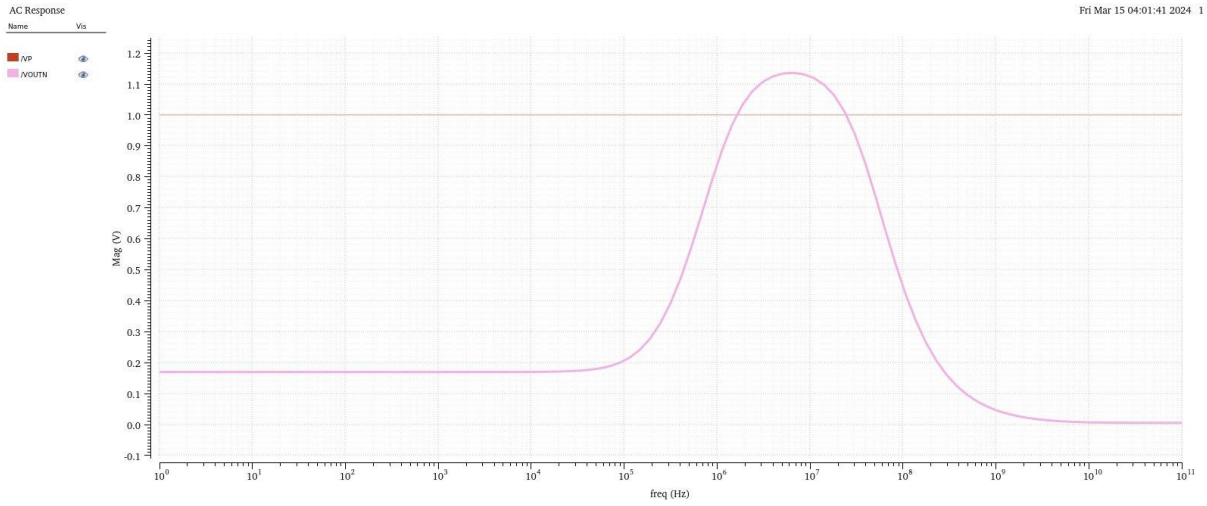


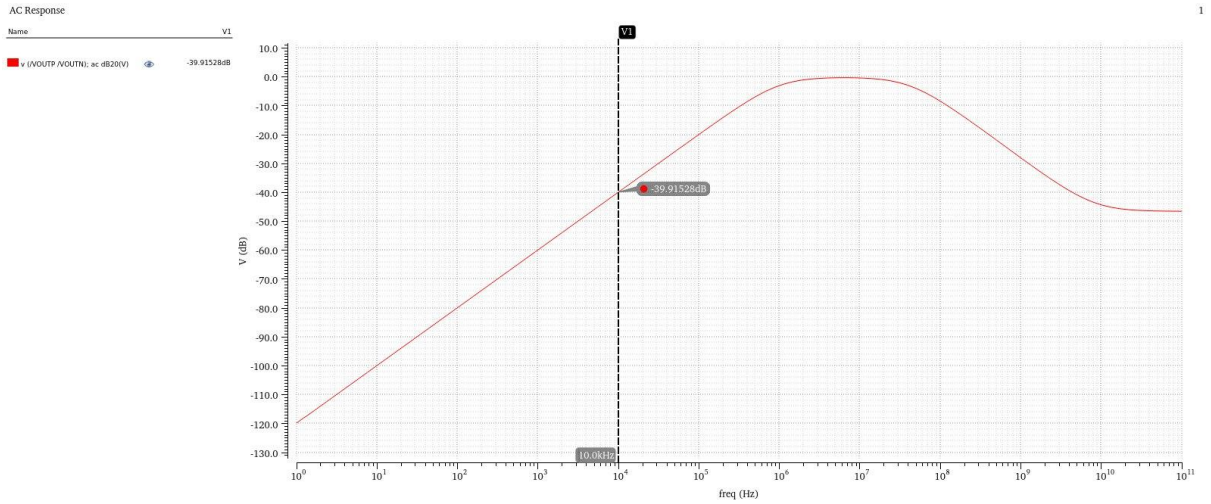

VP = VN = 20uV peak to peak

VOUTP = 125.6V peak to peak

Common Mode Gain = 6.28 v/v = **15.95 dB**

Apply Common mode input voltage and run AC analysis.






Observations:

| | Theoretical | Practical |
|---|---|---|
| Ad | 50 dB | 39.40 dB |
| Ac | 0 | -39.91 dB |
| CMRR | 60 dB | 79 dB |

Due to assumptions in theoretical calculations the practical gain is slight lower than the calculated gain, but this can be easily increased by increasing width of M1 and M2.

In Active Load configuration very, high gain can be achieved easily using single stage amplifier.