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1. Finding MOSFET Parameters

1.1. Finding Kn of NMOS

Objective: Bias the NMOS transistor in the saturation region and note down DC Operating conditions and estimate the value of Kn.

We know that for a transistor operating in a saturation region.

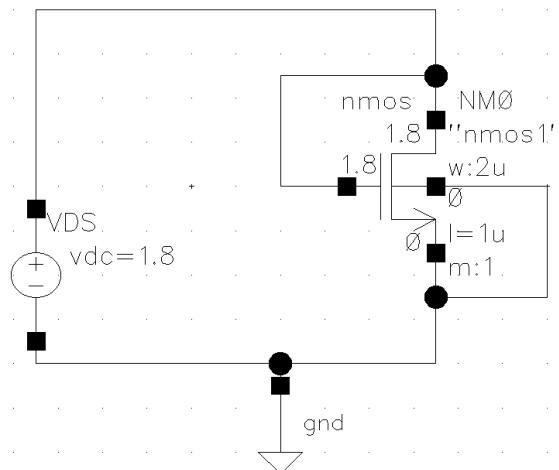
$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Then Kn can be calculated as

$$K_n = 2 I_{DS} / (W/L) (V_{GS} - V_{TH})^2$$

Keep the Transistor length sufficiently large to reduce the variation in IDS due to channel length modulation.

Short the gate and drain so that the transistor is in saturation.



Run DC Analysis

Results -> Print -> DC Operating Points -> In Schematic Select NMOS

From the DC Operating Points make sure transistor is in region 2 i.e. saturation

Note the values of IDS, and VTH

W/L	IDS	VTH	Kn	λ
400n/180n	279.249u	482.033m	144.68u	18.65u
2u/1u	338.293u	485.204m	195.69u	7.22m
4u/2u	409.908u	460.297m	228.385u	4.44m
8u/4u	426.516u	444.263m	232.05u	3.33m

Analyse the results for minimum feature size

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Then Kn can be calculated as

$$K_n = 2 IDS / (W/L) (V_{GS} - V_{TH})^2$$

$$Kn = 144.68u$$

Which is almost half of beta effective

~~beff~~ 321.552u

$$1 + \lambda * VDS = IDS / ((Kn/2)*(W/L)*(VGS-VTH)^2)$$

$$1 + \lambda * VDS = 1.000033587$$

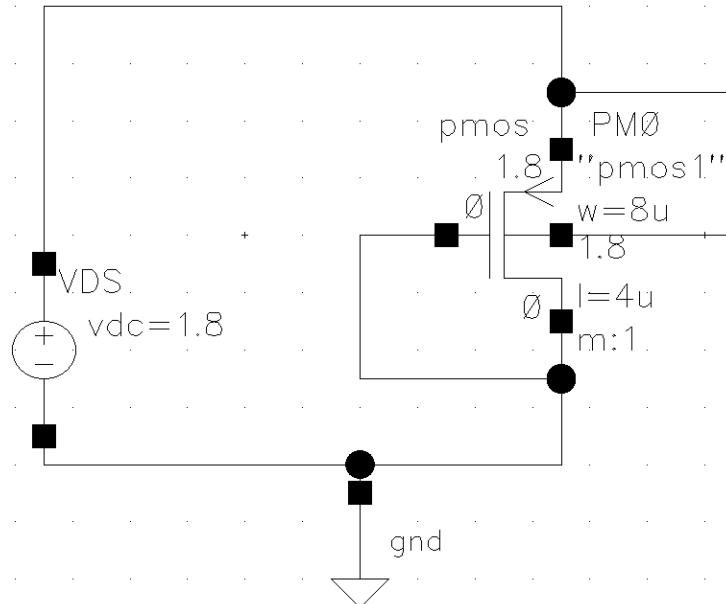
$$\lambda * VDS = .000033587$$

$$\lambda = 18.65u$$

Then rds = 192M

1.2. Finding Kp of PMOS

Similarly Find the Value of Kp for PMOS.



W/L	IDS	VTH	Kp	λ
2u/1u	-71.655u	-456.541m	39.70u	9.15u
4u/2u	-73.8131u	-438.306m	39.80u	116u
8u/4u	-76.519u	-428.553m	40.68u	

2. Simple Current Mirror

2.1. Simple Current Sink

Objective: Design a simple current sink to sink a current of 10uA. VDD = 1.8V, VSS = 0V, L = 2u, VGS = 0.6V, VTH = 0.45V, Kn = 200u, λ = 7m.

$$I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{REF}$$

Calculate the value of R.

$$R = (VDD - VGS - VSS) / Iref = 120K$$

Calculate the W of the transistors.

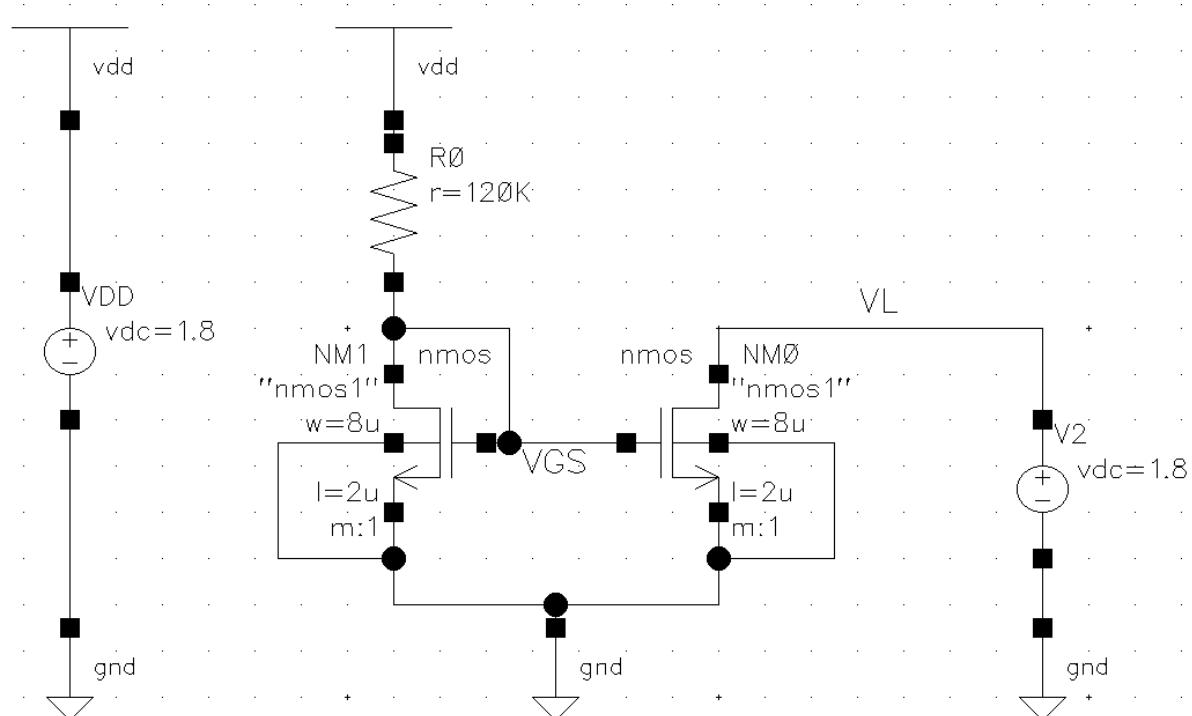
$$10u = \frac{1}{2} (200u) * (W/2u) * (VGS - VTH)^2 = 8.88u = 8u.$$

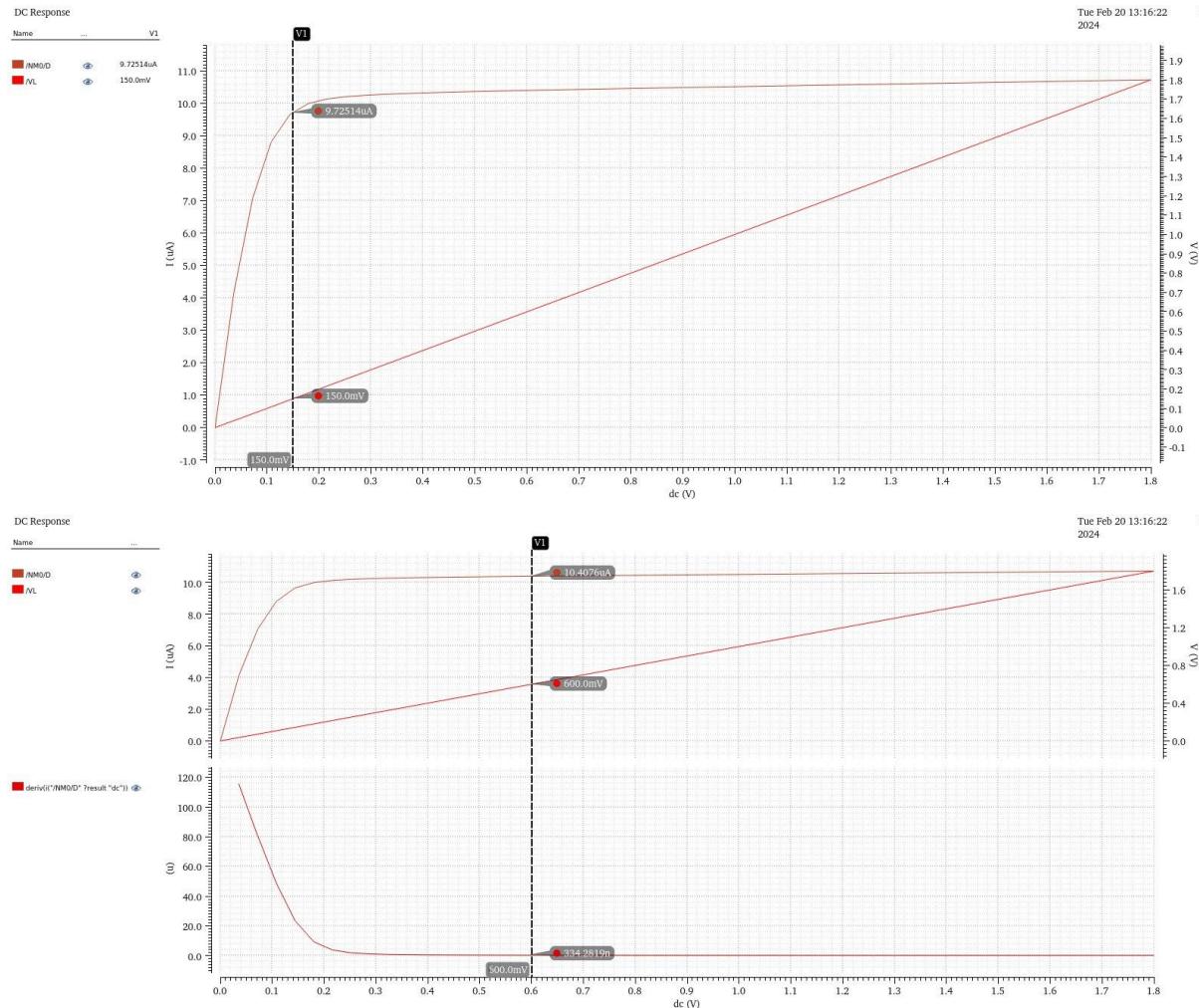
If we set $W = 6u$ then actual current will be.

$$I = \frac{1}{2} (200u) * (8u/2u) (0.6 - 0.45)^2 = 9u A.$$

$$\Delta V = V_{GS} - V_{TH} = 0.6 - 0.45 = 0.15$$

$$r_0 = 1/\lambda l_0 = 14.28M$$





The slope of this curve gives go $1/g_o$ is r_o
 $r_o = 2.99M$, it will increase when moved further

2.2. Simple Current Source

Objective: Design a simple current source to source a current of 10uA. VDD = 1.8V, VSS = 0V, L = 2u, VGS = 0.6V, VTH = 0.45V, Kp = 40u.

Calculate the value of R.

$$R = (VDD - VGS - VSS) / I_{ref} = 120K$$

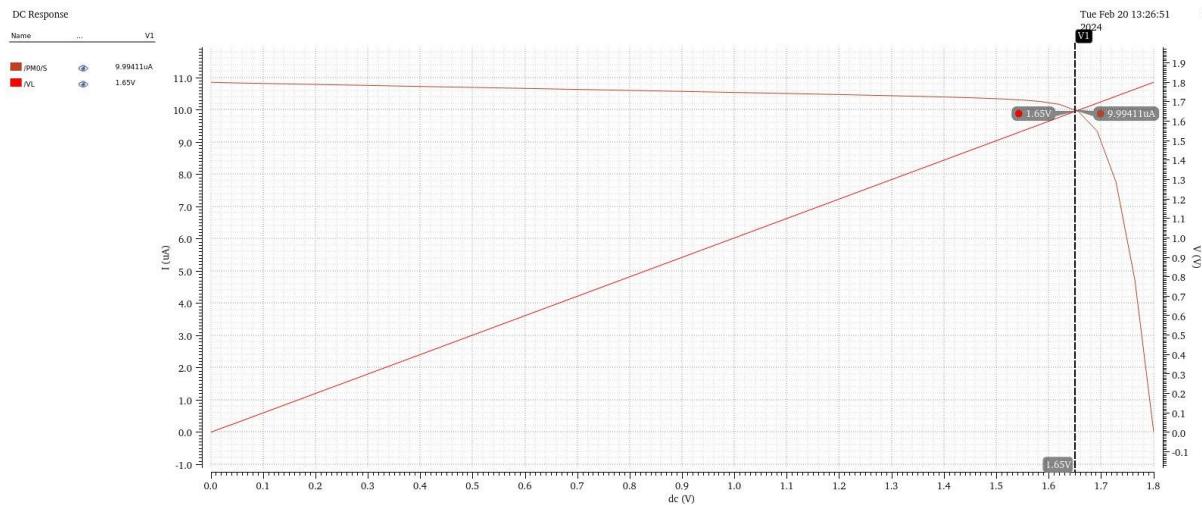
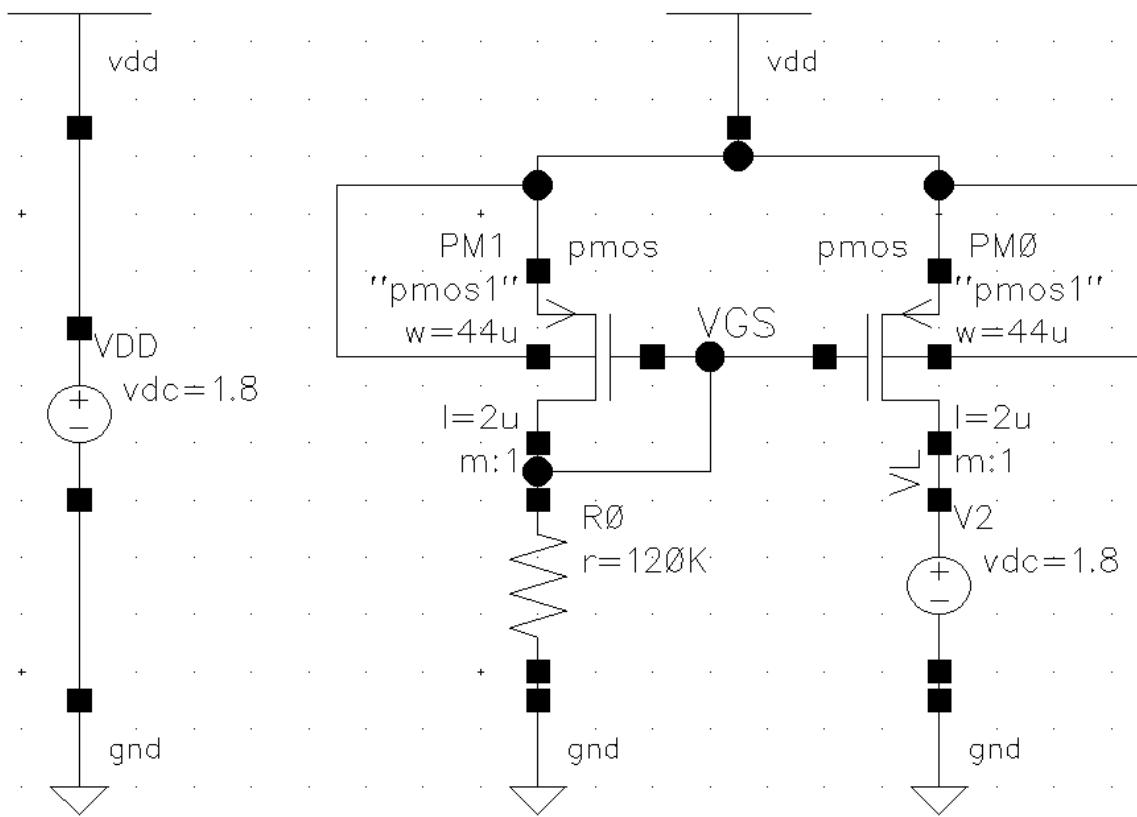
Calculate the W of the transistors.

$$10u = \frac{1}{2} (40u) * (W/2u) * (VGS - VTH)^2 = 44.44u = 44u$$

If we set W = 44u then actual current will be.

$$I = \frac{1}{2} (40u) * (44u/2u) (0.6 - 0.45)^2 = 9.9u A$$

$$\Delta V = VGS - VTH = 0.6 - 0.45 = 0.15$$



2.3. Simple Current Mirror with multiple output currents

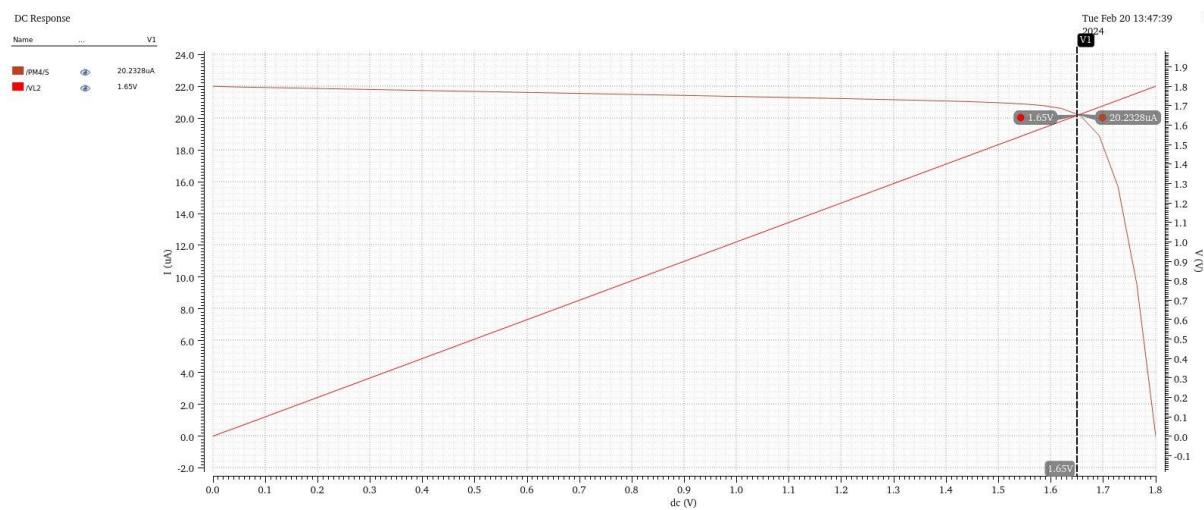
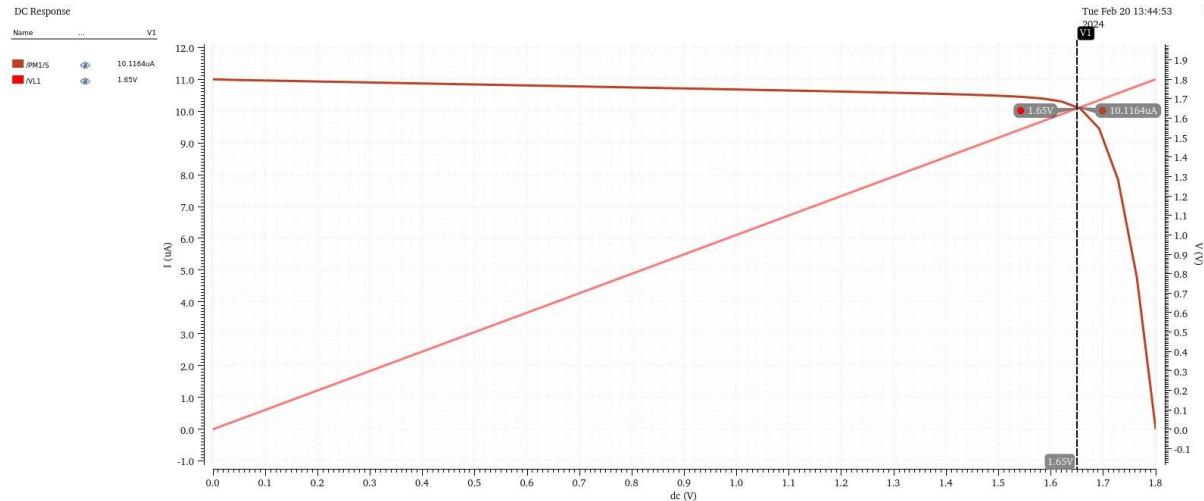
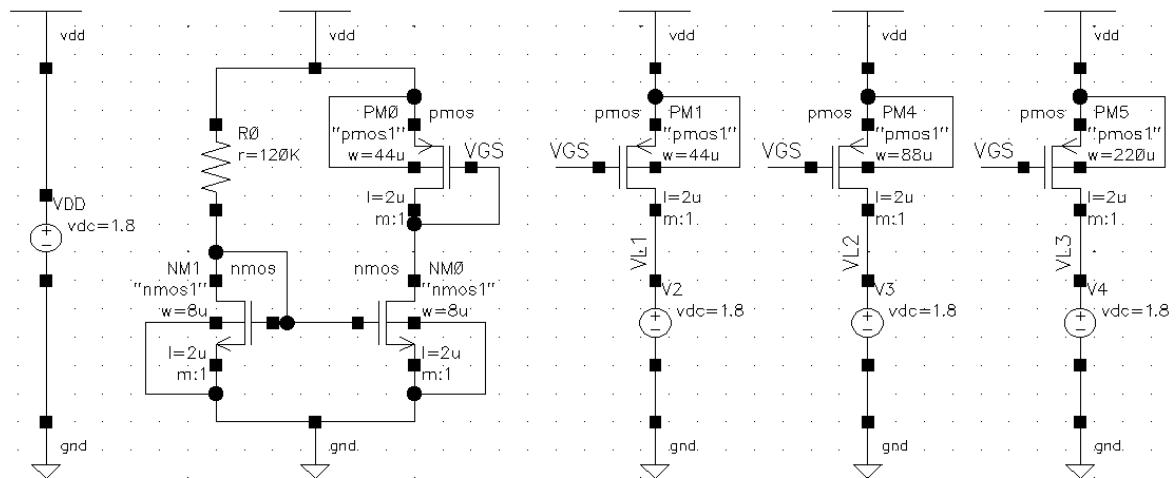
Objective Design Simple Current Source From above designed current sink with output currents output currents of 10u, 20u and 50u.

For 10uA width of pmos is 44u

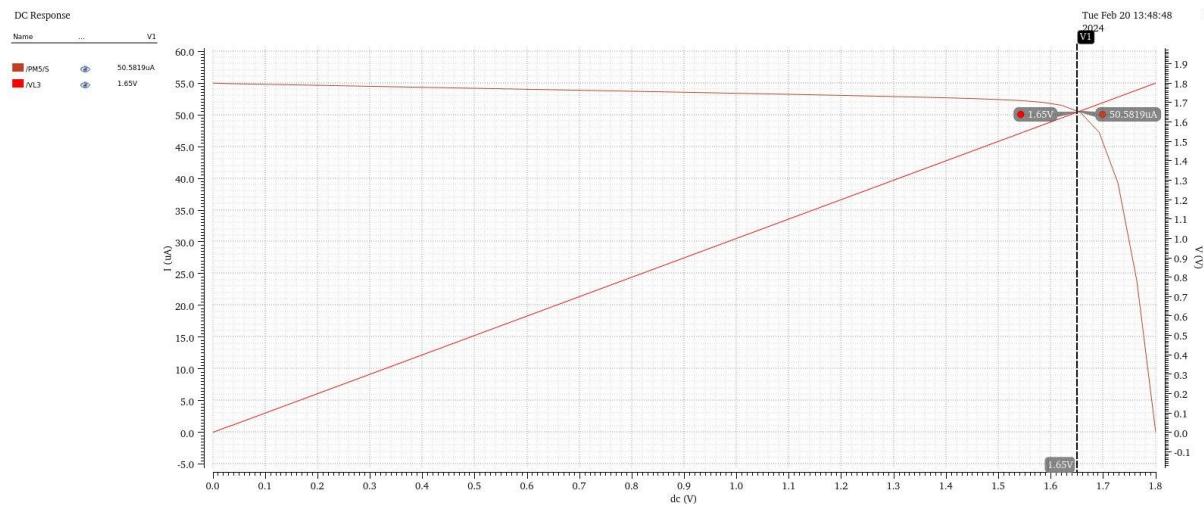
For 20uA width of pmos is 88u

For 50uA width of pmos is 220u

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3. Cascode Current Mirror

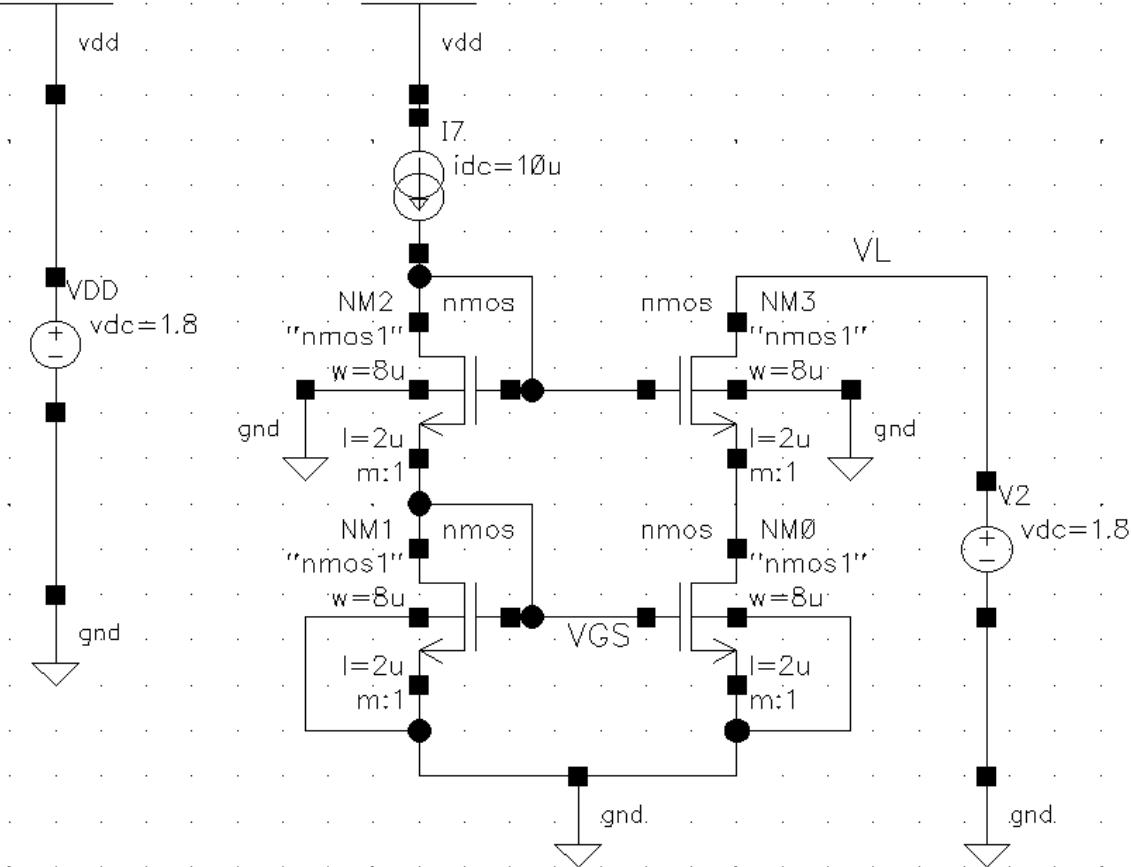
3.1. 2 Stage Cascode Current Mirror

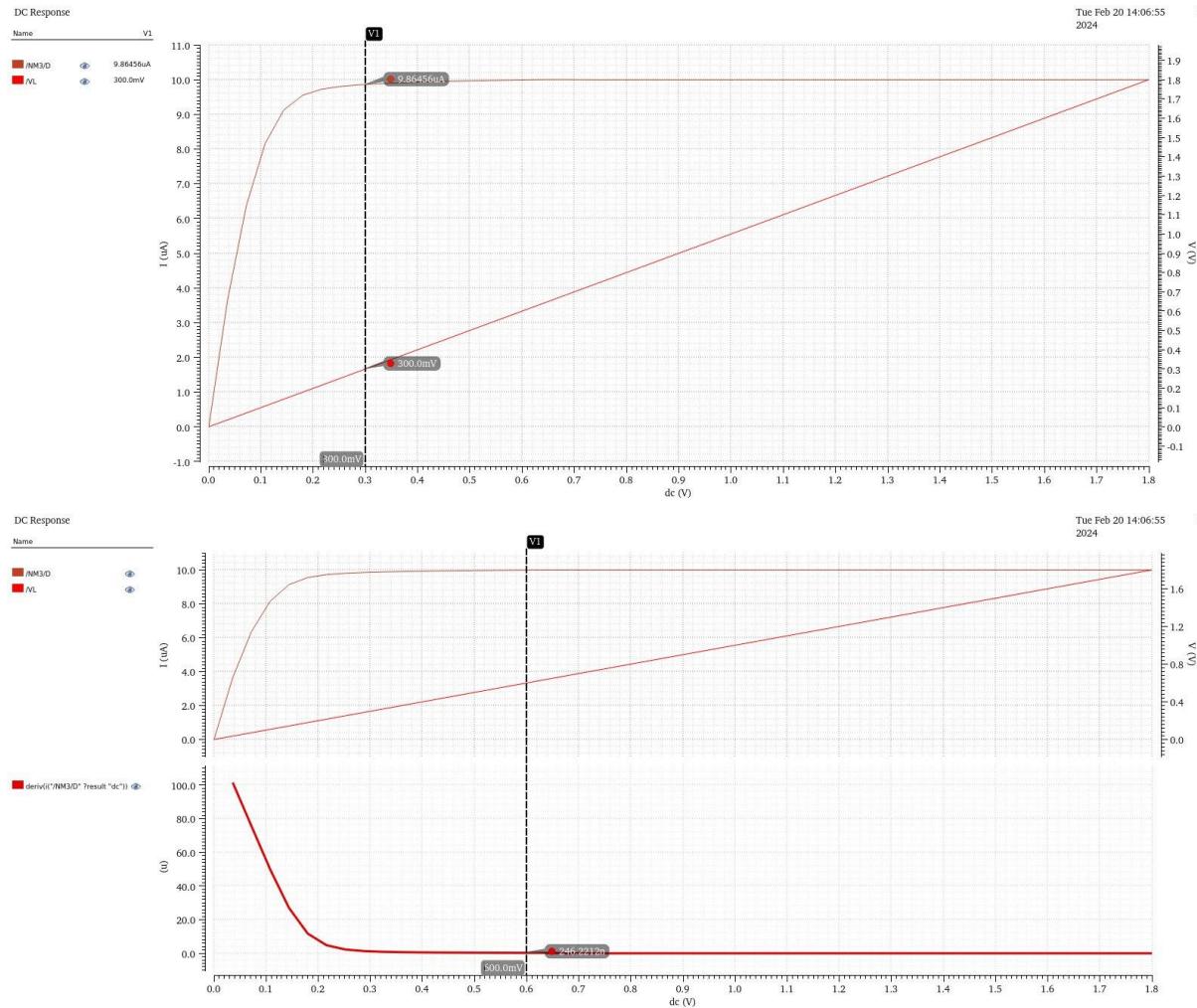
Objective: Design a two stage current sink to sink a current of 10uA. VDD = 1.8V, VSS = 0V, L = 2u, VGS = 0.6V, VTH = 0.45V, Kn = 200u.

Calculate the W of the transistors.

$$10u = \frac{1}{2} (200u) * (W/2u) * (VGS - VTH)^2 = 8.88u = 8u.$$

$$r_o = g_m \cdot (r_o^2) = 200u \cdot (14M * 14M) = 39G$$

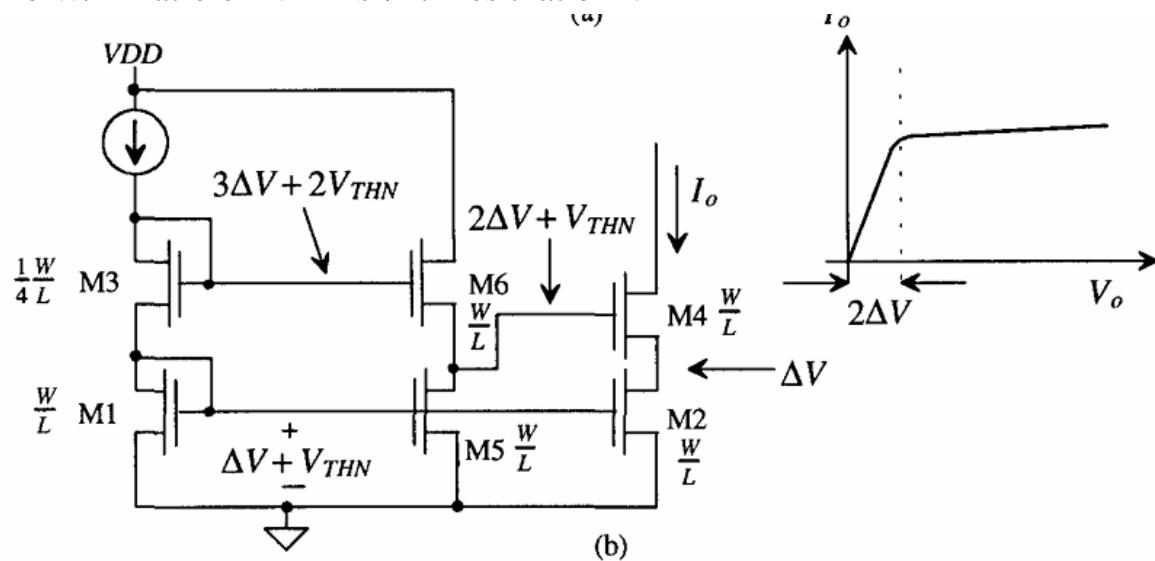




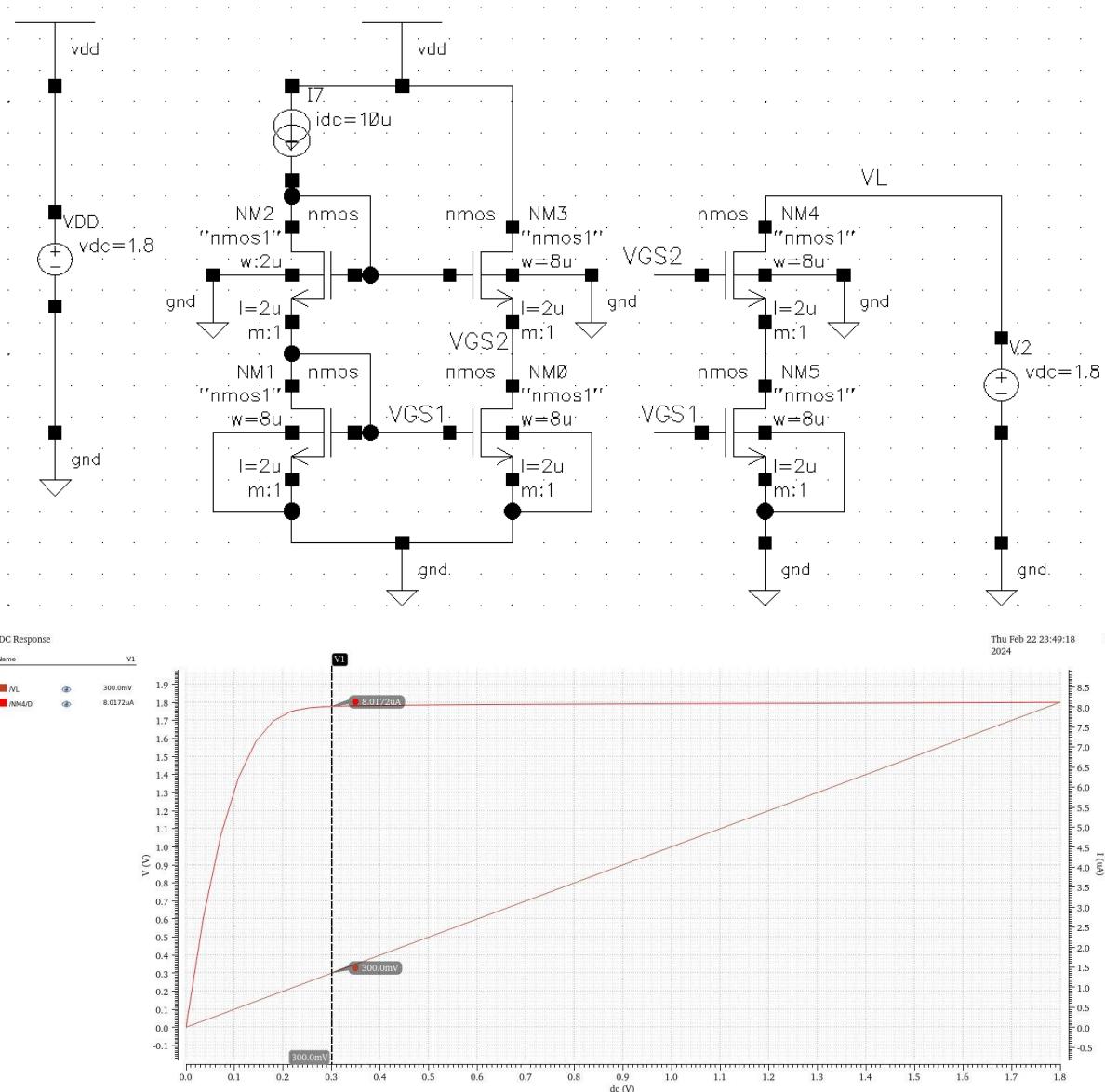
$r_o = 4.06M$, it will increase to G as moved further

3.2. 2 stage cascode current mirror with lower minimum voltage

The W/L Ratio of NM2 is $\frac{1}{4}$ times that of NM1



The current is reduced and needs to be fixed. There is no improvement observed in swing.



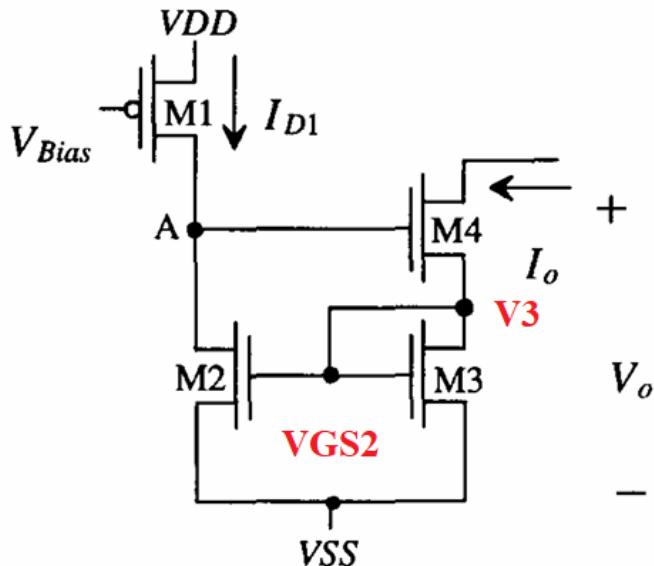
4. Wilson Current Mirror

Uses negative feedback.

Constant current IREF flows through M2.

If VO increases this causes an increase in IO, hence V3 increases.

This causes an increase in VGS3. But as IREF is constant VDS3 reduces this in turn reduces gate voltage of M4. Hence the current IO decreases.



$$\frac{I_{OUT}}{I_{REF}} = \frac{\left(\frac{W}{L}\right)_2 (1 + \lambda V_Y)}{\left(\frac{W}{L}\right)_1 (1 + \lambda V_X)}$$

$$V_o(\min) = \sqrt{\frac{2I_o}{\beta_3}} + V_{THN3} + \sqrt{\frac{2I_o}{\beta_4}} = 2\sqrt{\frac{2I_o}{\beta_{3,4}}} + V_{THN3}$$

Let IREF = 10uA, design a wilson current mirror, with IO = 50uA.

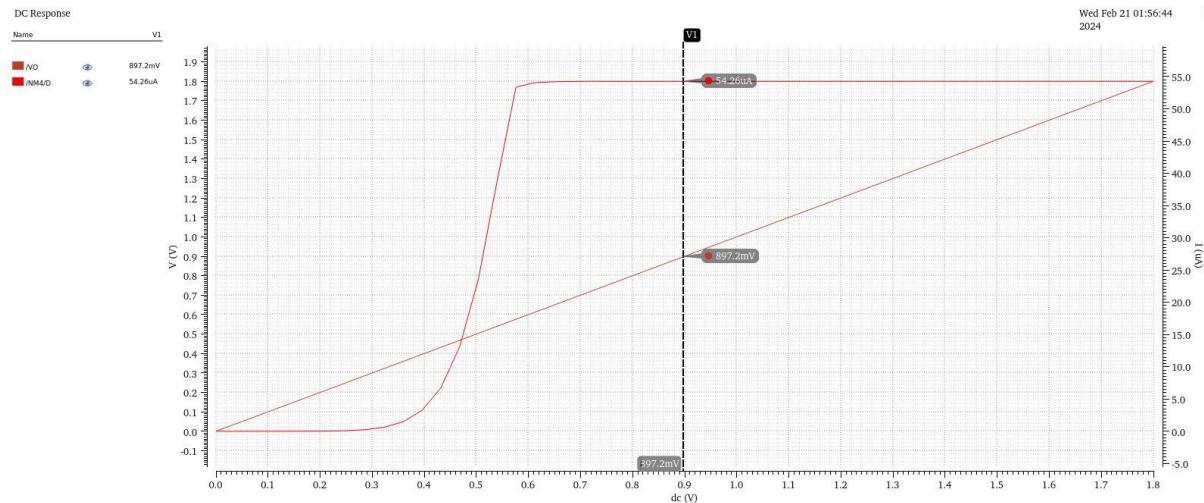
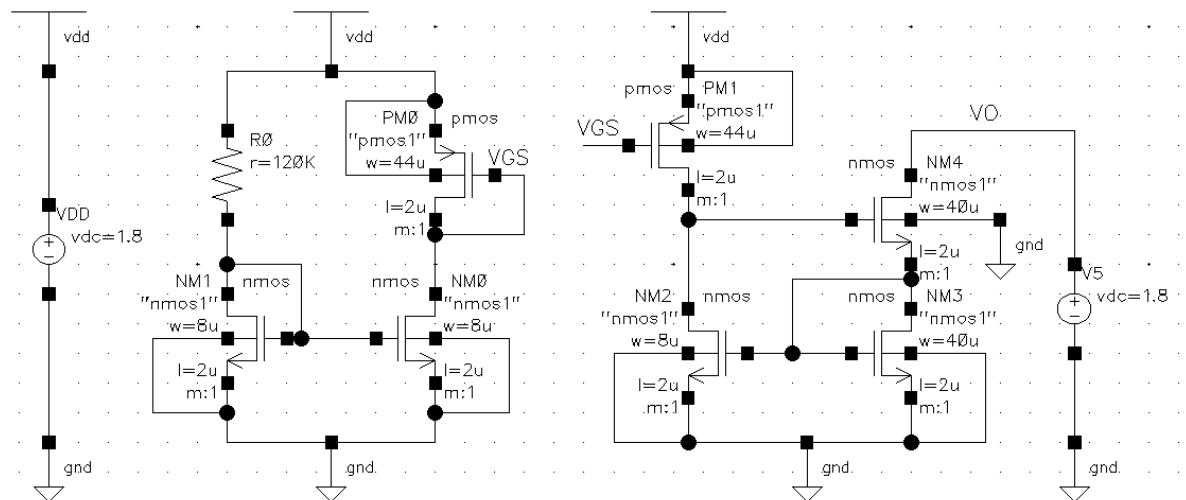
Design a current source to deliver 10uA (Previous Problem)

Let W2 = 8u, L2 = 2u (From Previous problem)

W3 = 5 * W2 = 40u

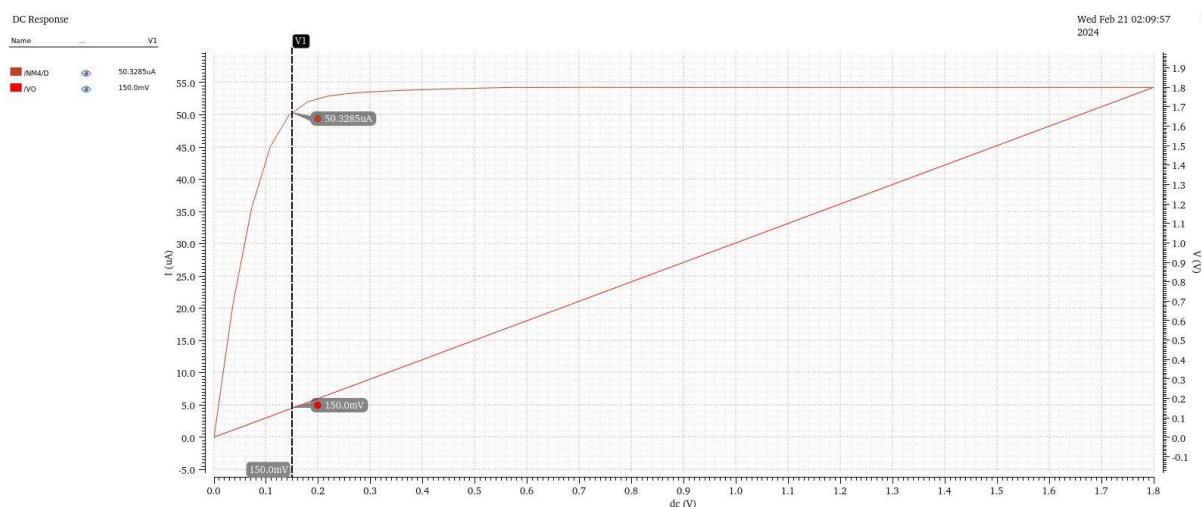
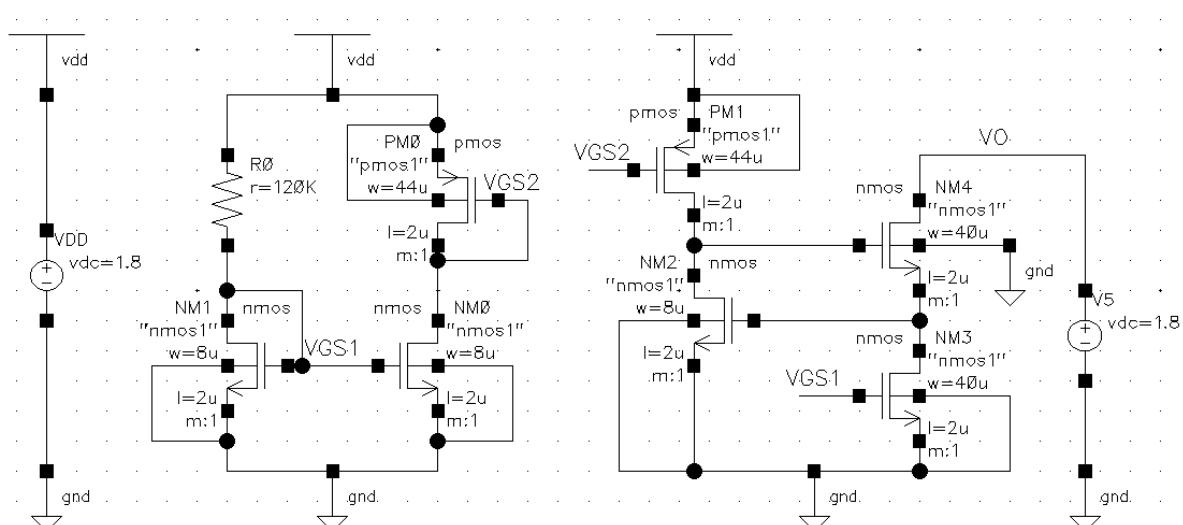
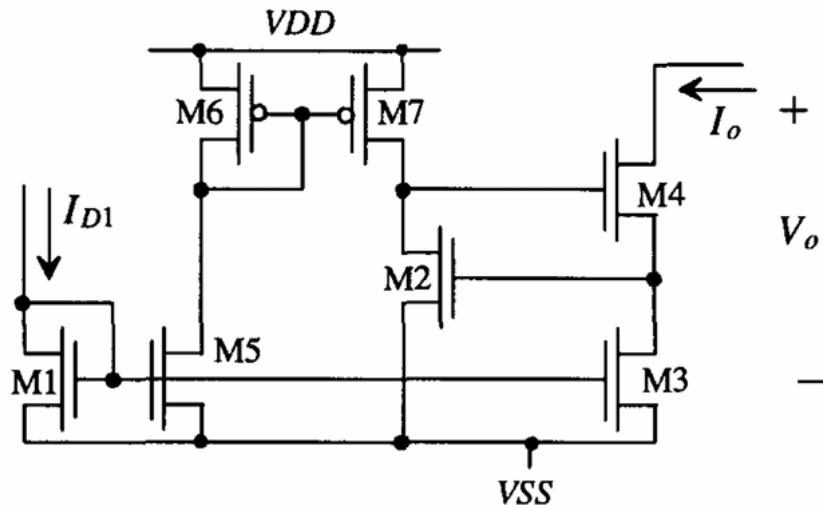
$$V_o \min = 2 * (\sqrt{2 * 50u / 2m}) + V_{TH3} = 0.8972$$

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5. Regulated Cascode Current Mirror

Using IREF 10uA, generate IO of 50uA using a regulated current mirror.



6. Simple Voltage References

6.1. Resistor MOSFET Voltage Reference

Design a Resistor MOSFET Voltage Reference with reference voltage 1V.

$$V_{REF} = VTN + \sqrt{2(VDD - VREF) / R \beta}$$

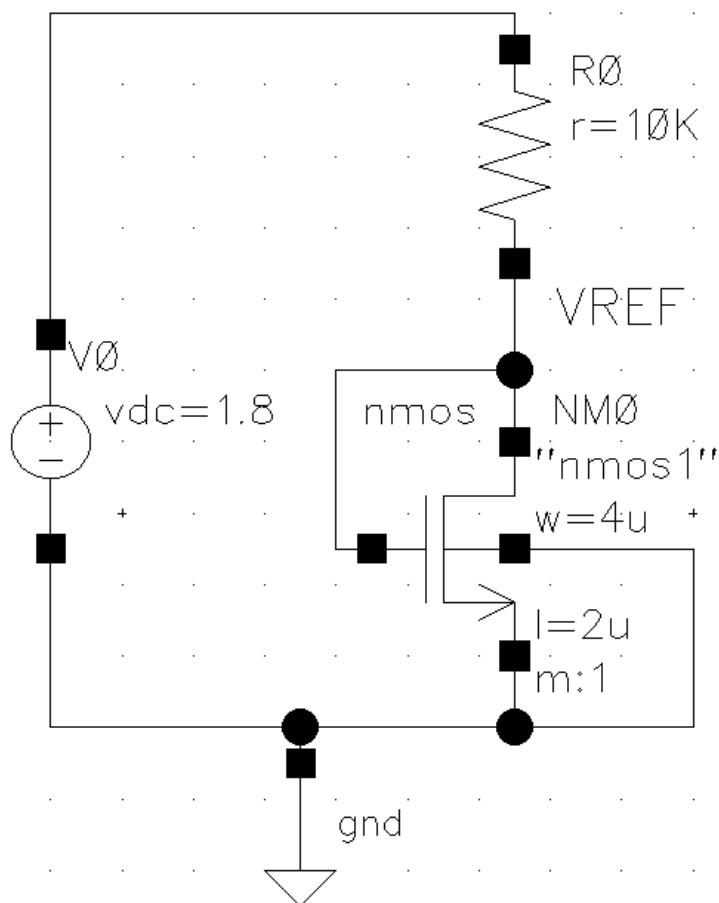
Let L = 2u and W = 4u and Kn = 200u

$\beta = \frac{1}{2} K_n (W/L) = 200u$

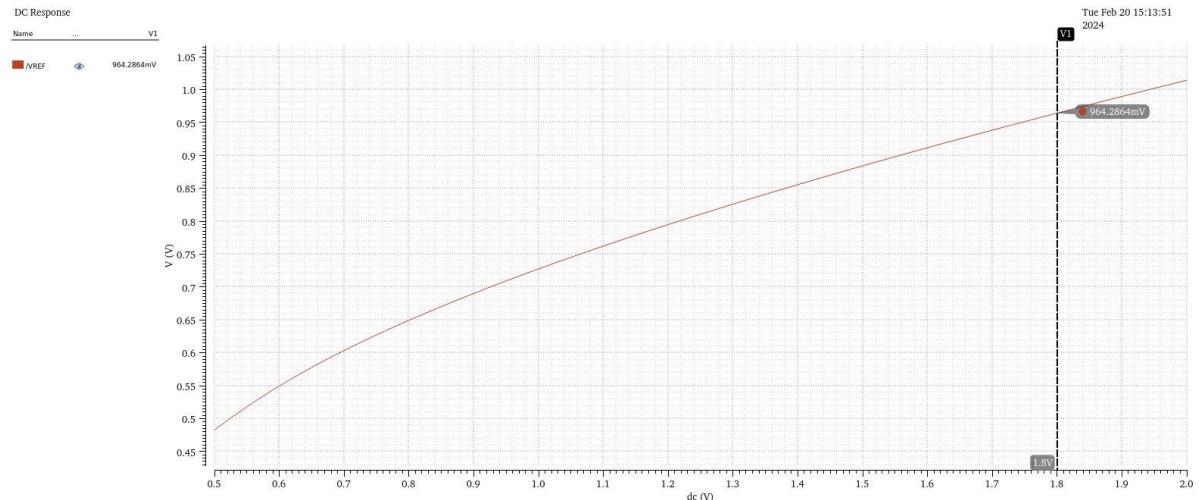
$$1 = 0.45 + \sqrt{2(1.8 - 1) / R 200u} = 10.031K = 10K$$

Actual Theoretical VREF for 10K Resistor

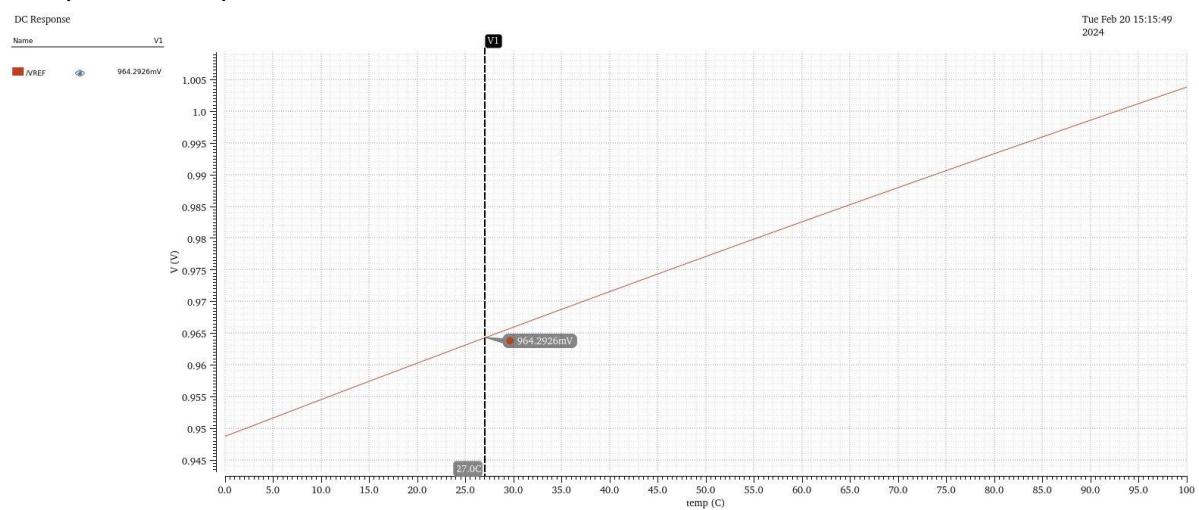
$$V_{REF} = 1.34$$



Voltage Dependence



Temperature Dependence



6.2. MOSFET Only Voltage Reference

Objective: Design 1V MOSFET only voltage reference. Determine the temperature coefficient of the resistance.

$VDD = 1.8V$, $LP = LN = 2\mu$, $Vtp = Vtn = 0.45$, $Kn = 200\mu$, $Kp = 40\mu$

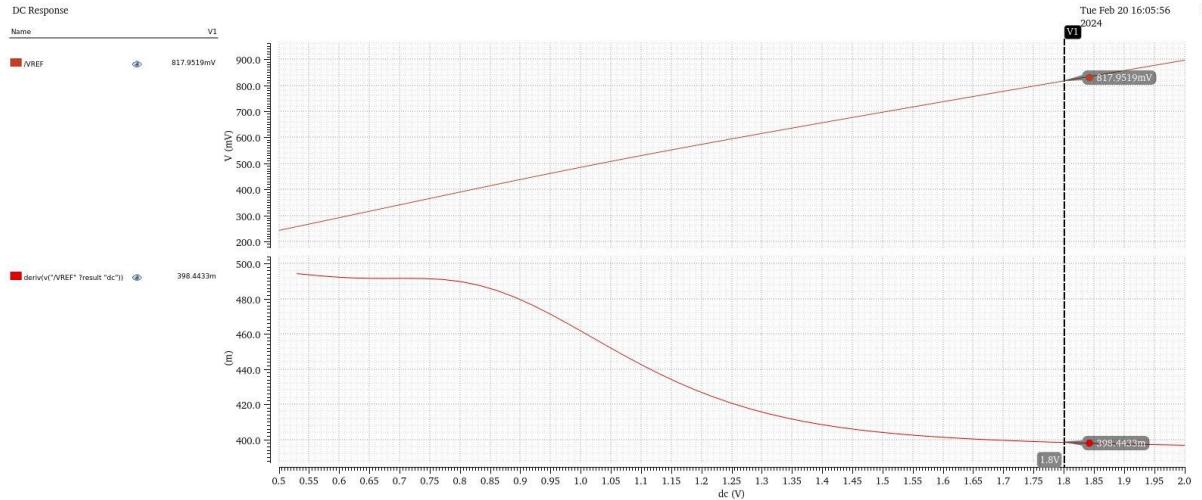
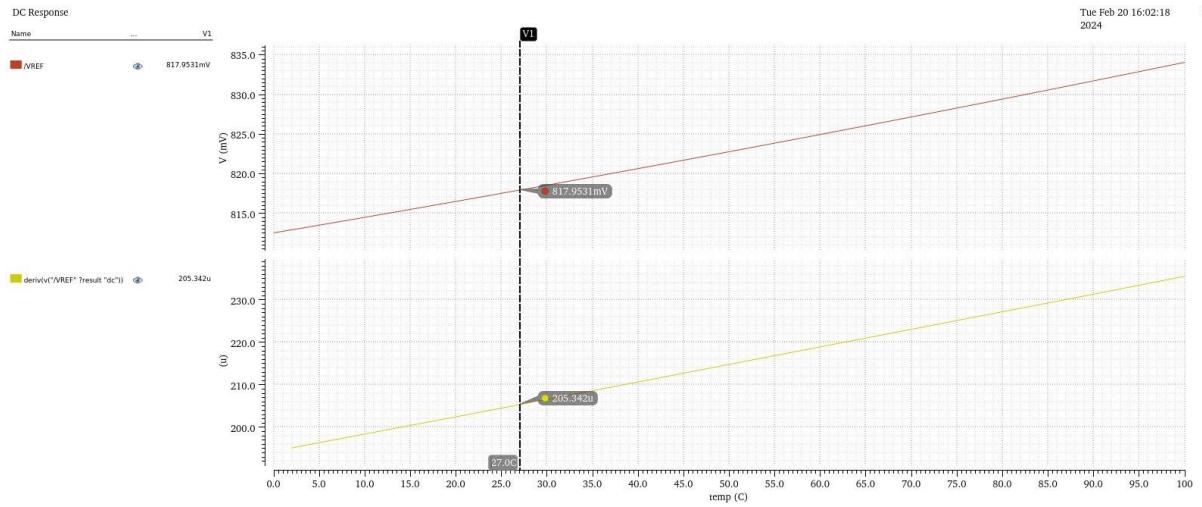
$$\begin{aligned}\beta_p/\beta_n &= [(VDD - VREF - VTP) / (VREF - VSS - VTN)]^2 \\ &= 0.6363\end{aligned}$$

$$\beta_p/\beta_n = (\frac{1}{2} K_p (W_p/L_p)) / (\frac{1}{2} K_n (W_n/L_n))$$

Let $L_p = L_n = W_n$

Then $W_p = 6.3636\mu = 6\mu$

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398.87mV change in VREF per 1V change in VDD

7. Threshold Voltage Referenced Self Bias

Objective: Design a threshold voltage referenced self biasing current source with IREF = 10uA.

$$IR = V_{GS1} = V_{THN} + \sqrt{\frac{2I}{\beta_1}} \quad (21.16)$$

If β_1 is large, the current, I , is given by

$$I \approx \frac{V_{THN}}{R} \quad (21.17)$$

In practice, the second term in Eq. (21.16) is not negligible, and the current is given by

$$I = \frac{V_{GS1}}{R} \quad (21.18)$$

$$I_{REF} = V_{th} / R$$

$$R = V_{th} / I_{REF} = 0.45 / 10u = 45K$$

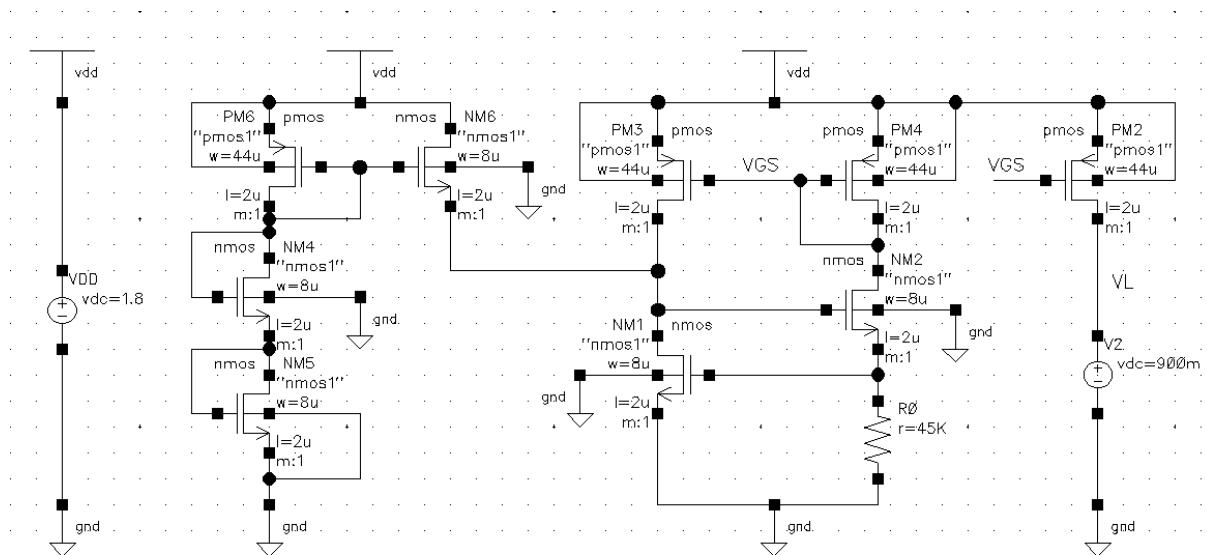
$$\text{Let } L = 2u$$

Calculate the W of PMOS.

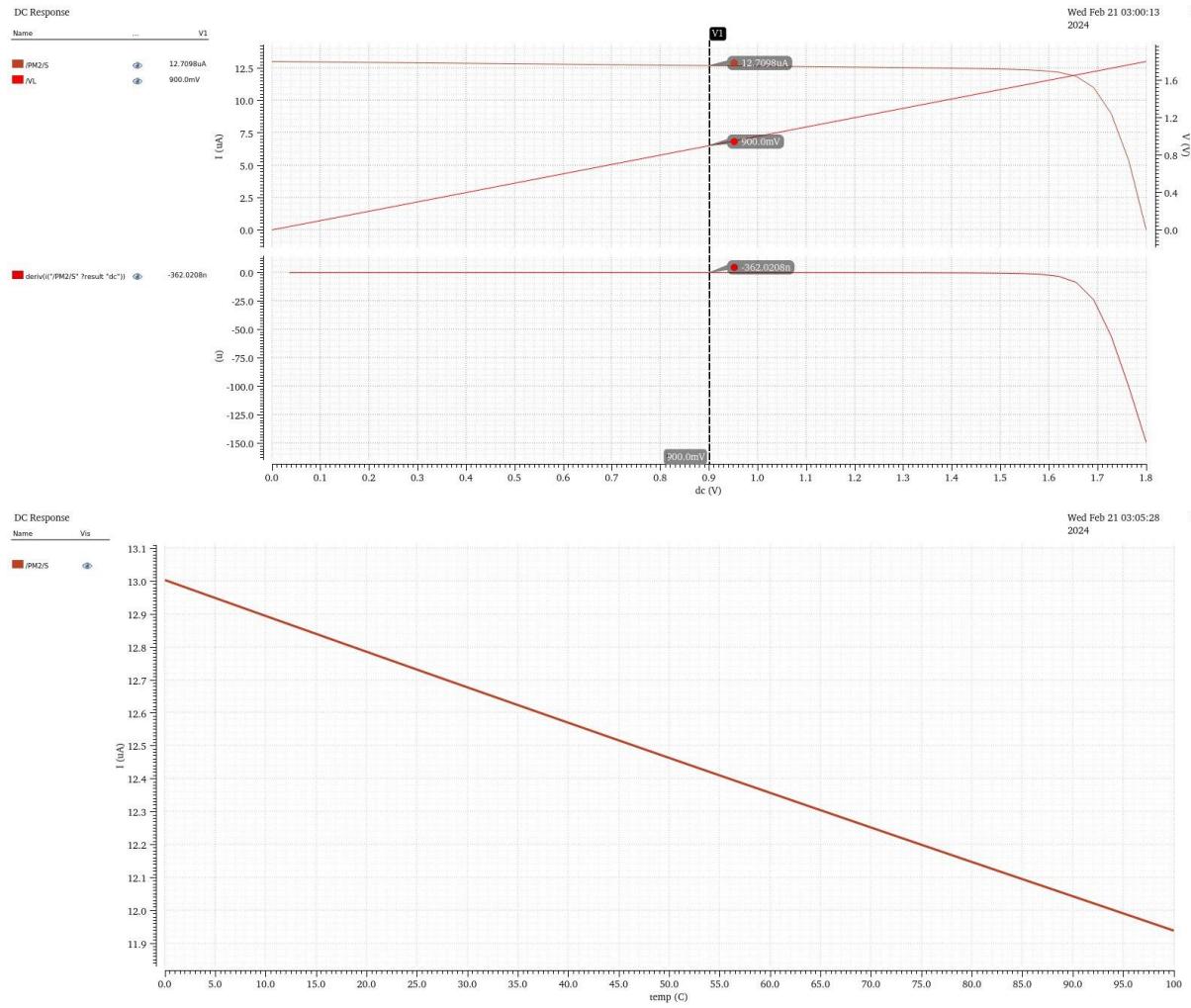
$$10u = \frac{1}{2} (40u) * (W/2u) * (VGS - VTH)^2 = 44.44u = 44u.$$

Calculate the W of NMOS.

$$10u = \frac{1}{2} (200u) * (W/2u) * (VGS - VTH)^2 = 8.88u = 8u.$$



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Negative Temperature Coefficient is observed.

8. Diode Referenced (CTAT)

Objective: Design a Diode referenced self biasing current source with IREF = 10uA.

Minimum emitter width allowed for PNP transistor is 0.6

$$I = \frac{V_d}{R} = I_s e^{V_d/n \cdot V_T}$$

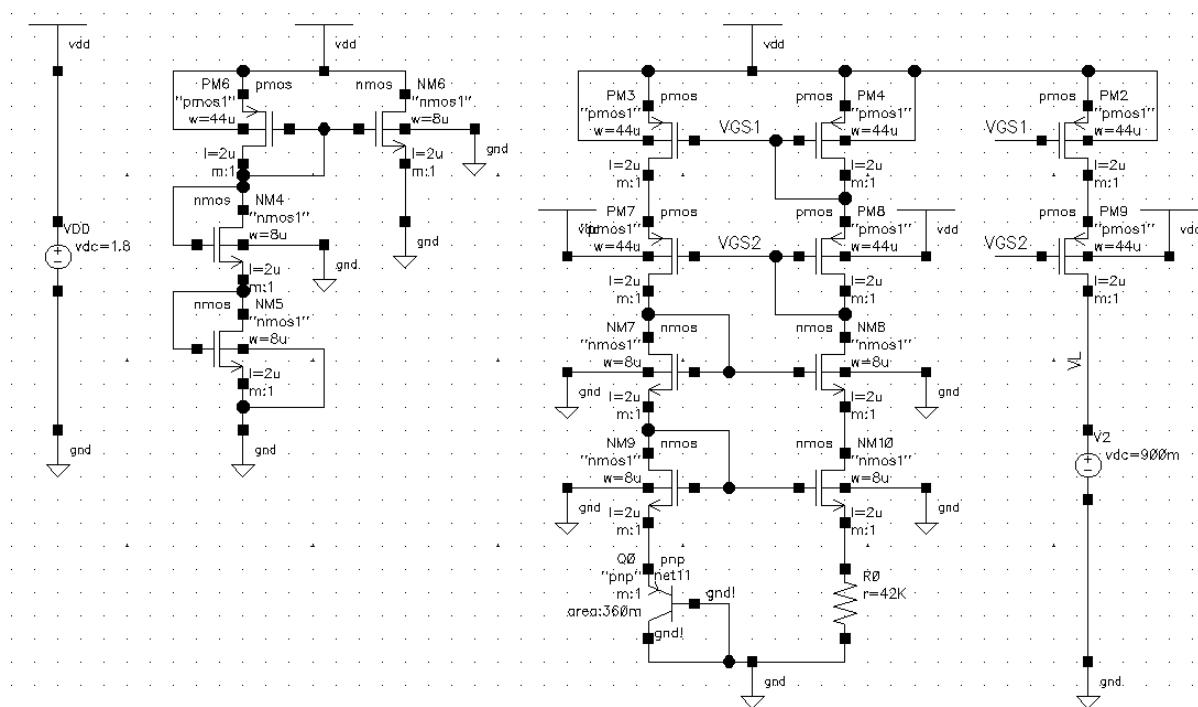
$$I_s = 10^{-15} \text{ A}$$

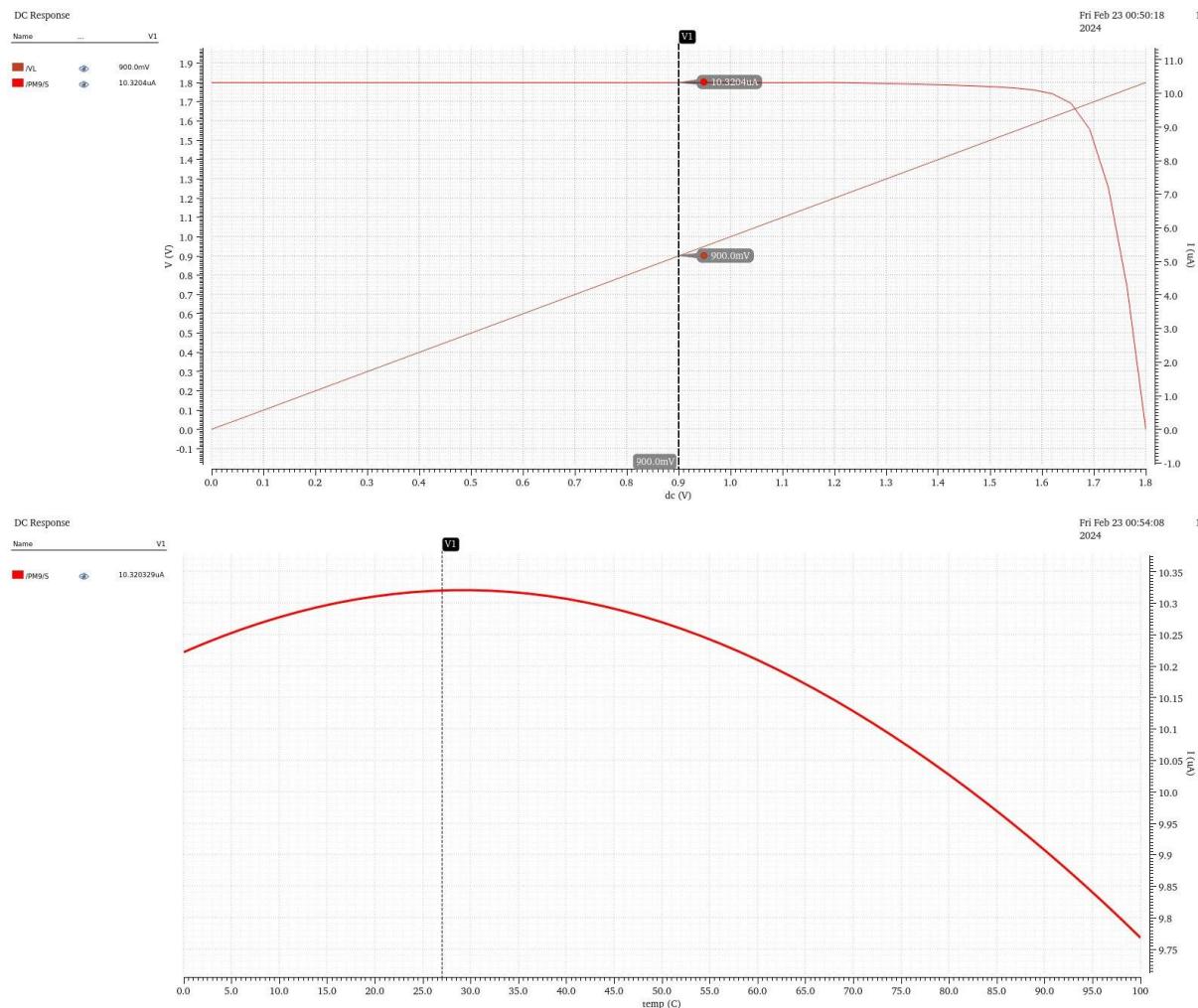
$$R = \frac{n \cdot V_T}{I} \ln \frac{I}{I_s}$$

$$I = 10\text{u}, \eta = 1, V_T = 26\text{mV}, I_s = 10^{-12}\text{A}$$

$$R = 2.6 \text{ K} * 16.11 = 41.886\text{K} = 42\text{K}$$

Note: Startup circuit is left unconnected





9. Thermal Voltage Referenced

Objective: Design a Diode referenced self biasing current source with $I_{REF} = 10\mu A$.

Minimum emitter width allowed for PNP transistor is 0.6

Second PNP transistor is K times

Let $K = 8$

$$V_{d1} = IR + V_{d2}$$

$$I_{d1} = I_s e^{V_{d1}/nV_T} \rightarrow V_{d1} = nV_T \cdot \ln \frac{I}{I_s}$$

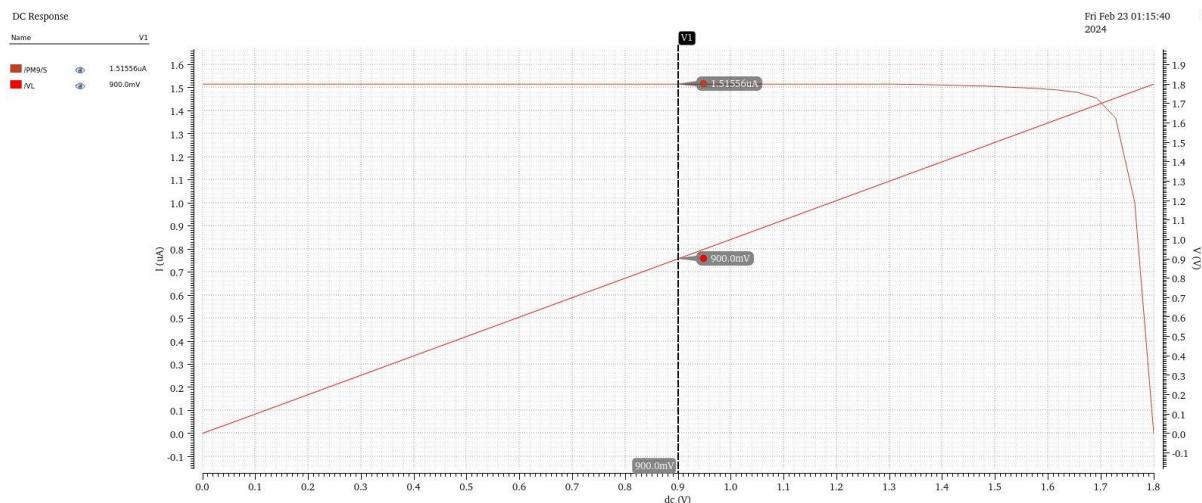
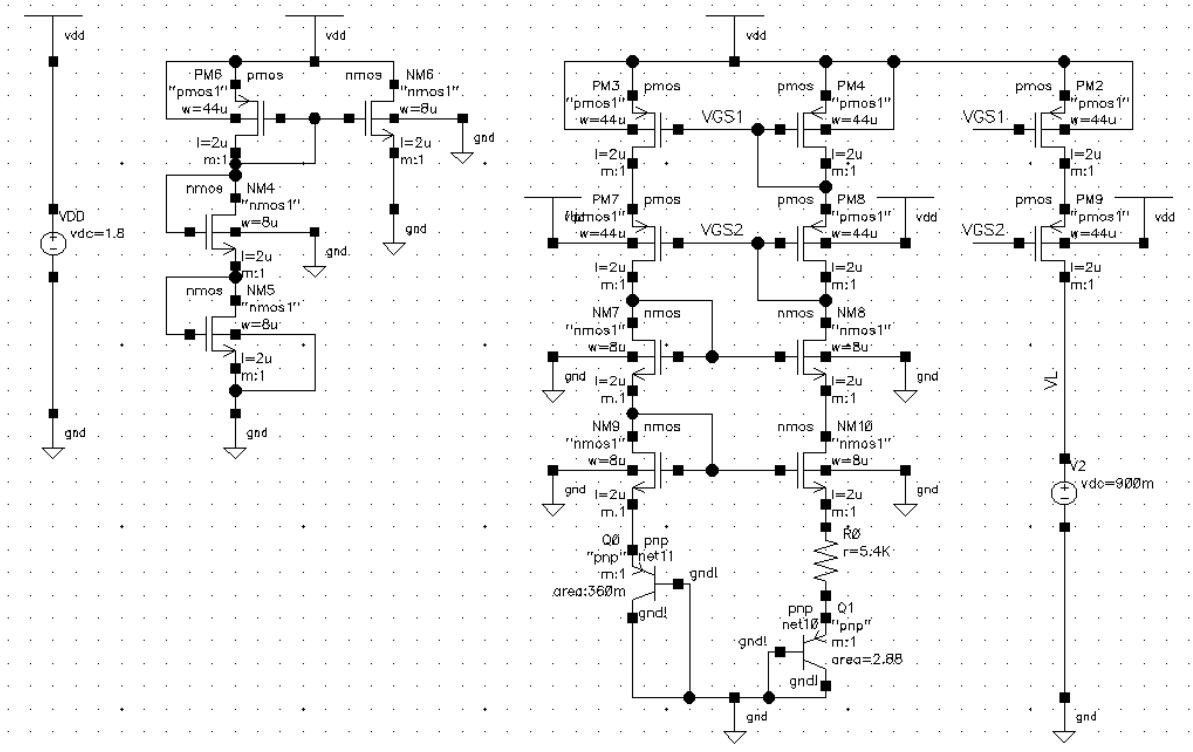
$$I_{d2} = K \cdot I_s e^{V_{d2}/nV_T} \rightarrow V_{d2} = nV_T \cdot \ln \frac{I}{K \cdot I_s}$$

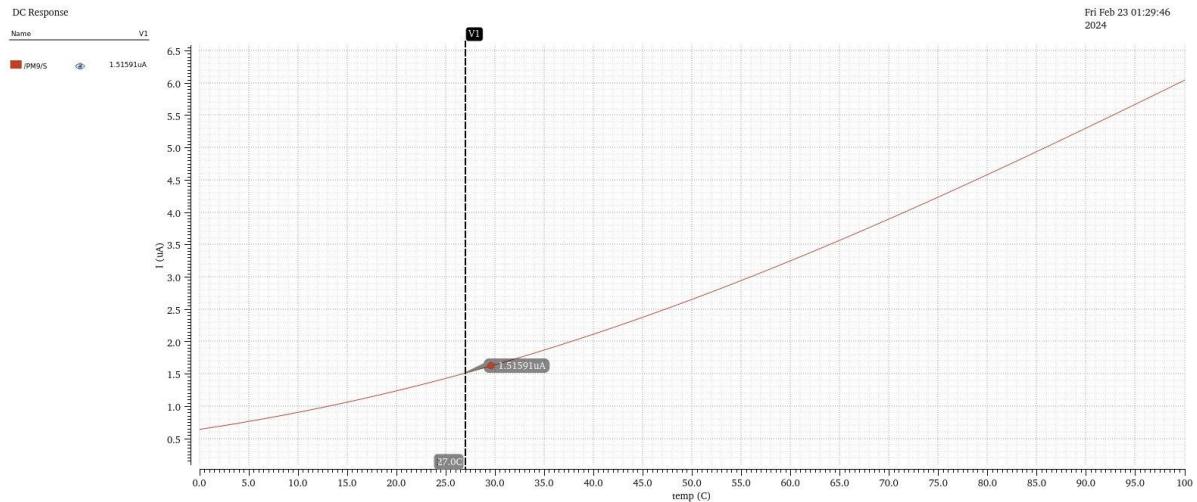
$$R = \frac{nV_T \cdot \ln K}{I} \text{ or } I = \frac{nk \cdot \ln K}{qR} \cdot T$$

$I = 10\mu A$, $\eta = 1$, $VT = 26mV$, $K = 8$

$R = 5.4K$

But for $K = 8$ current is very low, need to find the reason





10. Bandgap Voltage Reference

11. Beta Multiplier Reference Self Bias

12. Common Source Amplifier

12.1. Common Source with Resistor Load

Design a Common Source Amplifier with Resistive Load.

VDD = 1.8V

f = 100MHz

Av = 5

CL = 5pF

$$R = 1/2\pi f c = 318.3098$$

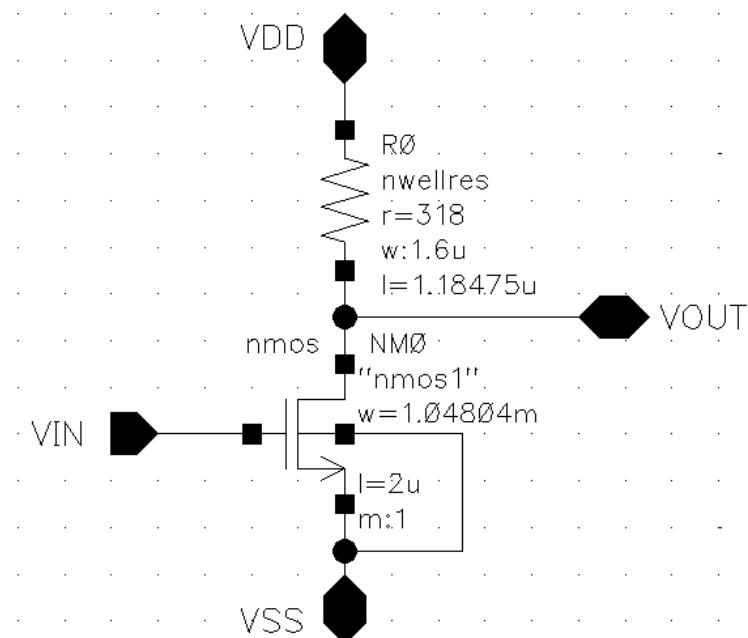
$$A_v = -gm R \Rightarrow gm = 15.7079m$$

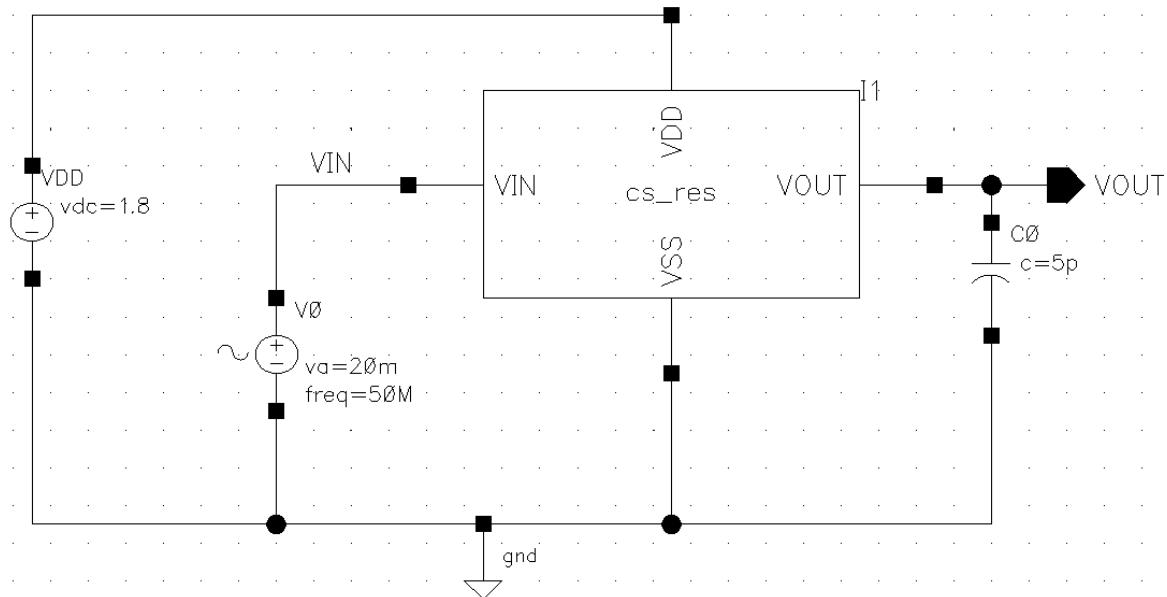
Let VGS = 0.6V, VTH = 0.45, Kn = 200u and set L = 2u

$$ID = \frac{1}{2} gm (VGS - VTH) = 1.17mA$$

$$gm = Kn (W/L) (VGS - VTH)$$

$$W = 1047.1933u = 1048u$$





AC Source = 20m, 50M signal, DC Voltage = 600m , AC Magnitude = 1

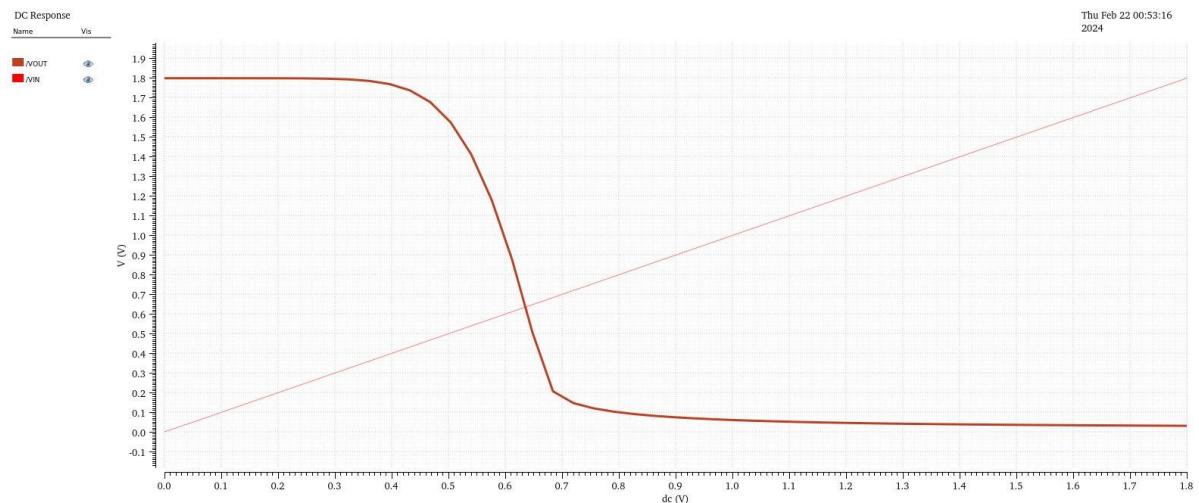
Perform DC analysis by varying the DC voltage of ac source and note down the operating condition by printing DC operating points

Vary DC voltage of ac source from 0 to 1.8

$V_{TH} = 467.84m$

$R_O = 17.3K$

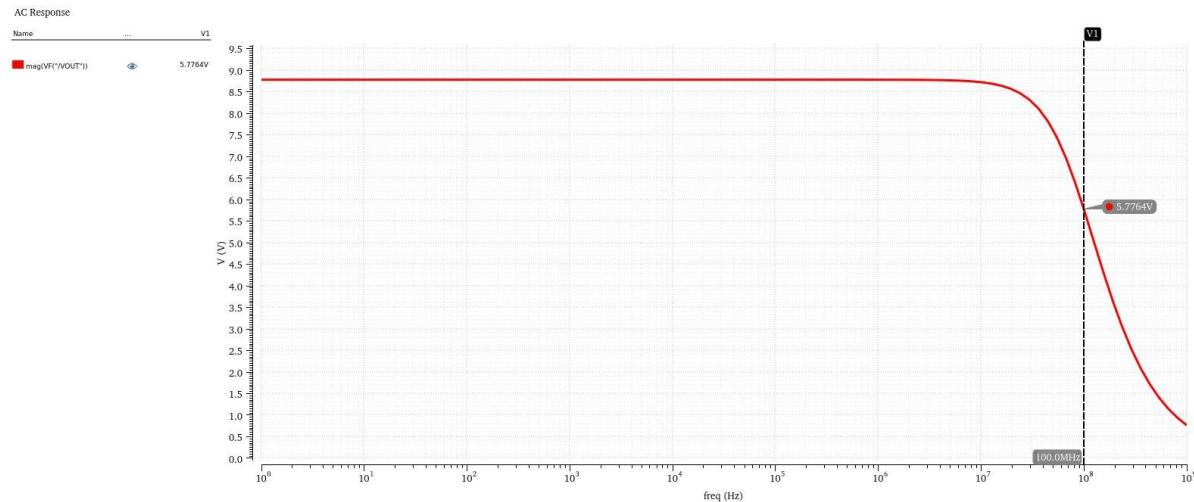
$g_m = 28m$



Perform ac analysis to calculate gain

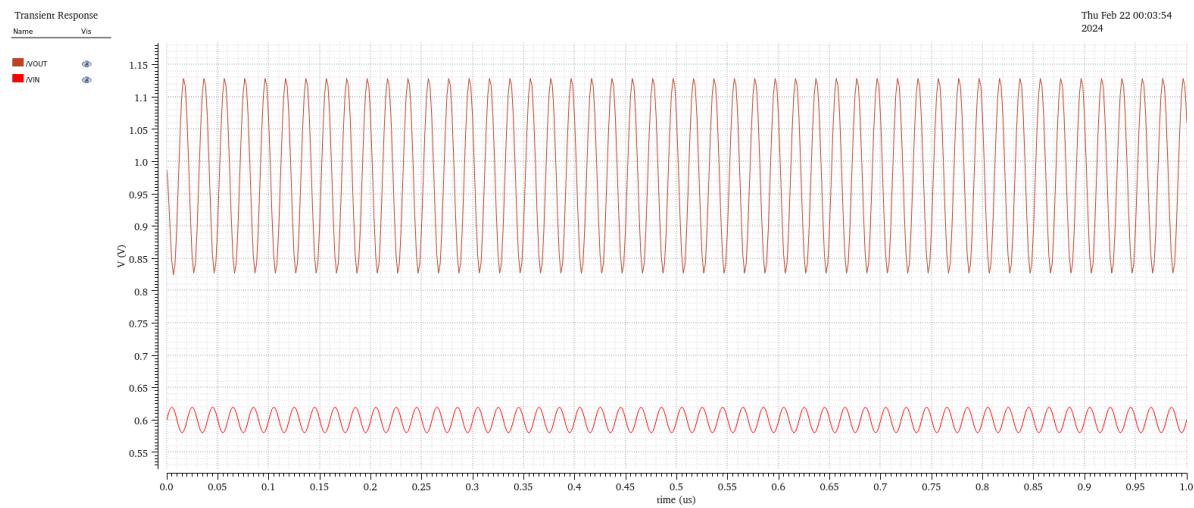
Vary frequency from 1 to 1GHz

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Perform Transient Analysis

Calculate Peak to Peak Voltage using calculator



peakToPeak(v"/VIN" ?result "tran")	
Expression	Value
1 peakToPeak(v"/...	39.89E-3
<hr/>	
Expression	Value
1 peakToPeak(v"/...	304.2E-3

$$Av = 7.625$$

12.2. Common Source with PMOS Diode Load

Design a Common Source Amplifier with PMOS Diode Load.

VDD = 1.8V

f = 100MHz

Av = 5

CL = 5pF

$$A_v = -\sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_2}}$$

$$Av = -gm \cdot RO \Rightarrow gm = 15.7079m$$

Let VGS = 0.6V, VTH = 0.45, Kn = 200u and set L = 2u

$$ID = \frac{1}{2} gm (VGS - VTH) = 1.17mA$$

$$gm = Kn (W/L) (VGS - VTH)$$

$$W = 1047.1933u = 1048u$$

12.3. Common Source with NMOS Diode Load

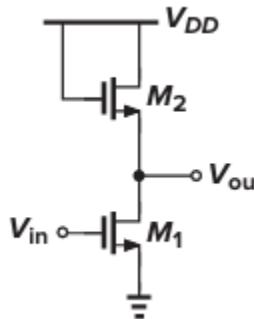
Design a Common Source Amplifier with PMOS Diode Load.

VDD = 1.8V

f = 100MHz

Av = 5

CL = 5pF



$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}$$

Let L1 = L2 = 1u

Let W1 = 1u

Then

$$25 = W2/1u \Rightarrow W2 = 25u$$

12.4. Common Source with Current Source Load

Finding Intrinsic Gain, Let $IDS = 10\mu A$
Assume $L = 180n$, $\lambda = 20\mu$, $K_n = 150\mu$

$$IDS = 10\text{uA}$$

Then $W = 4.444\text{u} = 4.4\text{u}$

$$gm = 25u$$

$$RO = 1/\lambda \text{ IDS} = 20M$$

$$Av = -gm * RO$$

$$Av \equiv 2640$$

Practically for 400n/180n size

$$Gm = 98u$$

Ro = 56K

$$Av = 5.488$$

This can also be observed from the ac analysis

Reg. Number	Max. Marks: 50	Max. Time: 3 Hours
VLS 5251: Advanced VLSI Design Lab		
Part - A		(20 marks)
1. Design a single stage common-source amplifier with a current mirror load for a small signal voltage gain (A_v) of 10v/v .		
a. Use $V_{DD} = 1.8\text{V}$ and 180nm technology and the appropriate model file for the required process parameter values.		
b. Missing values, if any, may be suitably assumed.		
2. Draw a neat diagram of the design specifying all the values.		
3. List all the formulae used in the design.		
Part - B		(20 marks)
1. Compare the results obtained both theoretically and practically through simulation.		
Part - C: Viva		(10 marks)

13. Common Drain Amplifier

13.1. Common Drain with Resistor Load

$$gm = Kn \left(\frac{W}{L} \right) (VGS - VTH)$$

13.2. Common Drain with NMOS Diode Load

14. Common Gate Amplifier

14.1. Common Gate with Resistor Load

Design a common gate amp with gain 10, and DC output voltage 0.9V.
Assume $IDS = 10\mu A$, $L = 1\mu m$

$$VDS > VGS - VTH$$

$$0.9 > VGS - 0.45$$

$$VGS = 1.35$$

$$VDD - VO = ID RD$$

$$RD = (1.8 - 0.9) / 10\mu A$$

$$RD = 90K$$

$$Av = gm RD$$

$$gm = 111.11\mu A/V$$

$$gm = \sqrt{2 K_n (W/L) IDS}$$

$$W = 3.085\mu m$$

$$ID = \frac{1}{2} (K_n) (W/L) (VGS - VTH)^2$$

14.2. Common Gate with PMOS Diode Load

15. Differential Amplifier Pair

Design Differential amplifier with Gain $A_v = 40$

Given bias current $I_{SS} = 200\mu A$

Assume $\lambda = 5m$, $K_n = 200\mu$

Then $I_{D1} = 100\mu A$

We know that

$$R_{DS} = 1/\lambda I_{DS1}$$

$$R_{DS} = 1/5m * 100\mu = 2M$$

We know that

$$A_v = g_{m1} (r_{ds2} // r_{ds4})$$

$$g_m = A_v / (R_{DS1} || R_{DS2})$$

$$g_m = 40 / (2M || 2M)$$

$$g_m = 40\mu$$

We know that

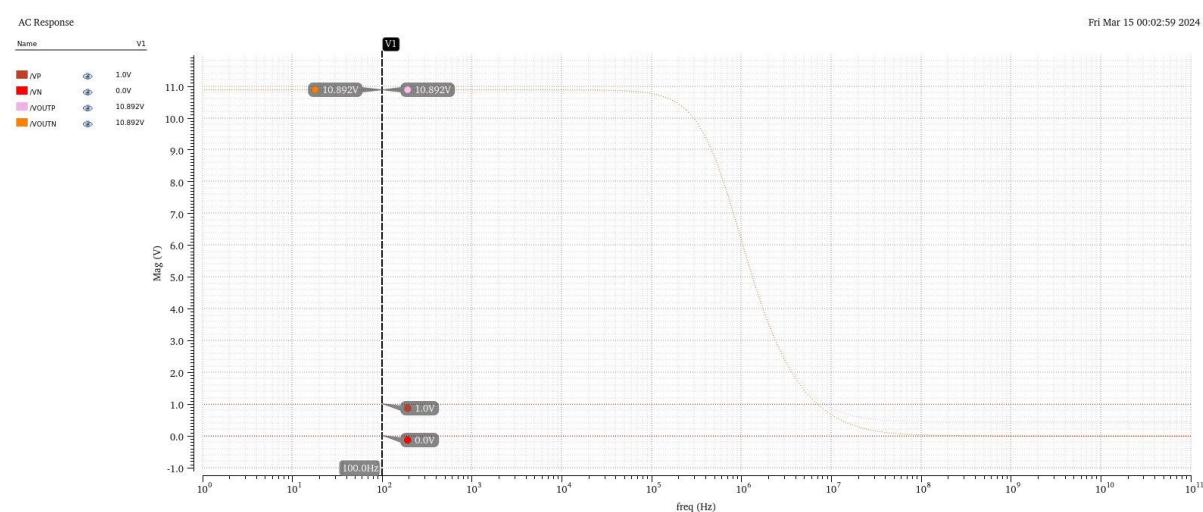
$$g_{m1} = g_{m2} = [\mu_n C_{ox} I_{SS} (W/L)]^{1/2}$$

$$40\mu = (K_n I_{SS} (W/L))^{1/2}$$

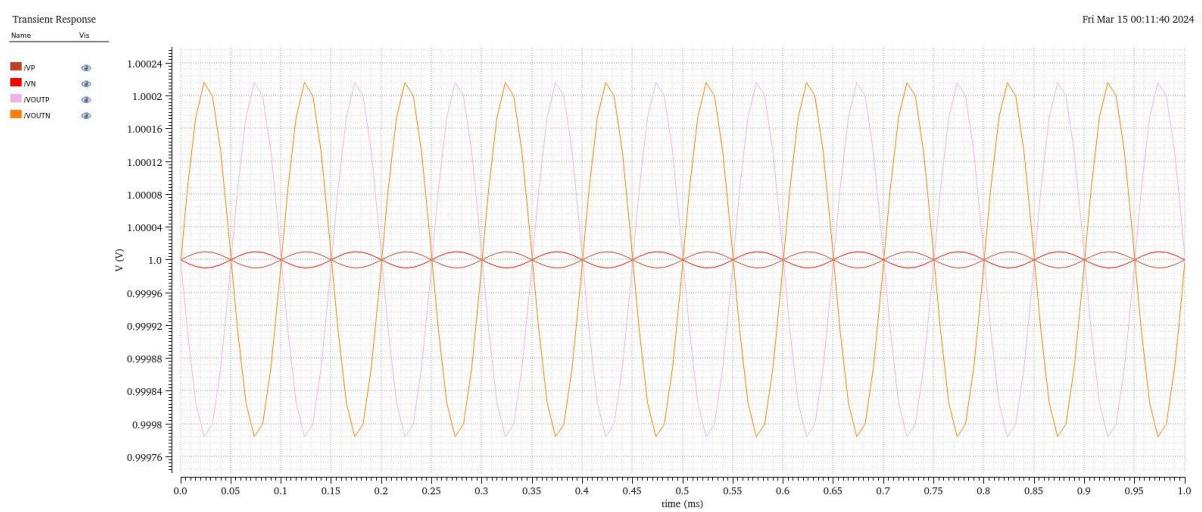
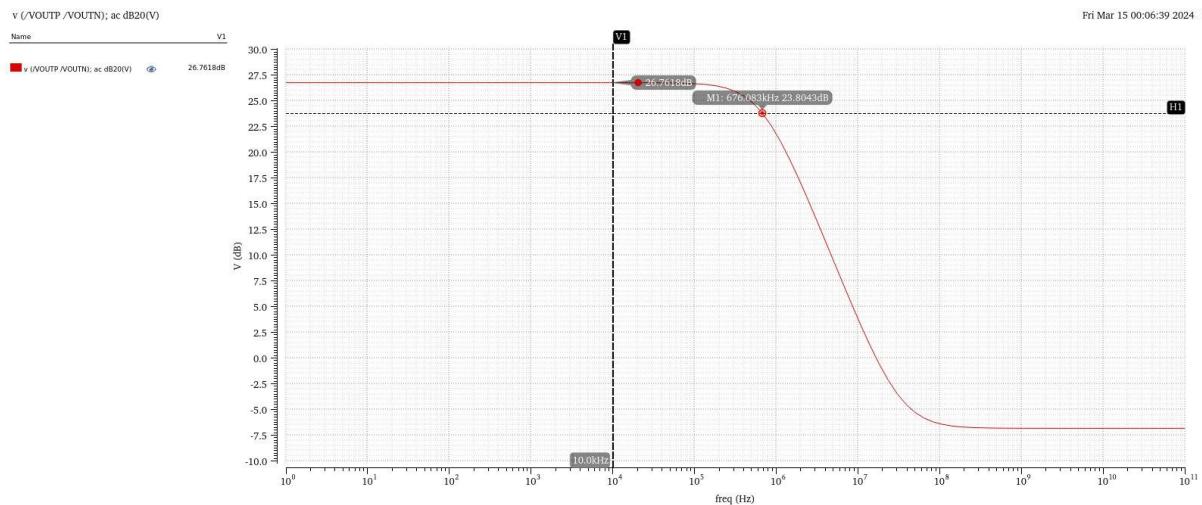
$$1600 = 40000 (W/L)$$

$$1/25 = W/L$$

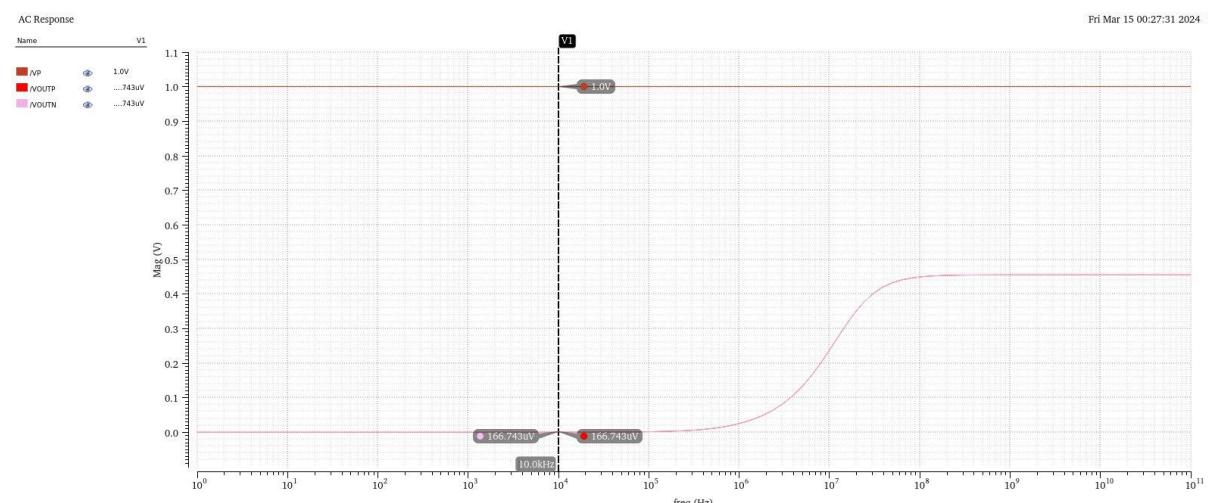
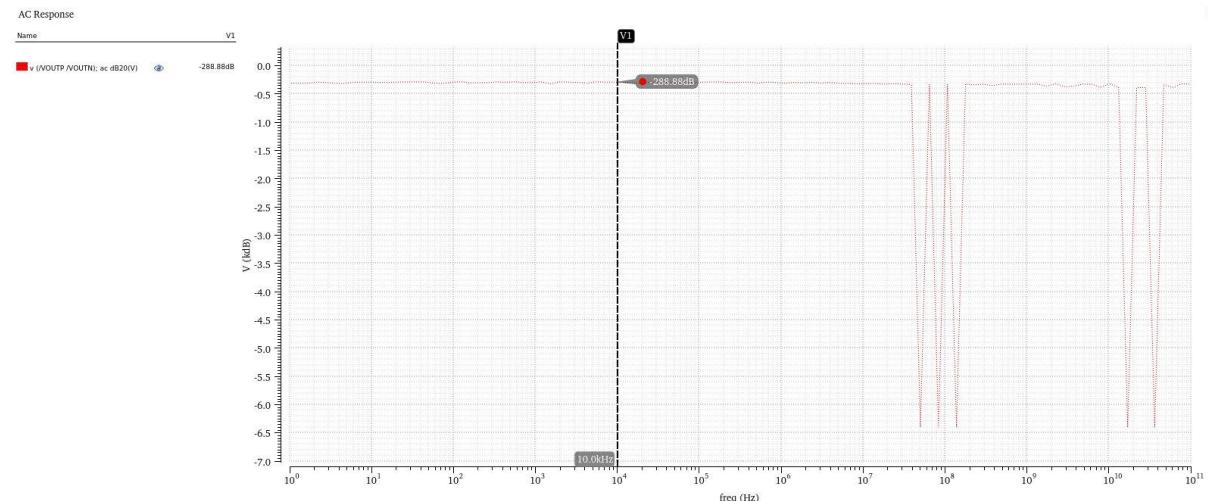
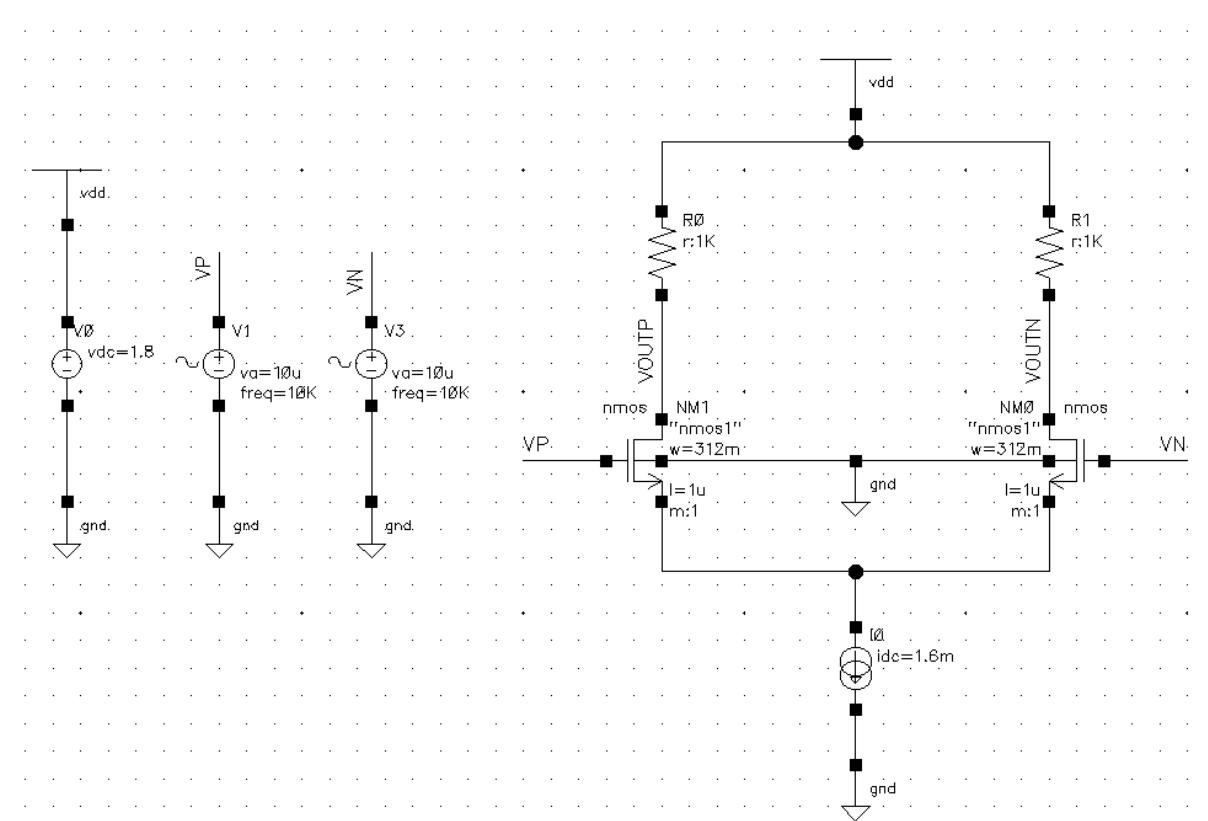
Let $W = 1\mu$ and $L = 25\mu$



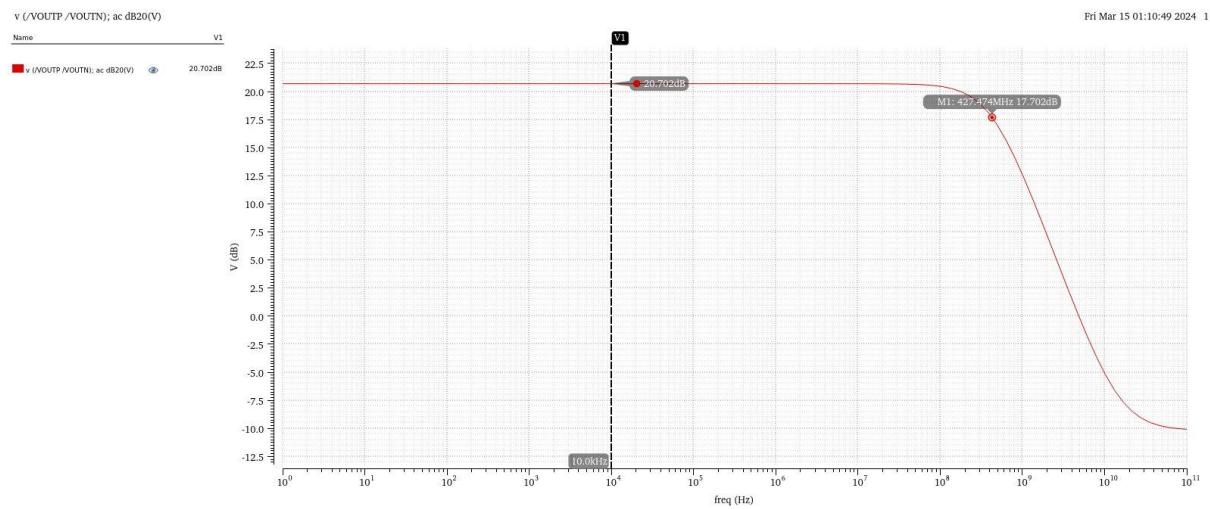
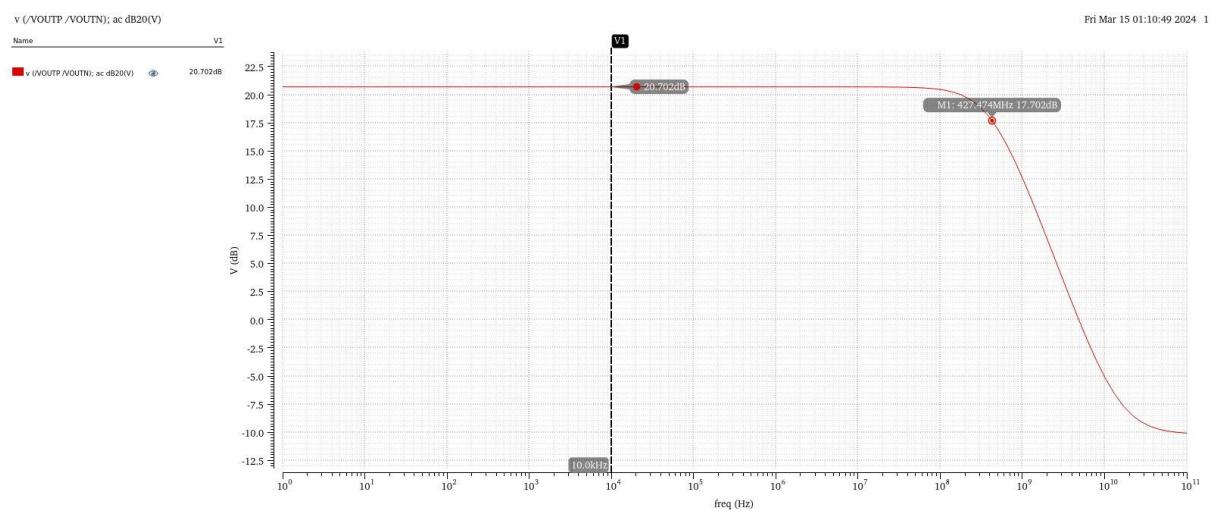
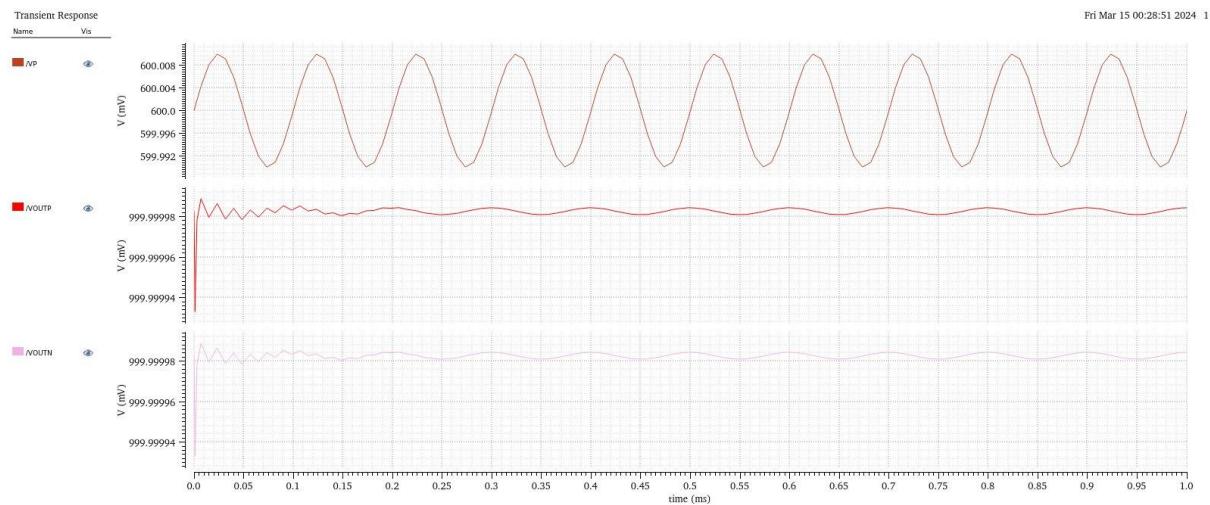
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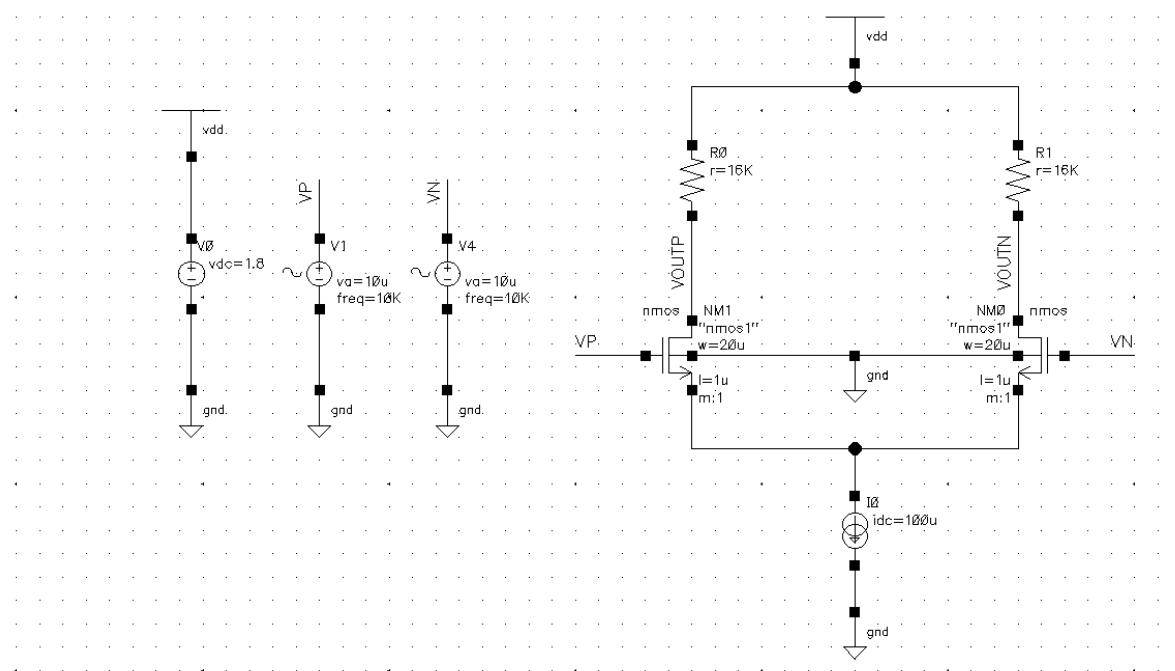
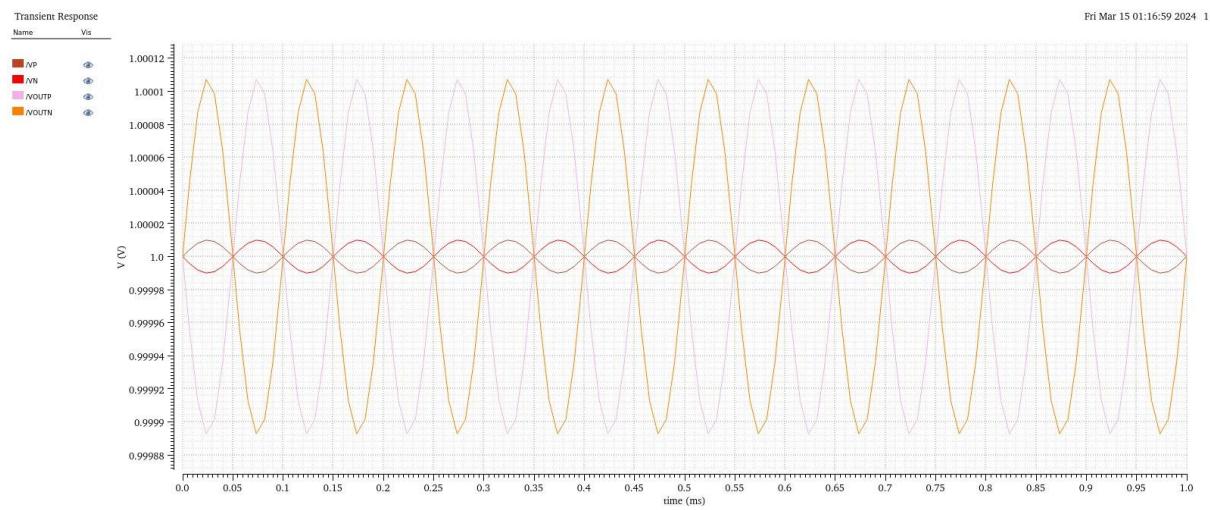
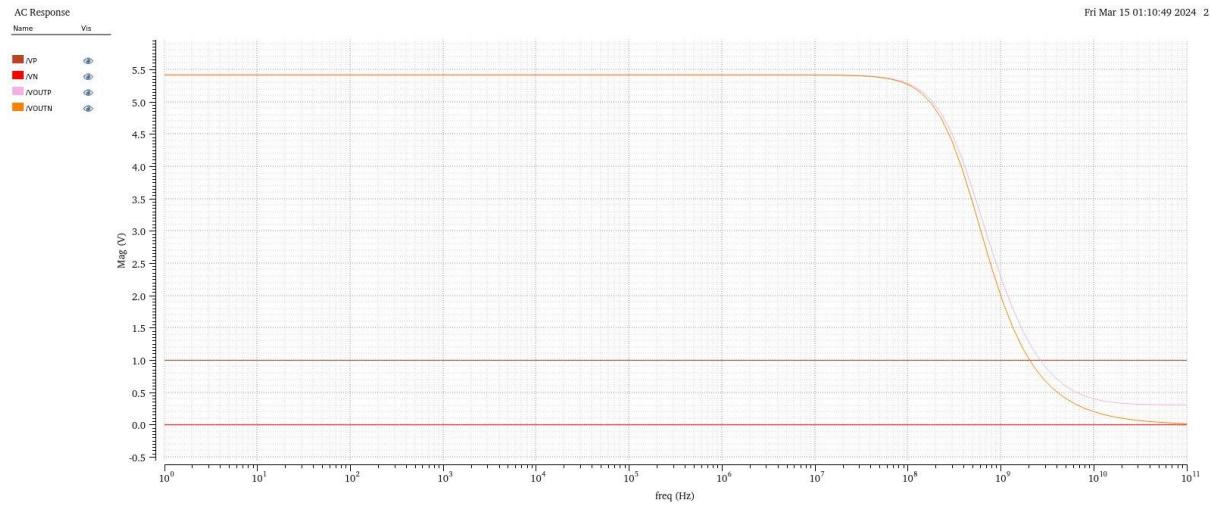
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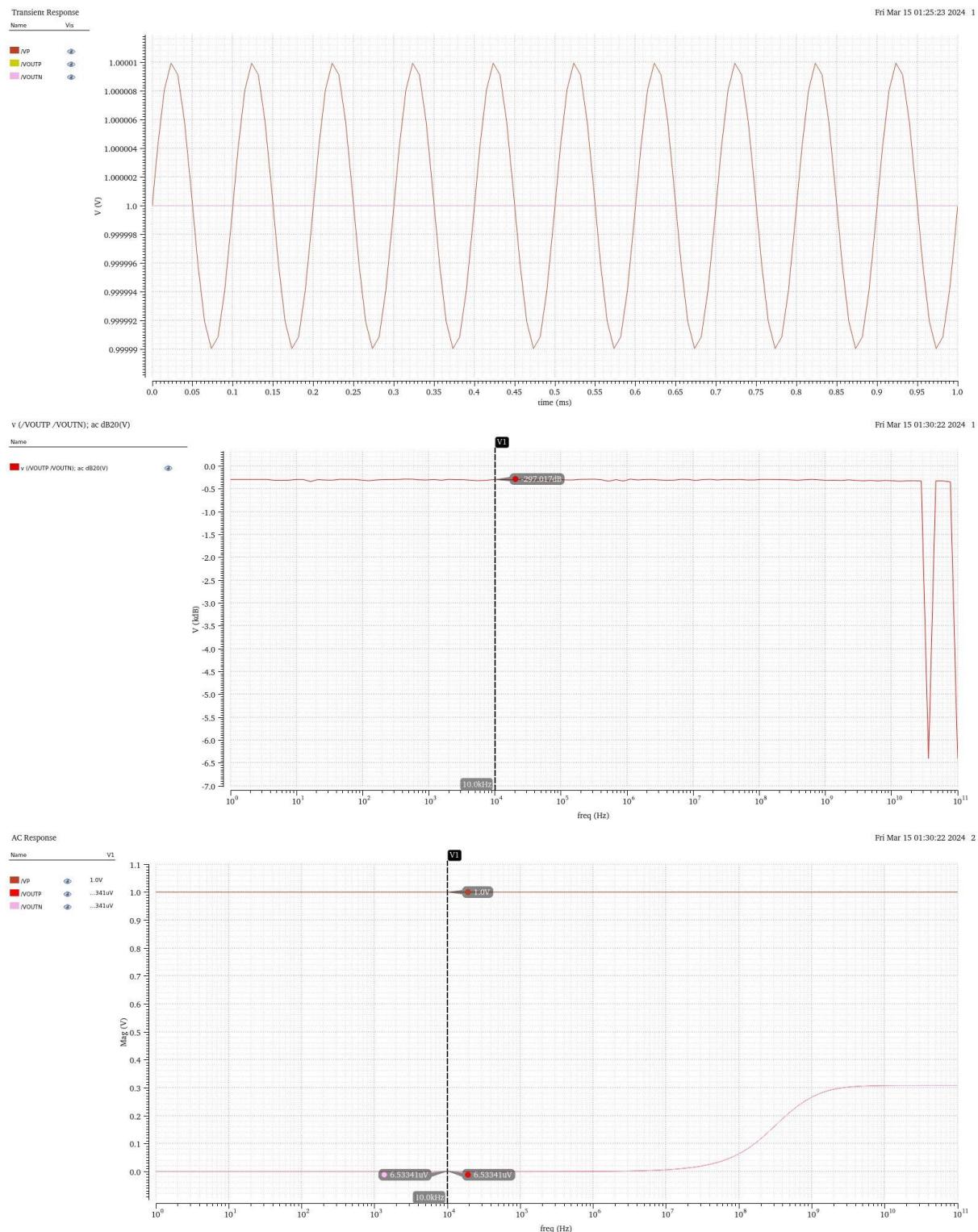
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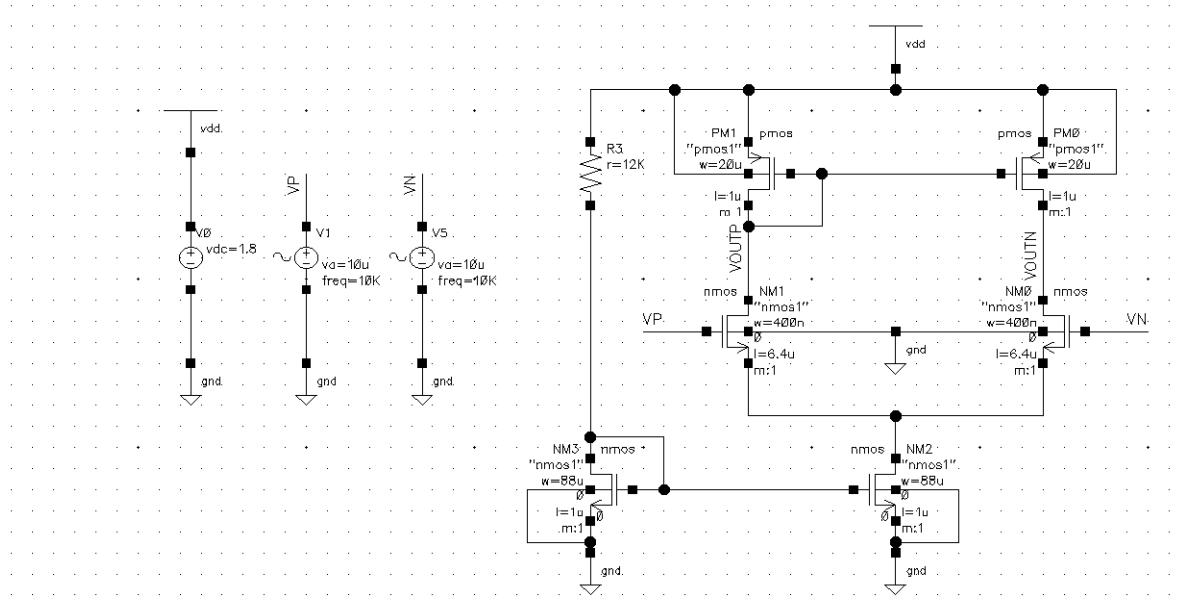
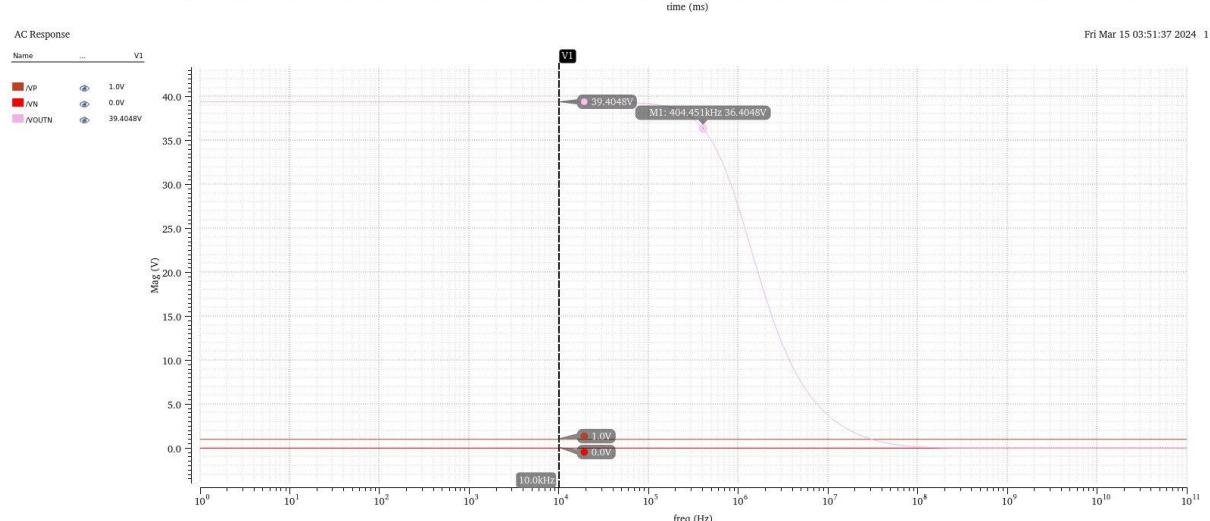
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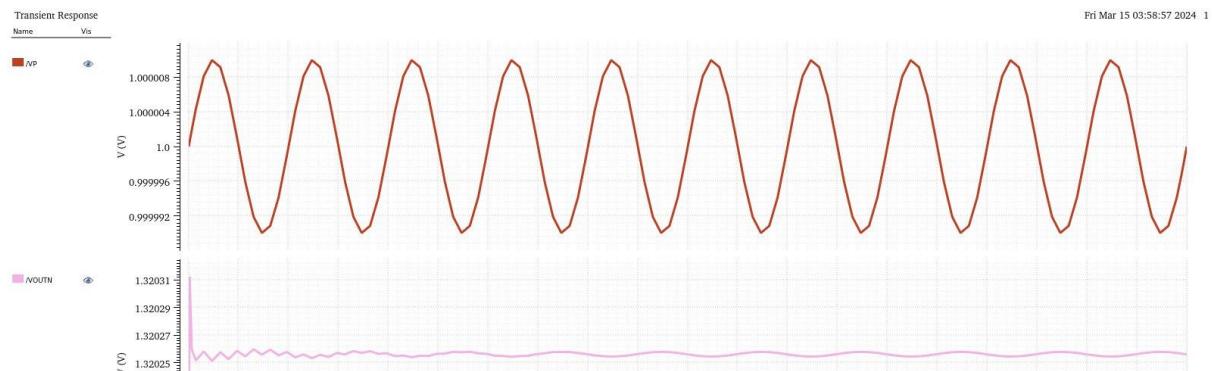
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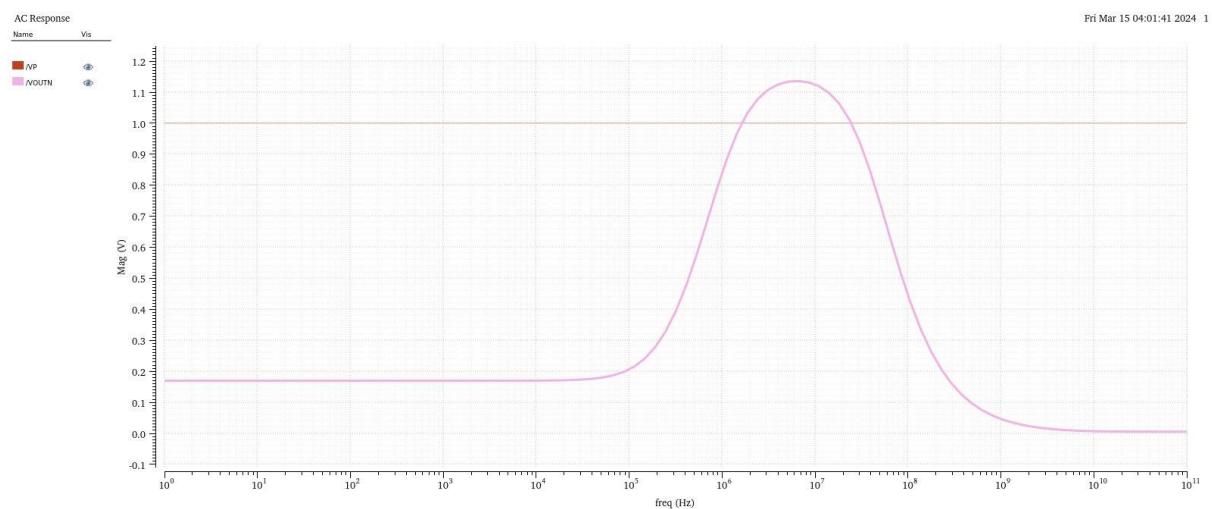
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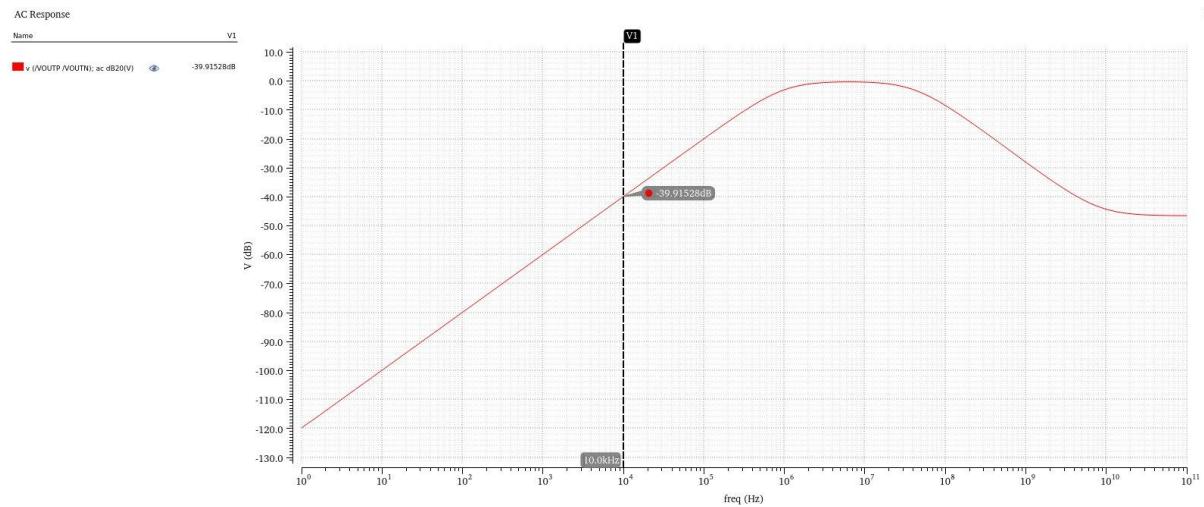
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