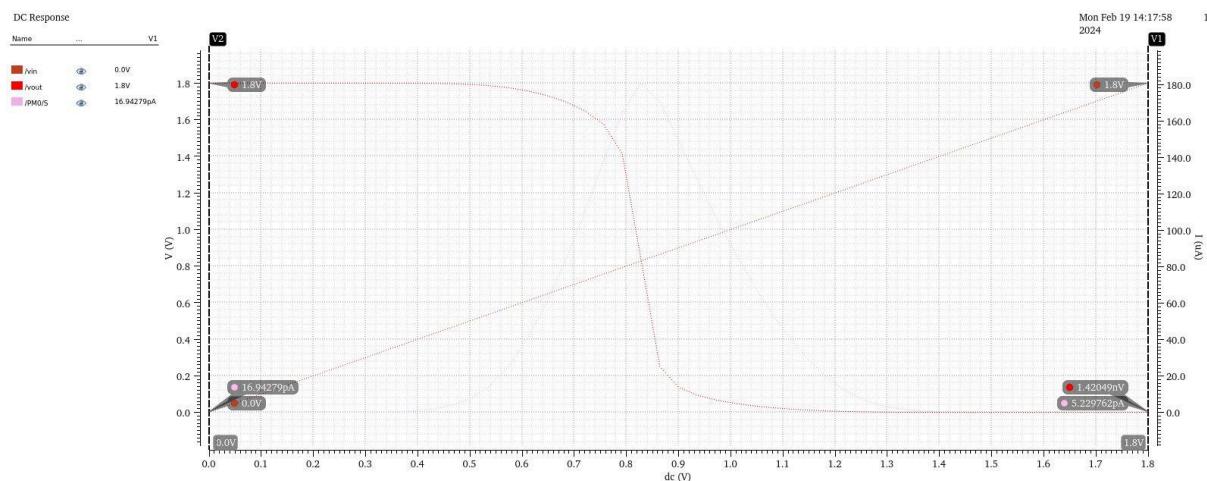
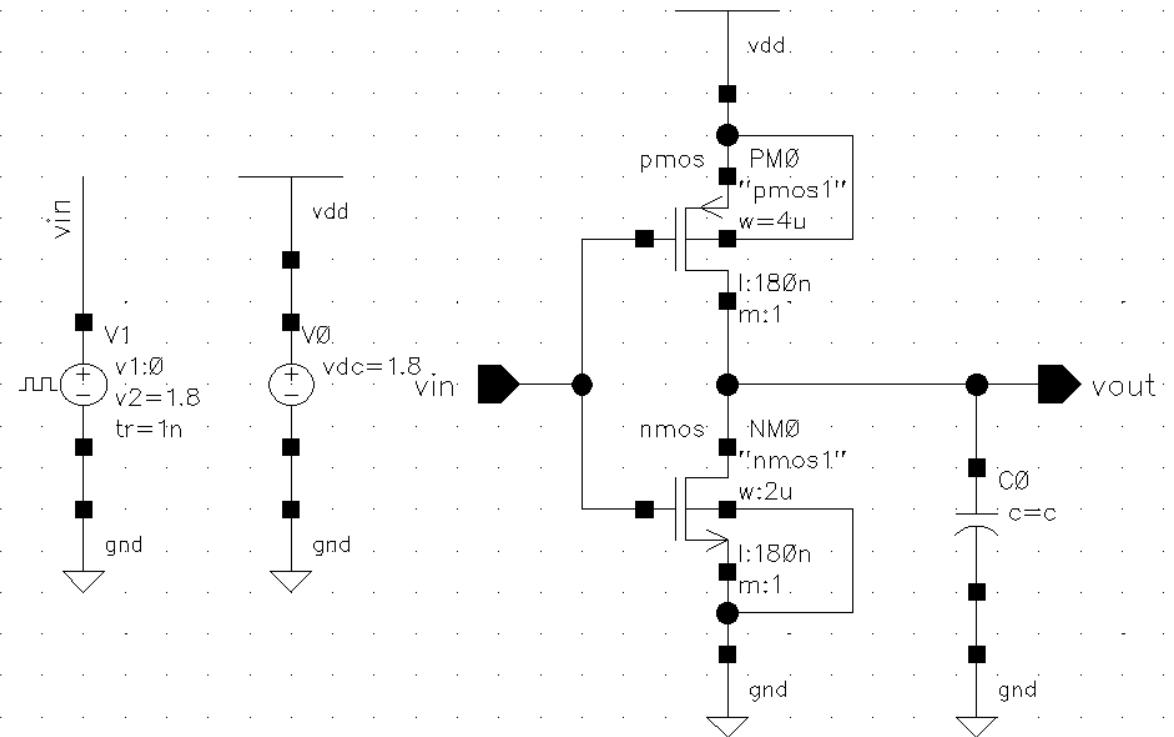
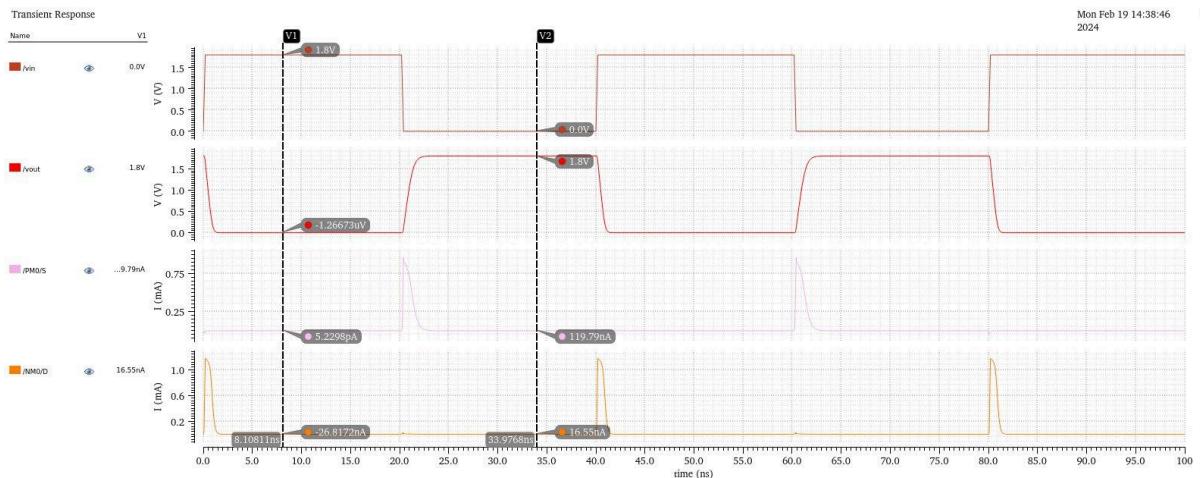


1. Plot I_{SC} for inverters by choosing suitable CL and W/L ratios for the MOS transistors.





Observe the variation of Short Circuit Current with respect to load capacitance. Set some finite value for rise and fall times of input.

Say Period = 40n, Pulse Width = 20n, Tr, Tf = 1n



When input is making 0 to 1 transition, NMOS turns on to discharge load capacitance, but short circuit current also flows from PMOS through NMOS.

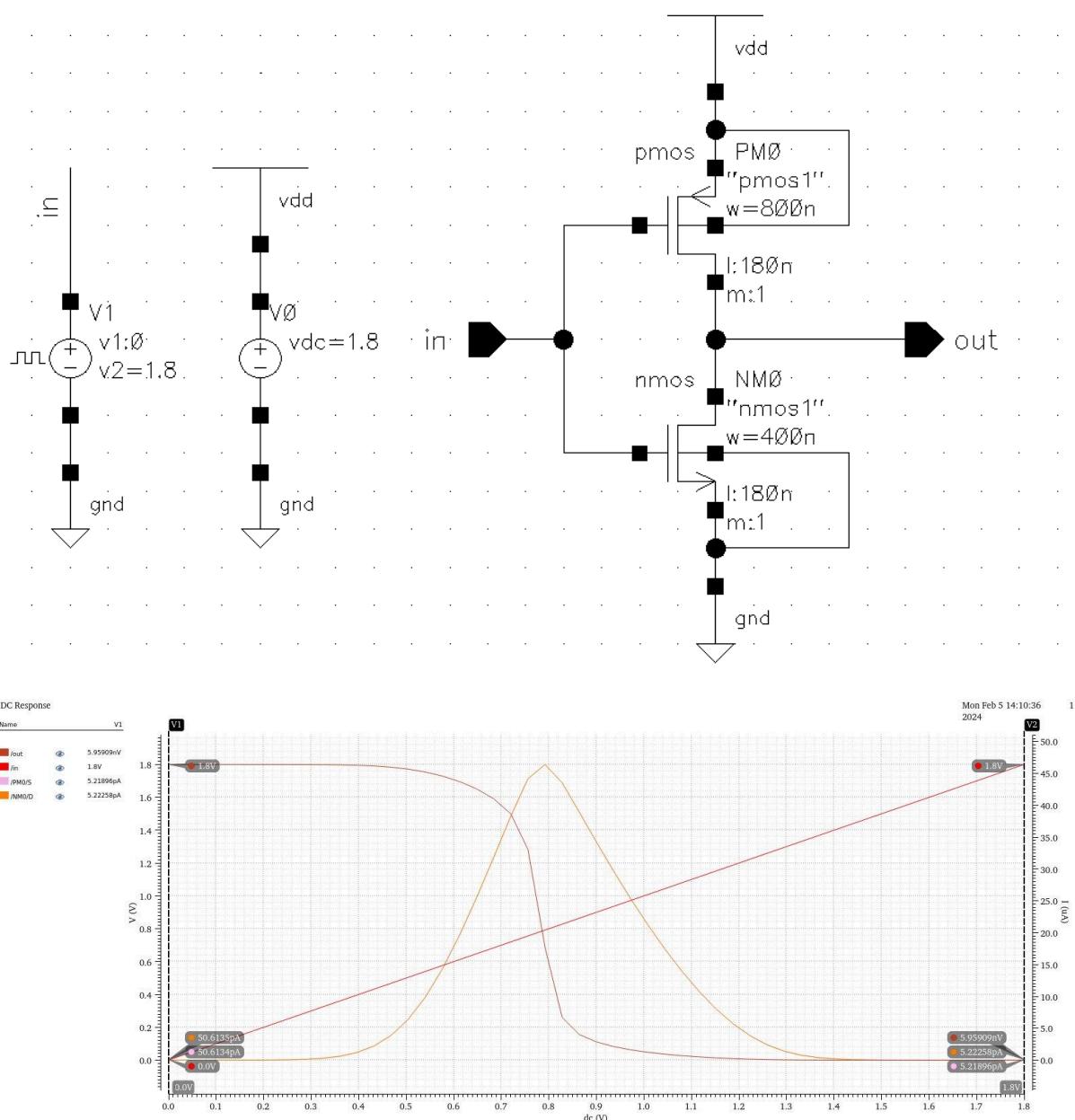
Similarly when input is making a 1 to 0 transition, PMOS will turn on and charge the load capacitance, but some amount of short current flows through NMOS.

Load Capacitance	Vin 0 → 1	Vin 1 → 0 (Isc)
0	128.5199u	163.4381u
10f	112.34u	143.43u
20f	104.65u	132.82u
50f	80u	117u
100f	61u	84u
200f	42u	64u

Short Circuit Current is decreasing as load capacitance is increasing.

When load capacitance is large, it takes more time to charge or discharge the load capacitance. During 0 to 1 transition of input, output will not go low as quick as input in that case $|V_{DS}| < |V_{GS}| - |V_{TH}|$, hence PMOS will be in a linear region and offers high resistance hence the short circuit current through PMOS will be reduced.

2. Plot leakage currents of minimum sized NMOS and PMOS transistors in 180nm.



Length	NMOS Width	PMOS Width	NMOS Leakage	PMOS Leakage
180n	400n	800n	50.6134pA	5.22258pA

180n	1u	2u	16.64428pA	4.350499pA
180n	2u	4u	16.9427pA	5.24147pA
180n	4u	8u	23.54176pA	7.44183pA

Length	NMOS Width	PMOS Width	NMOS Leakage	PMOS Leakage
360n	400n	800n	6.61647pA	2.94818pA
360n	1u	2u	6.10018pA	3.8492pA
360n	2u	4u	7.9794pA	5.4842pA
360n	4u	8u	12.2999pA	8.7919pA

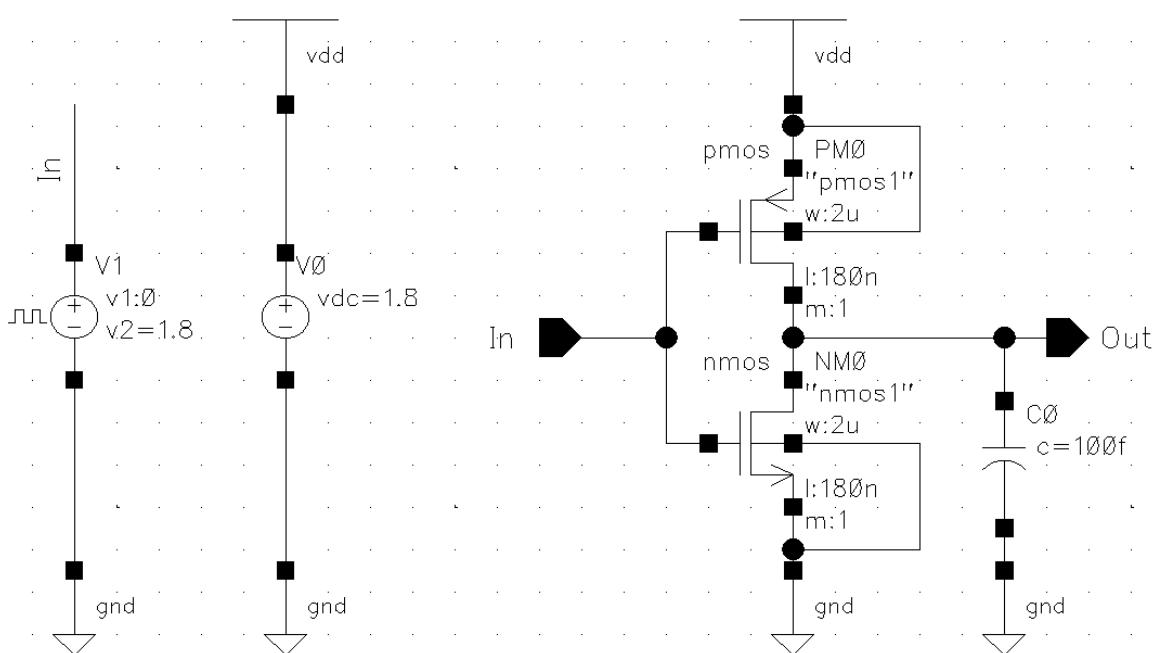
Minimum Transistor Length Supported in 180nm technology is 180 nm and minimum width supported is 400 nm.

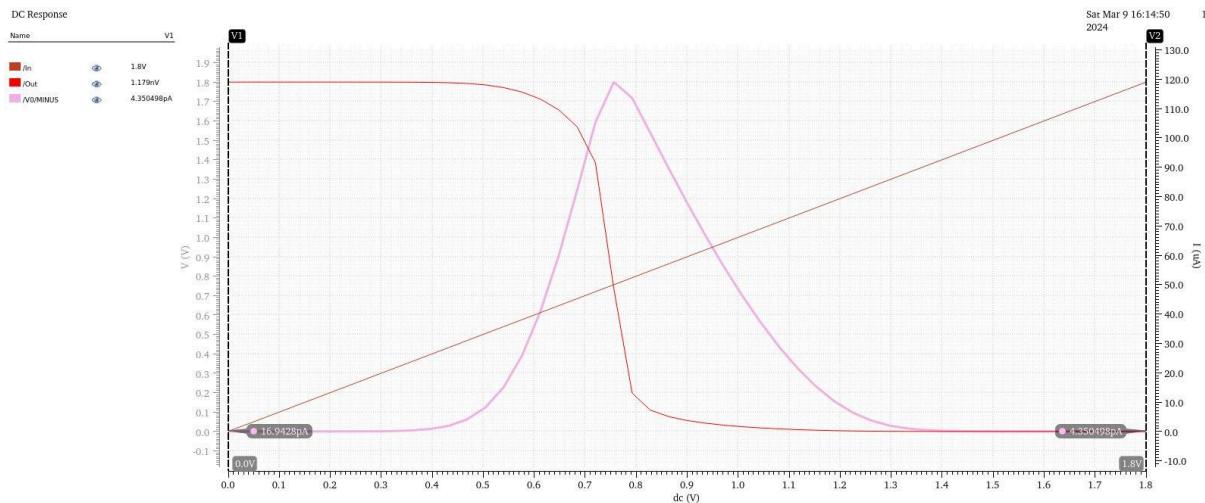
When length is kept constant and width of the transistor is varied, leakage current initially decreases and then increases.

When length of the transistor is increased then leakage current is reduced.

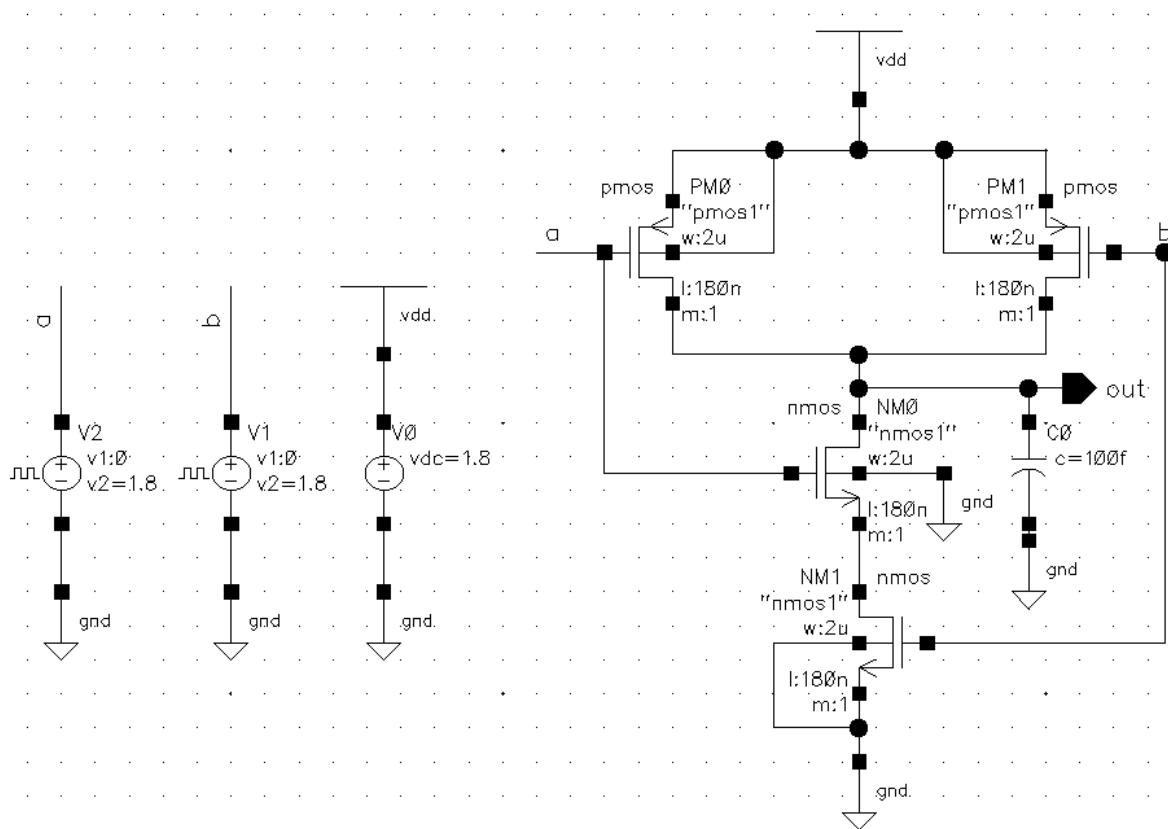
3. Natural stacking – check function and leakage current(I_{sub}) of

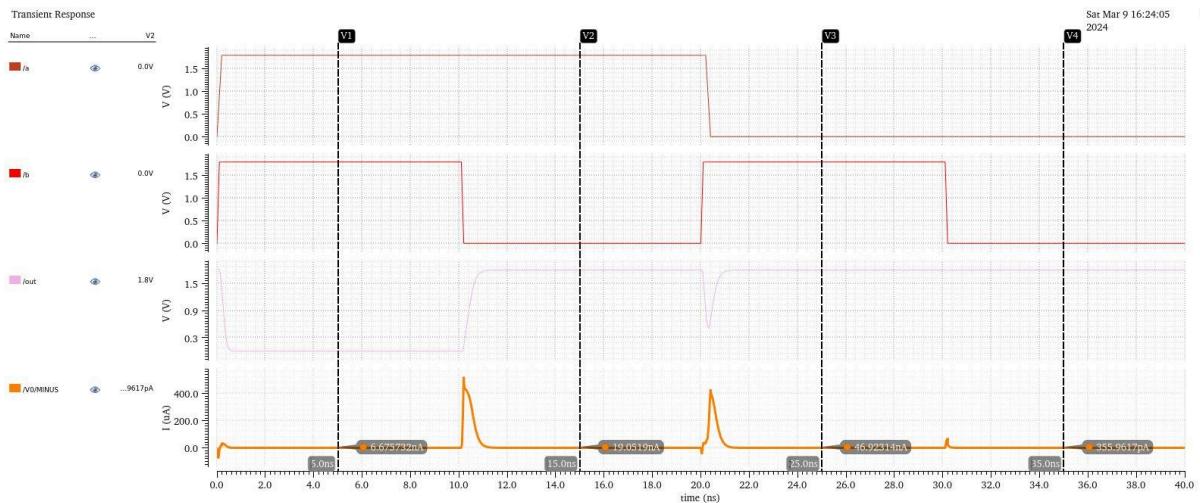
a) Inverter



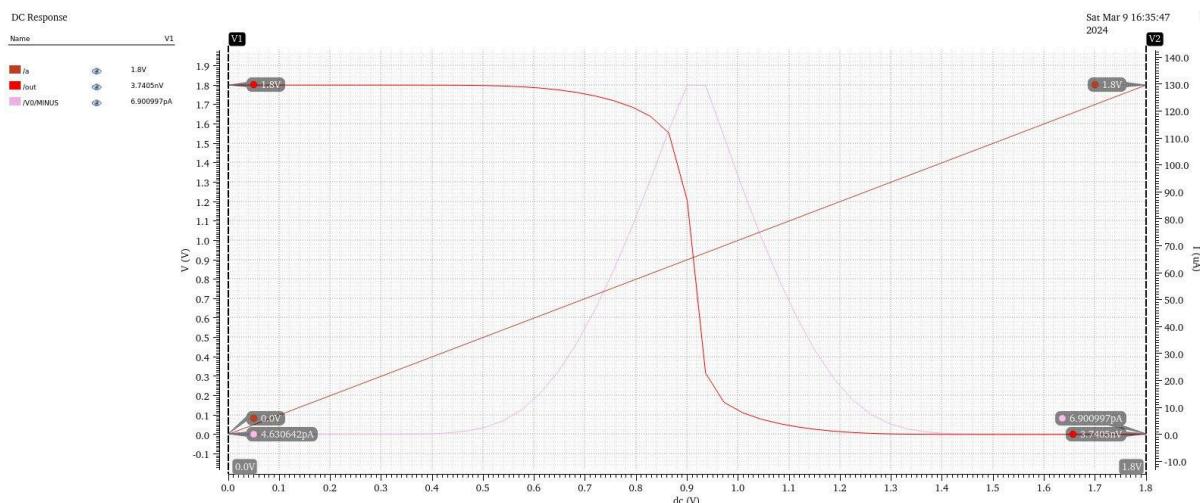


b) 2 input NAND gate for various input combinations.





A	B	Leakage
0	0	139.9pA
0	1	7.54pA
1	0	16.92pA
1	1	5.229pA

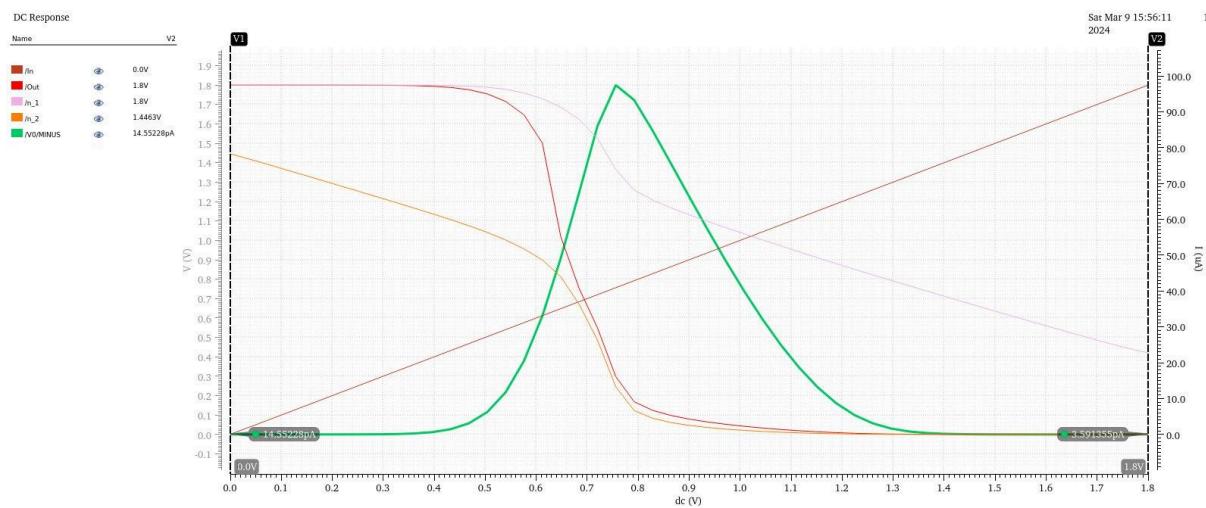
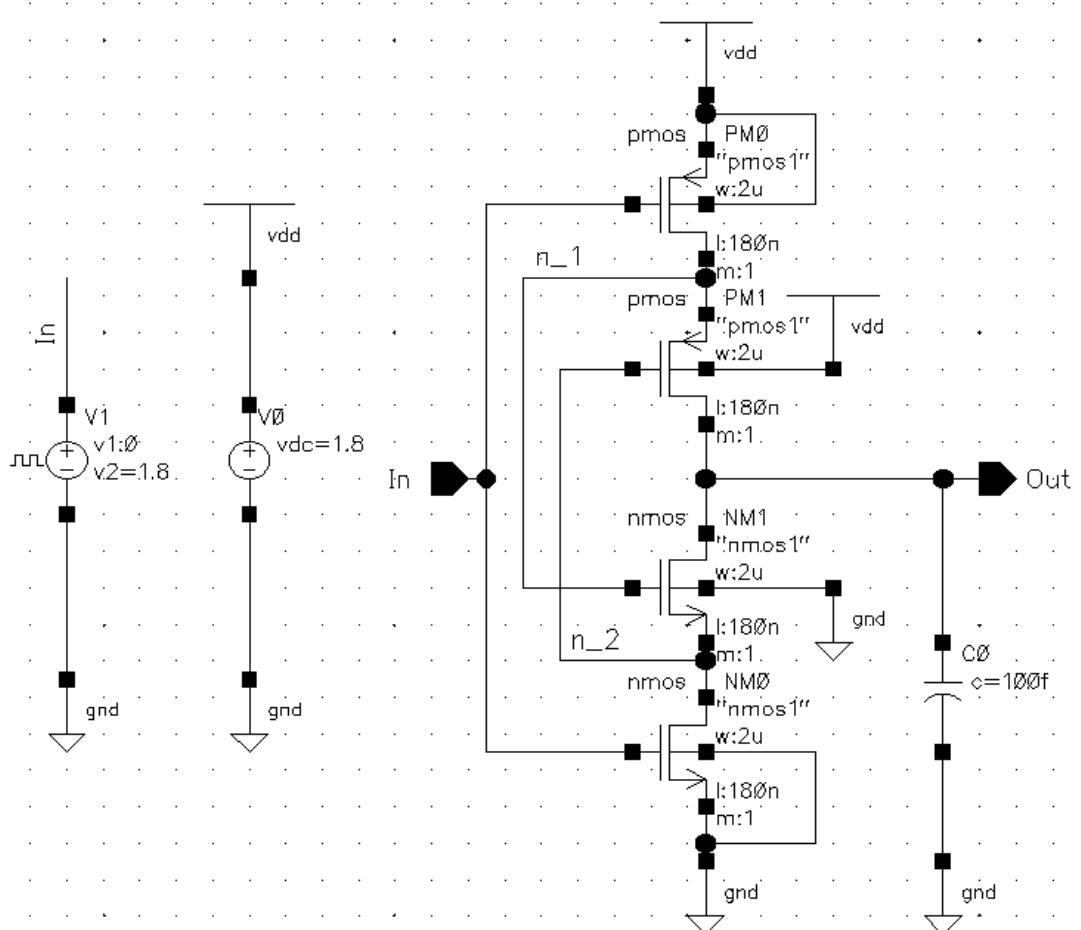


Circuit	NMOS Leakage	PMOS Leakage
Inverter	16.9428pA	5.2414pA
NAND (As inverter)	4.63pA	10.48pA

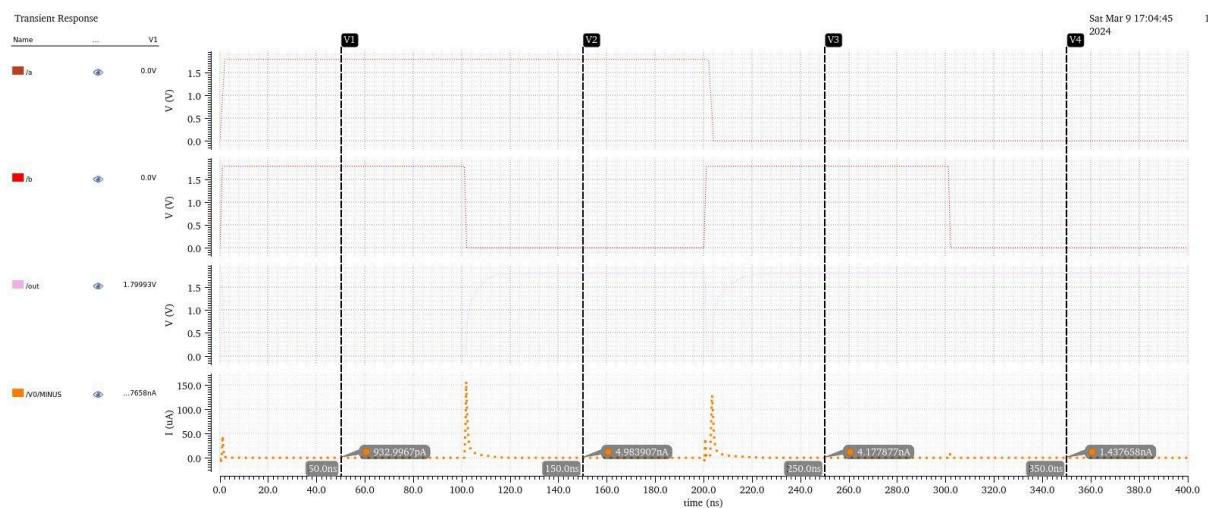
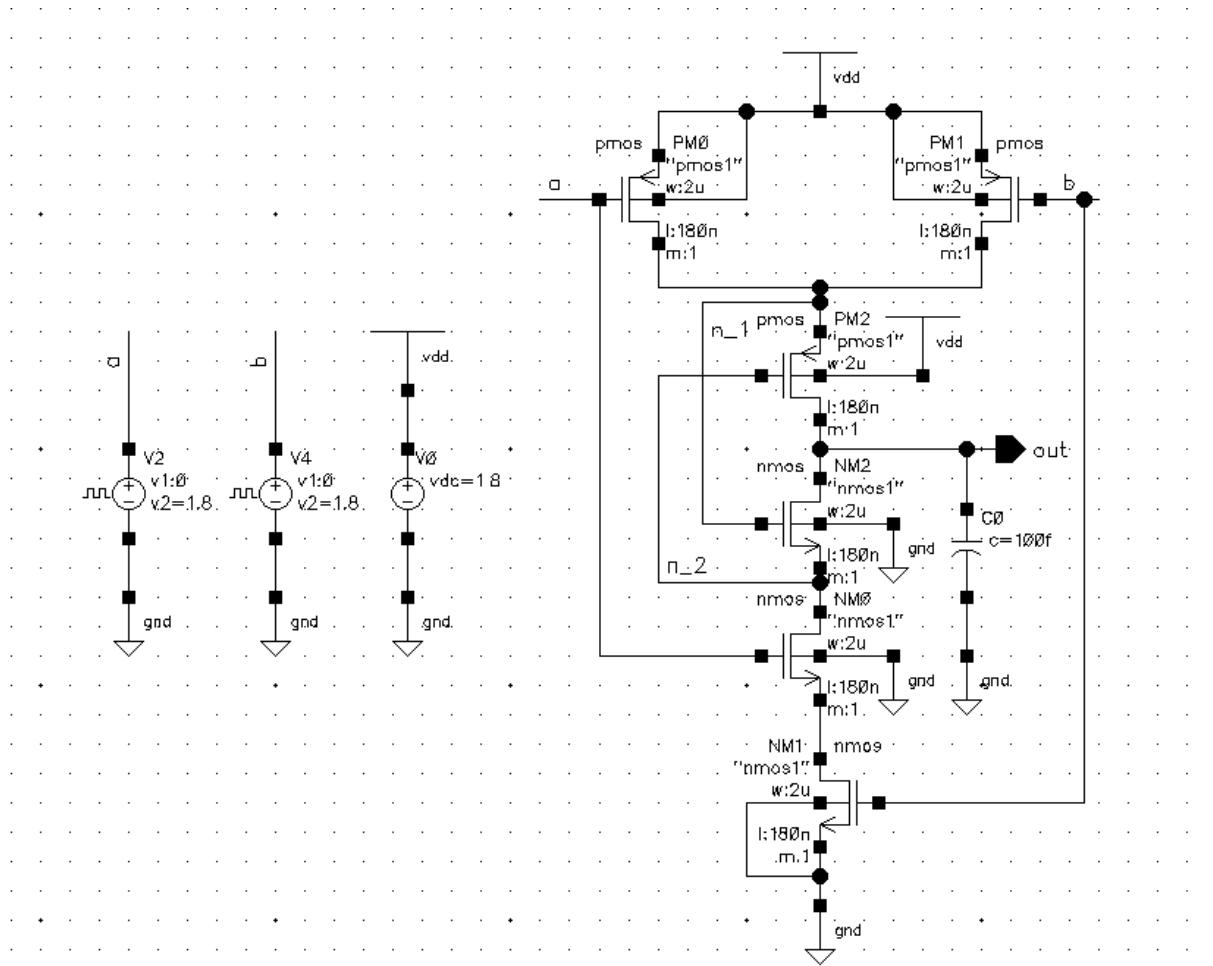
When NAND is made to function like an inverter, when ($A=B=0$) then output is high, leakage current flows through NMOS transistors.

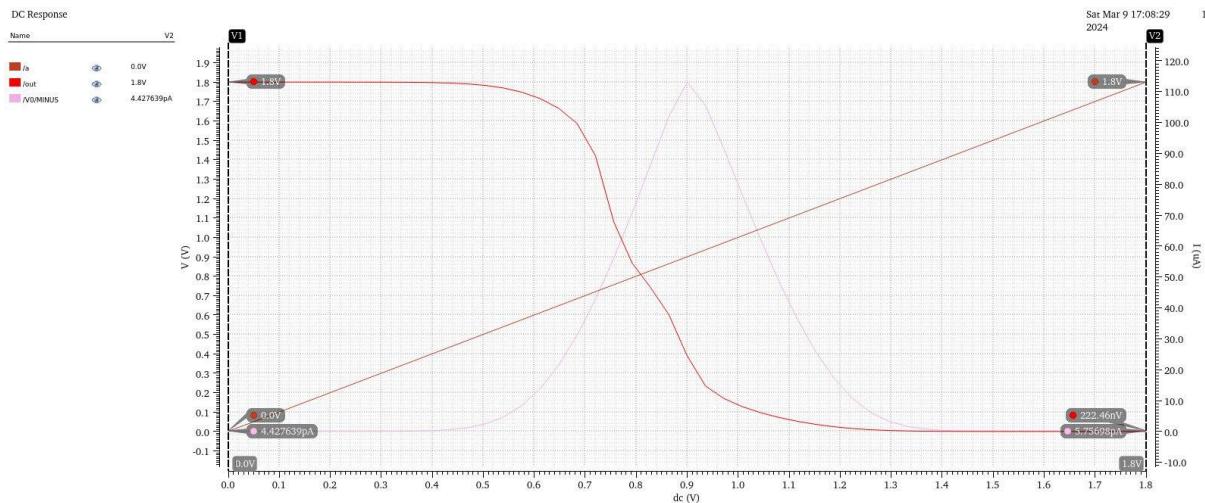
4. Artificial stacking – simulate function and leakage reduction compared to regular gate for

a) LECTOR inverter



b) LECTOR 2 input NAND gate

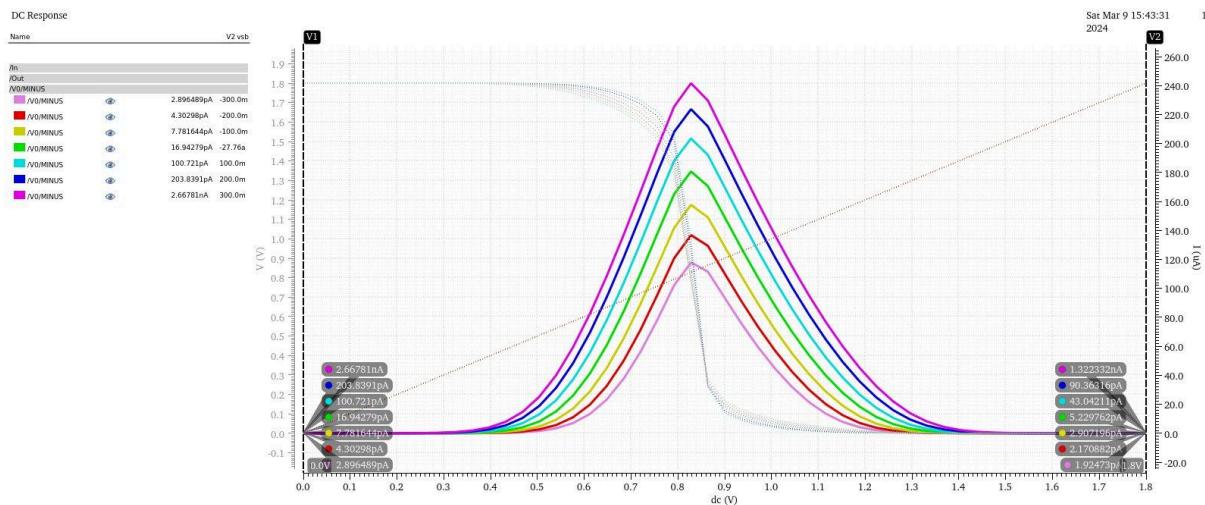
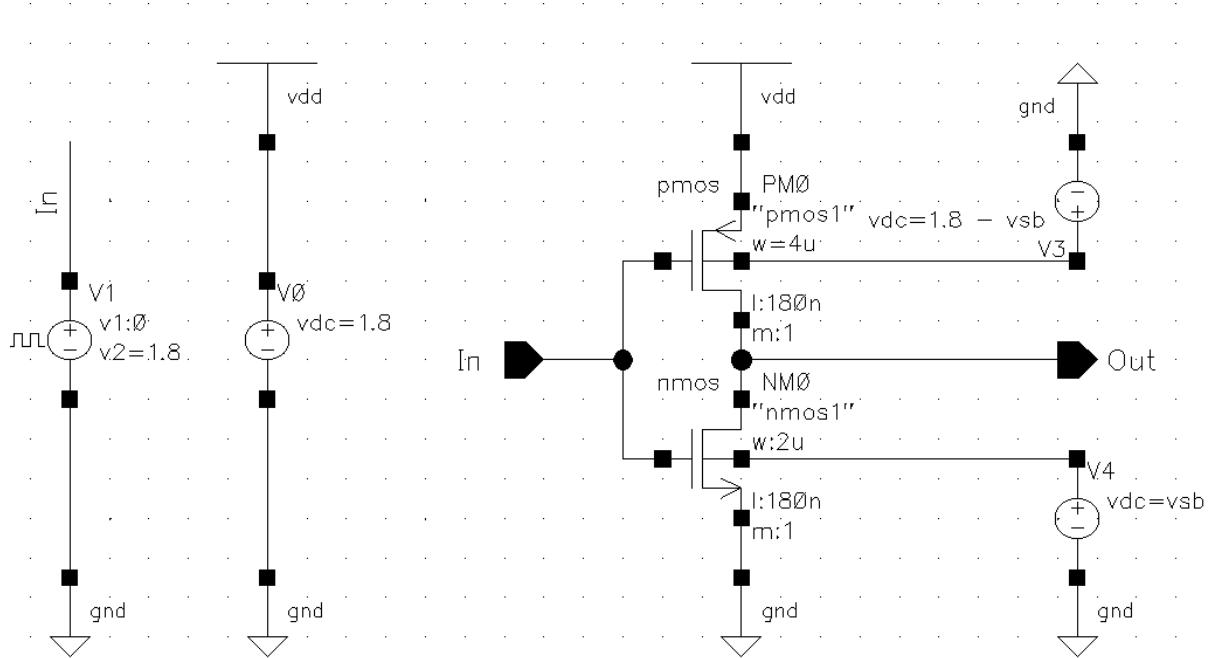




c) LECTOR 2 input NOR gate

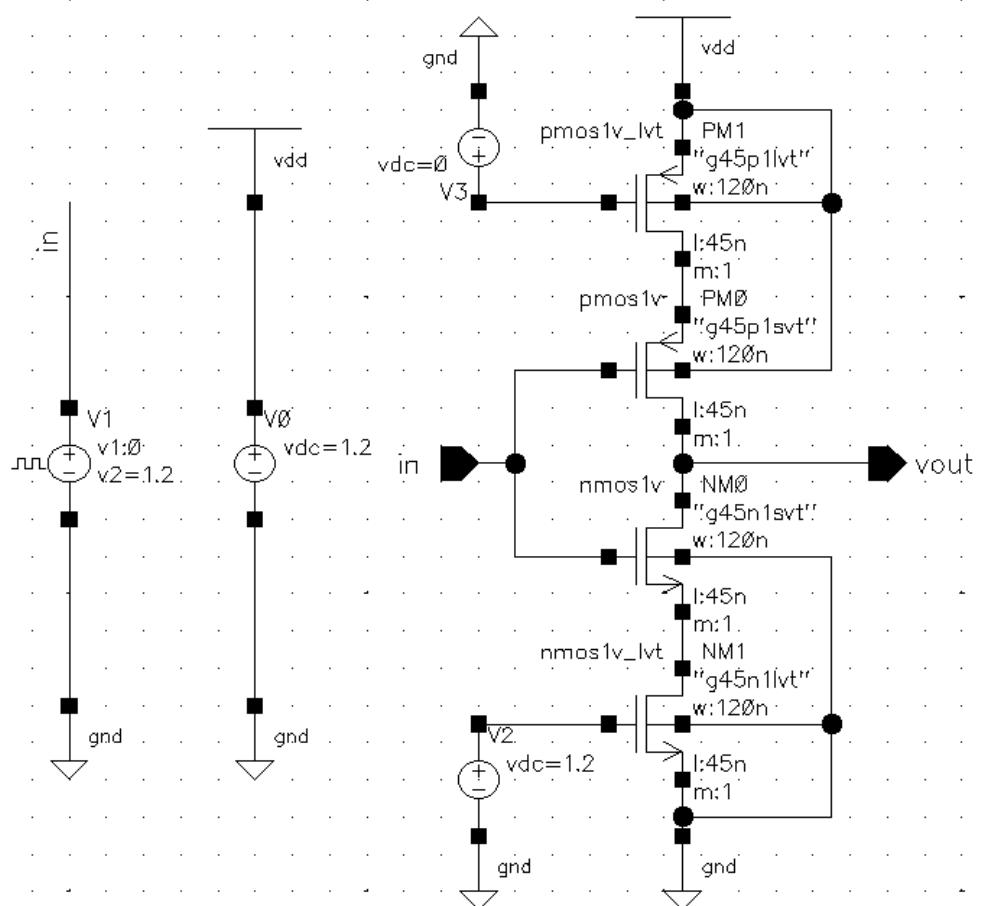
5. Multiple body biases - implement for inverter/NAND gate - check leakage for different Vsb.

NMOS				
VS	VB	VSB	Remark	
0	0	0	Normal	542m
0	-0.5	-0.5	More Reverse, VTH increase	668m
0	0.5	0.5	Reduce Reverse, VTH decrease	435m
PMOS				
VS	VB	VSB	Remark	
1.8	1.8	0	Normal	525m
1.8	1.8 - (-0.5)	-0.5	Increase Reverse, VTH decrease	682m
1.8	1.8 - (0.5)	0.5	Reduce Reverse, VTH increase	387m

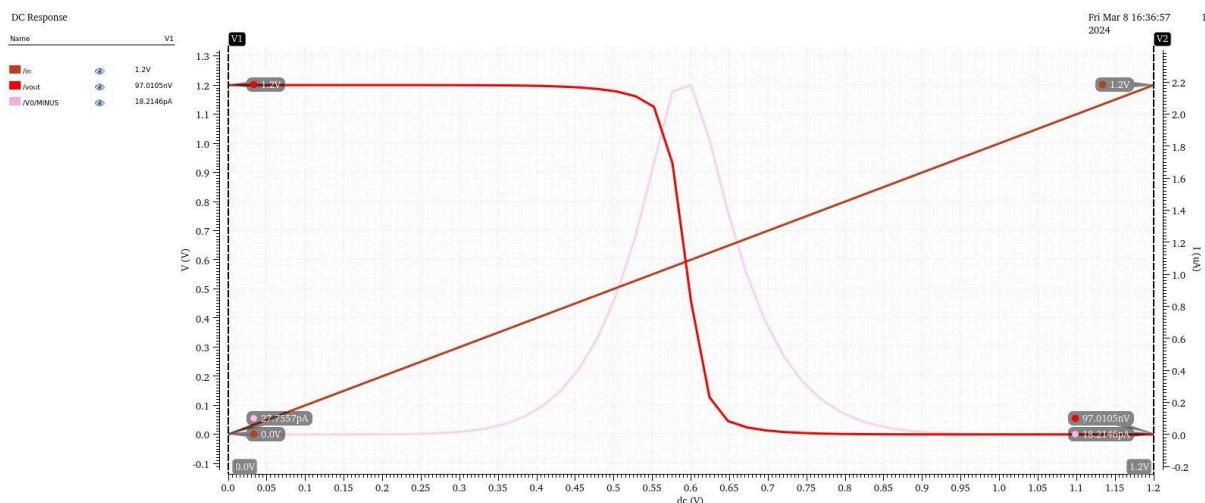


6. Super-cut off CMOS(SCCMOS) - check leakage for different gate biases in inverter/NAND gate.

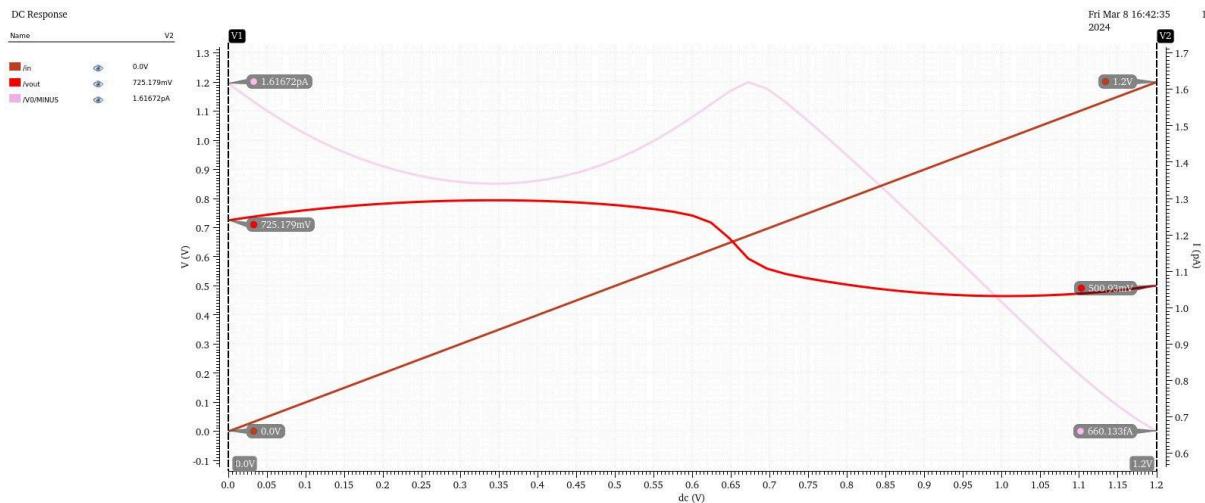
SCCMOS uses low VTH transistors with gate bias as sleep transistors.



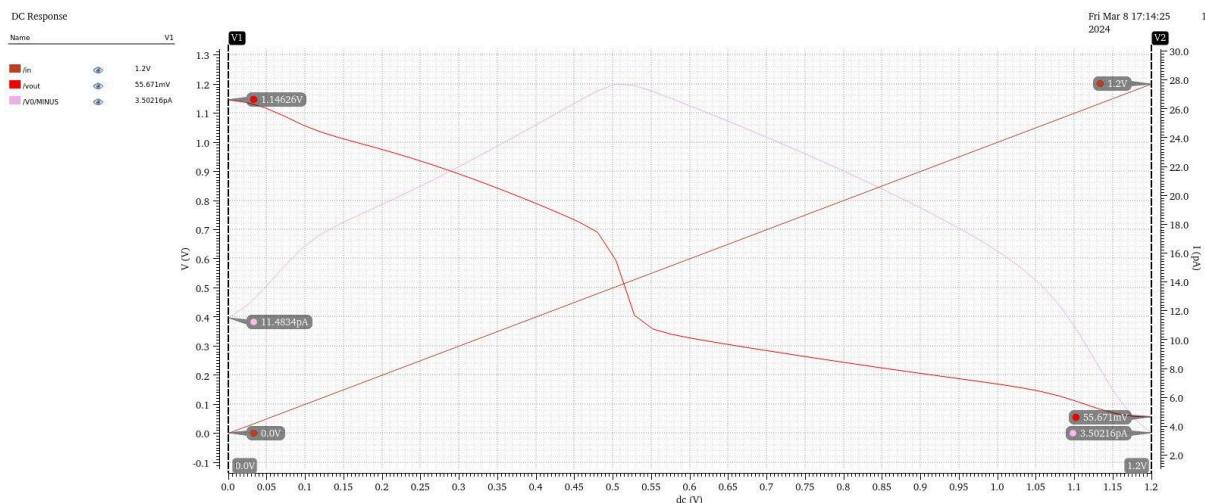
Active Mode: PMOS VG = 0, NMOS VG = VDD



Standby Mode: PMOS VG = VDD + 0.4, NMOS VG = VSS - 0.4



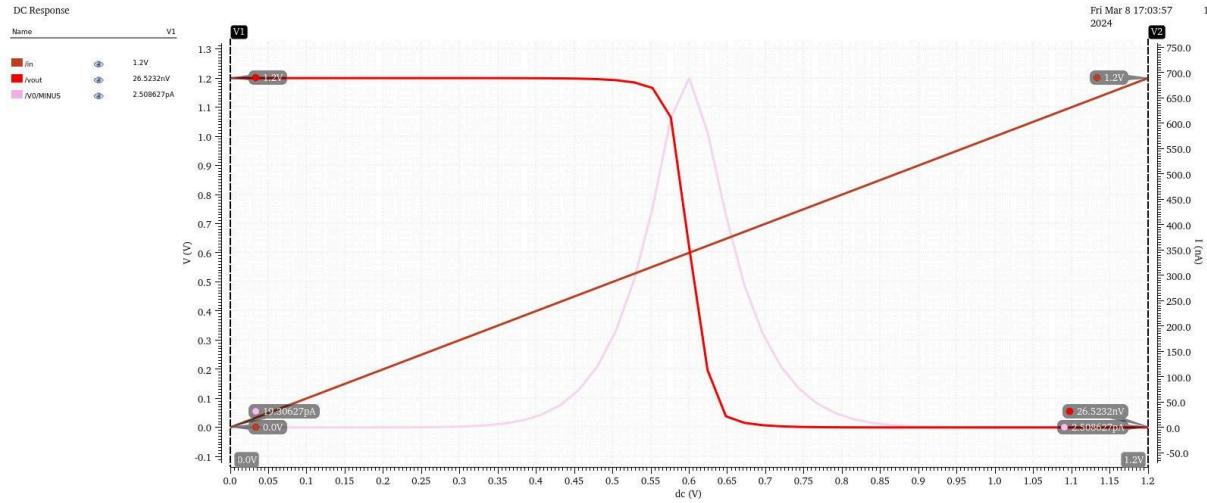
Normal Cutoff: PMOS VG = VDD, NMOS VG = 0



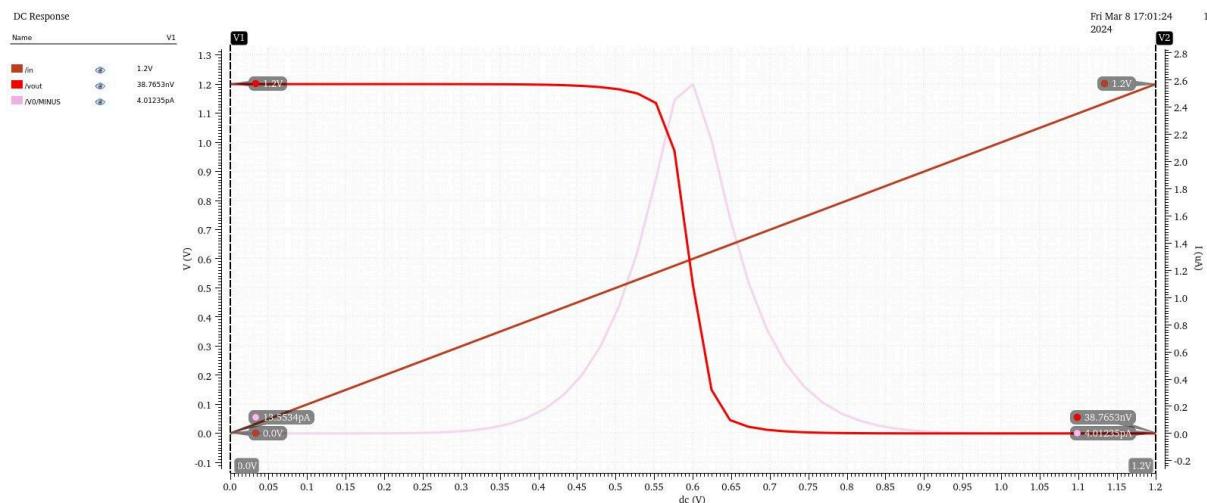
	Active Mode	Standby Mode (Super Cutoff)	Cutoff
NMOS Leakage	27.7p	1.6p	11.4p
PMOS Leakage	18.2p	660f	3.5p

GPKD 45 Inverter Effect of VTH on Leakage Current

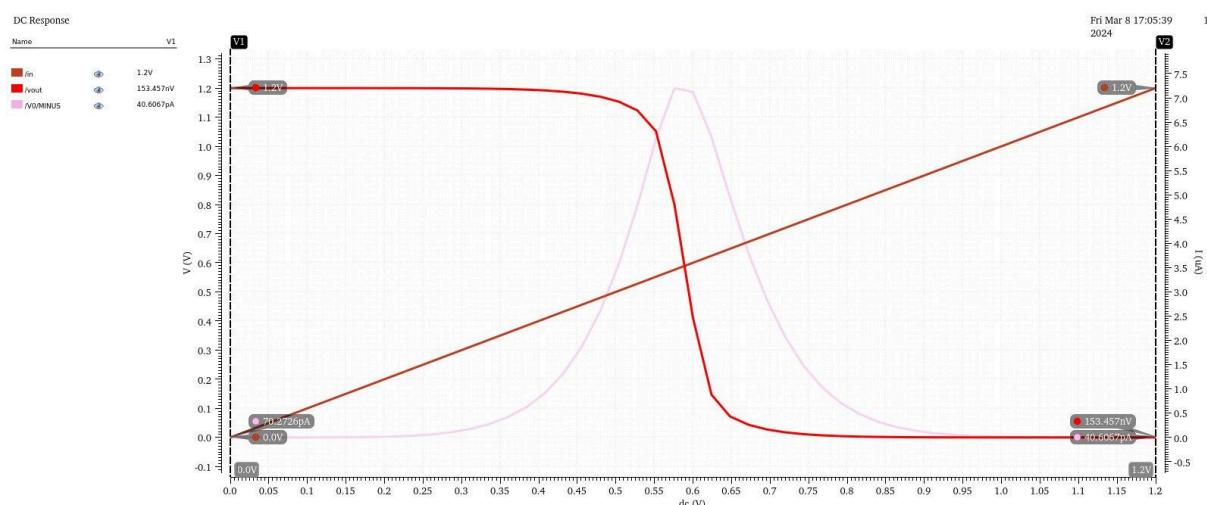
GPDK Inverter using High VT



GPDK Normal Inverter using Standard VT



Low VTH



	High VT	Standard VT	Low VT
PMOS VT	640m	565m	484m
NMOS VT	689m	586m	486m
PMOS Leakage	2.5p	4.0p	40.6p
NMOS Leakage	19.3p	13.5p	70.2p

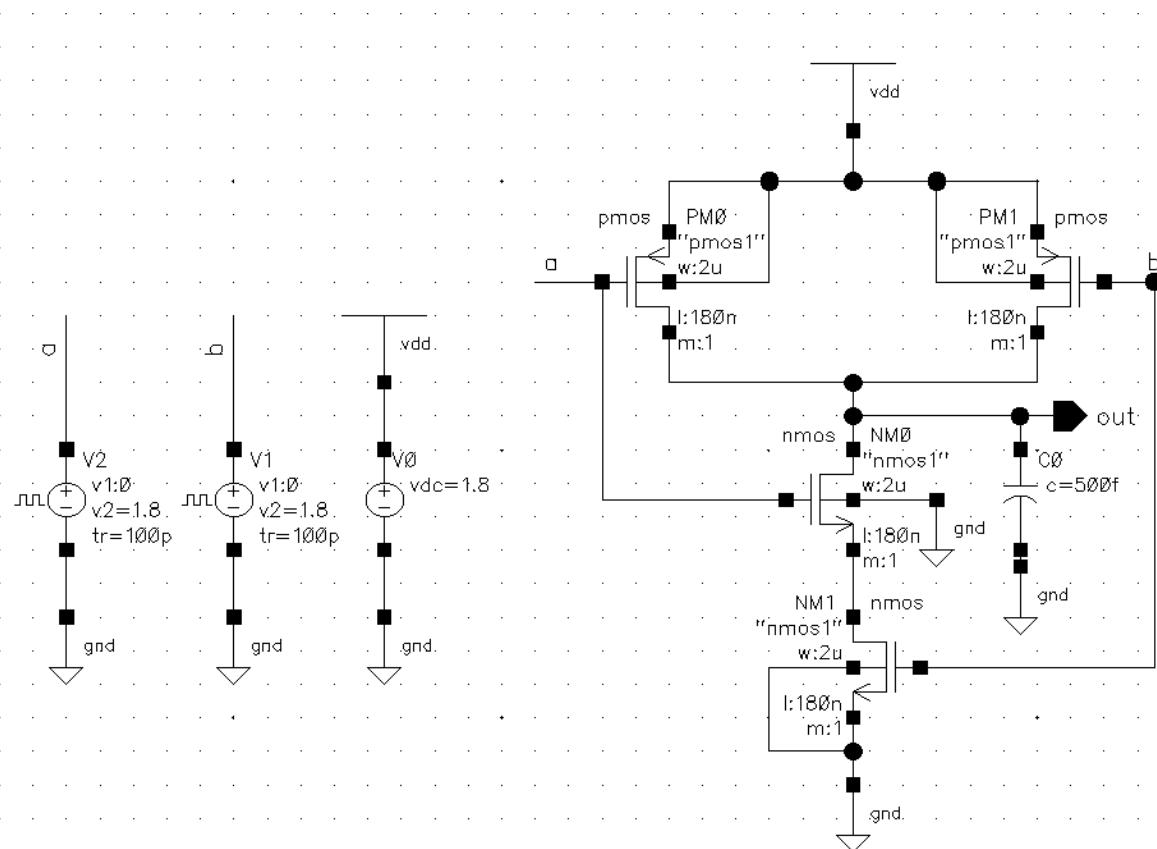
Glitch Power Dissipation

7. Plot glitch waveforms/power for a NAND gate, w.r.t. skew τ showing its dependency on the following.

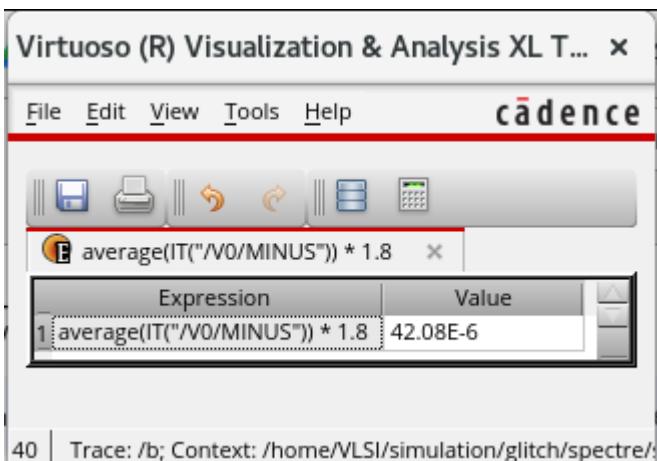
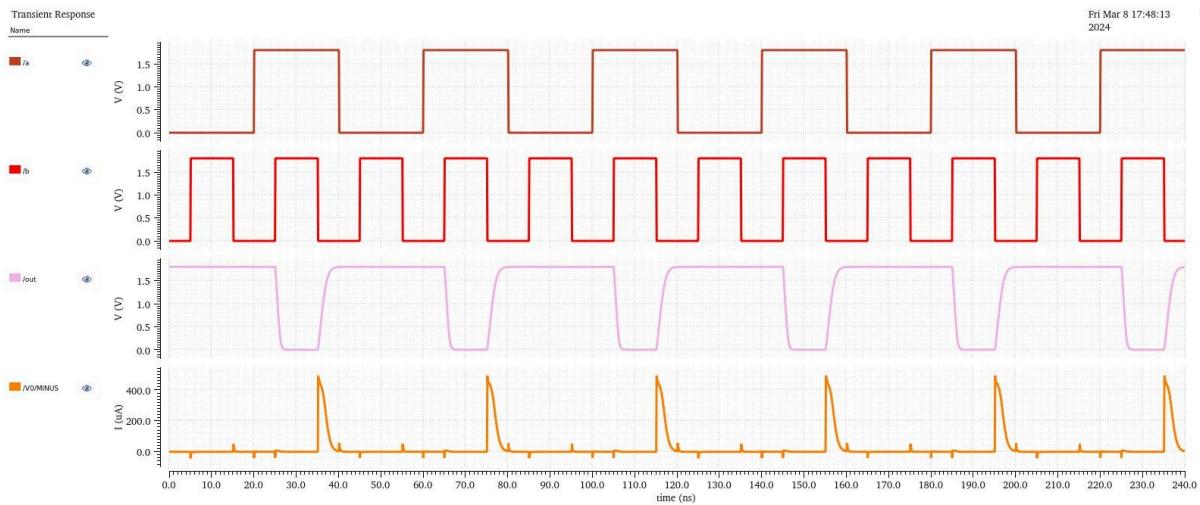
Glitch is an unwanted transition at the output due to skew in the inputs applied to the gate. Approximate power drawn during glitch is given by the below equation.

$$P_{glitch} = \frac{1}{T} \cdot C_{load} \cdot V_{dd} \cdot \sum_{i=1}^n \Delta V_i$$

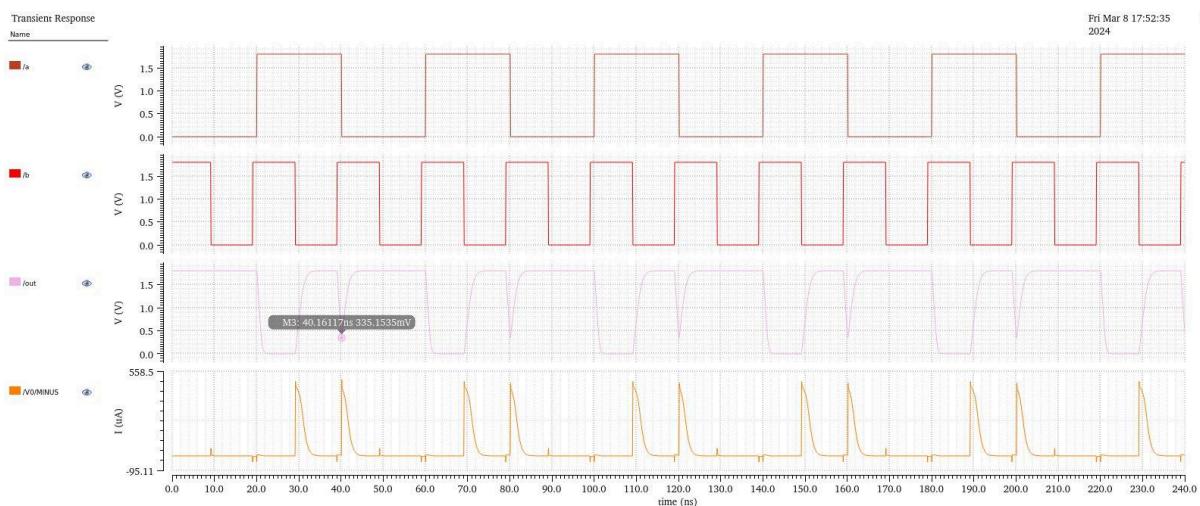
Where ΔV_i is the voltage swing of a sequence of n incomplete transitions within the period T.

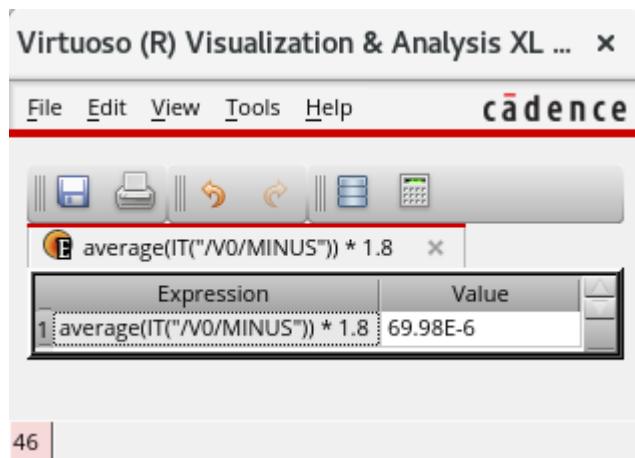


Without Glitch



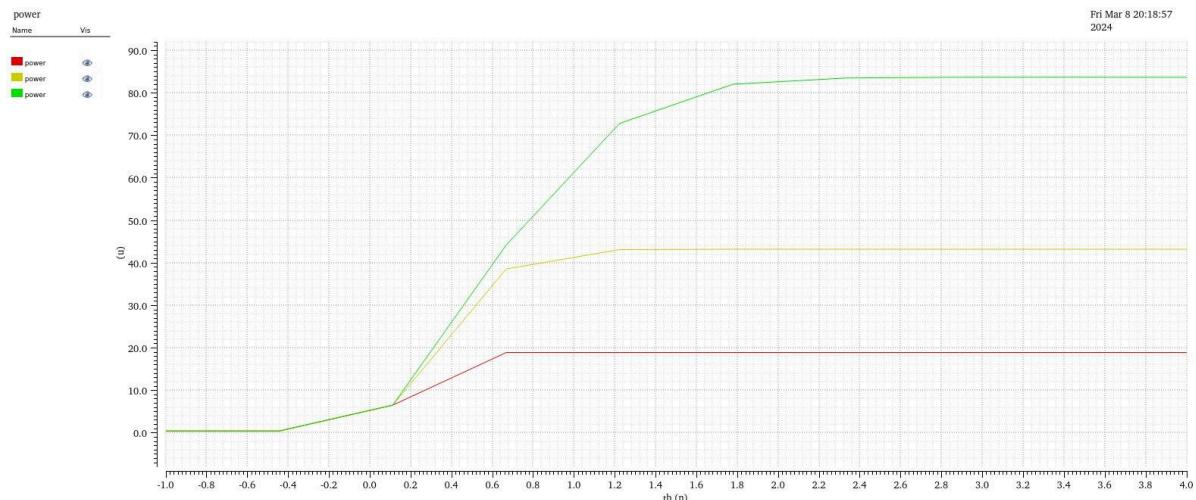
With Glitch





a. Output load

Add variable for capacitance as c.
 Change c manually 100f, 250f, 500f, 1000f
 Vary tb from -1n to 4n parametrically.
 Plot graph in append mode.



b. Input pattern

AB (10) -> (01)
 A Goes from 1 to 0
 B Goes from 0 to 1

Set Following parameters for A

Voltage 1: 1.8

Voltage 2: 0

Period: 40n
 Pulse Width: 20n
 Delay: 10n + ta
 Rise Time: 100p

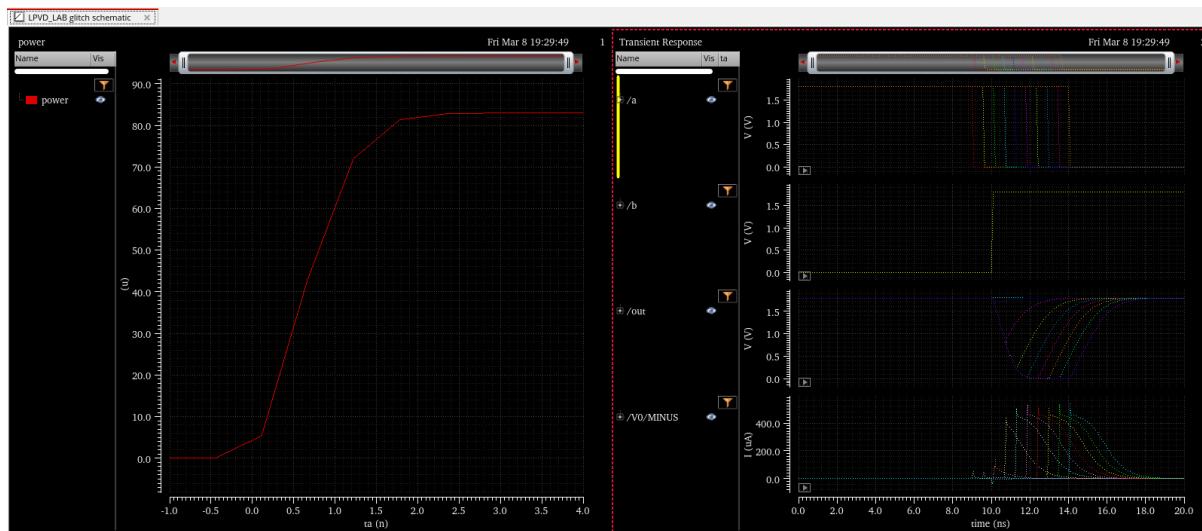
Set Following parameters for B

Voltage 1: 0
 Voltage 2: 1.8
 Period: 40n
 Pulse Width: 20n
 Delay: 10n + tb
 Rise Time: 100p

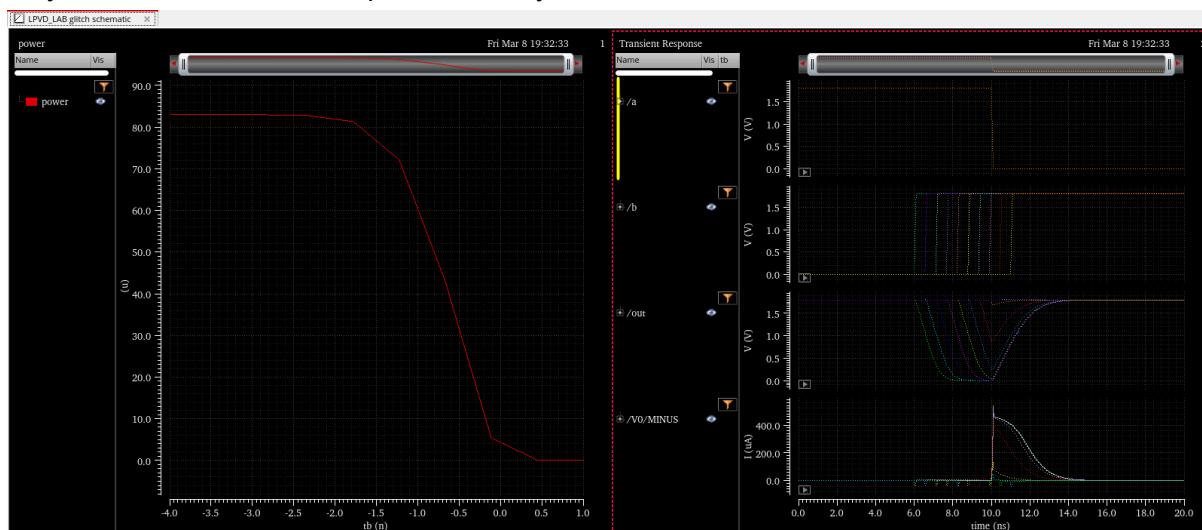
Set up transient analysis for 20n (Half Cycle)

Run transient analysis, add power equation to plot

Vary skew ta from -1n to 4n parametrically



Vary skew tb from -4n to 1n parametrically



AB (01) -> (10)

A Goes from 0 to 1

B Goes from 1 to 0

Set Following parameters for A

Voltage 1: 0

Voltage 2: 1.8

Period: 40n

Pulse Width: 20n

Delay: 10n + ta

Rise Time: 100p

Set Following parameters for B

Voltage 1: 1.8

Voltage 2: 0

Period: 40n

Pulse Width: 20n

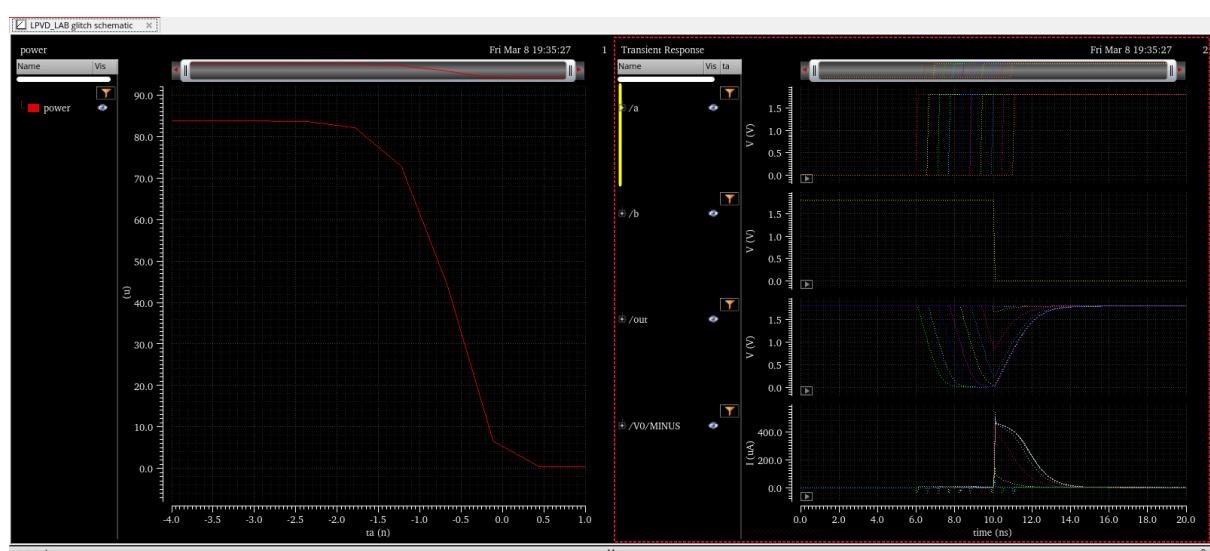
Delay: 10n + tb

Rise Time: 100p

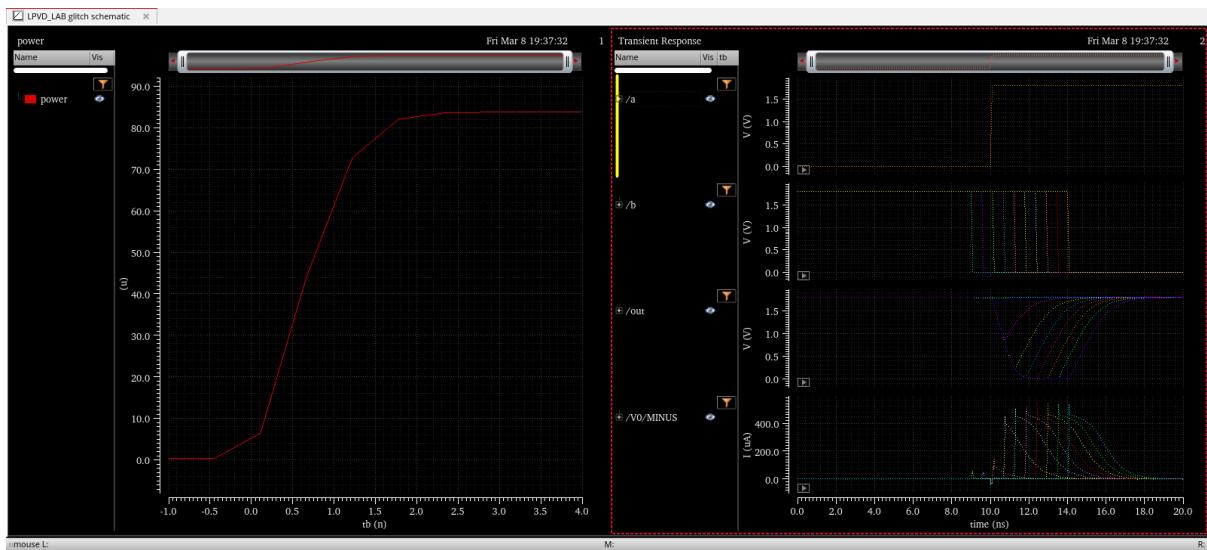
Set up transient analysis for 20n (Half Cycle)

Run transient analysis, add power equation to plot

vary skew ta from -4n to 1n parametrically

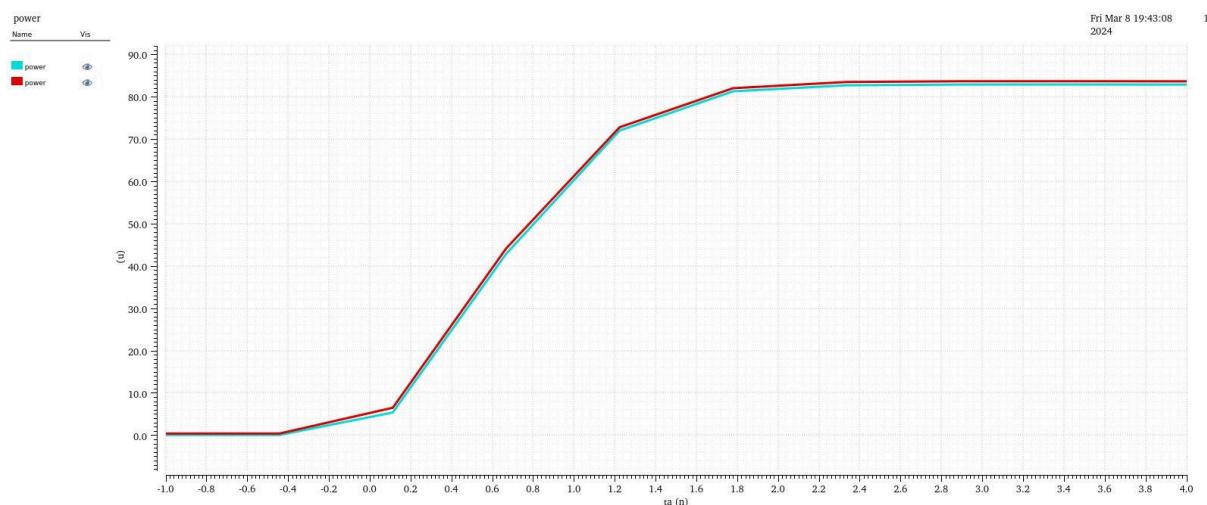


vary skew tb from -1n to 4n parametrically



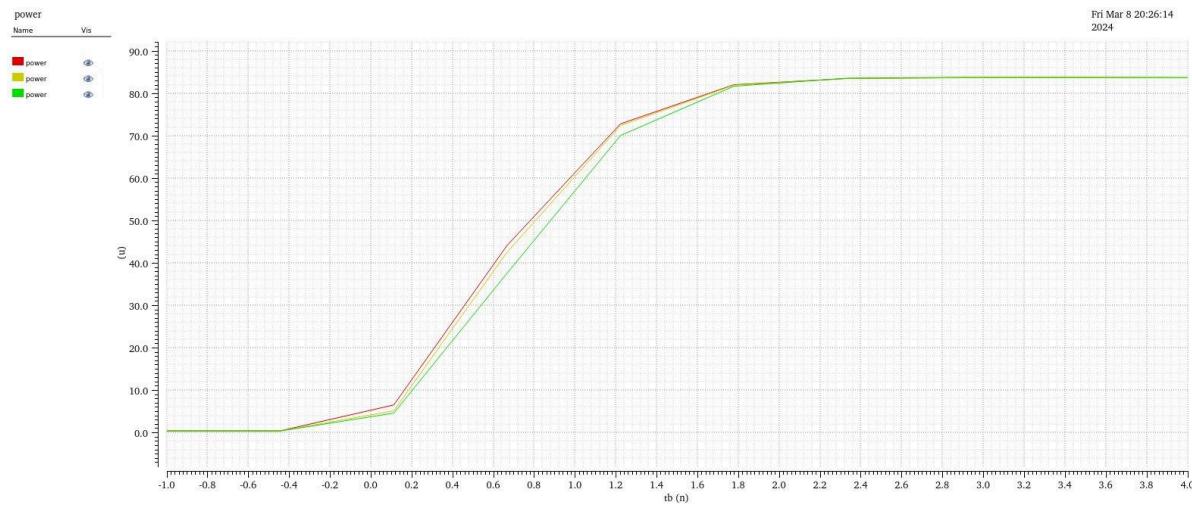
Append Case 1 and Case 4

AB (10) \rightarrow (01) - lower
AB (01) \rightarrow (10) - higher



c. Input slope

Add variables for rise time of A and B as tr.
Change tr manually 100p, 200p, 500p,
Vary tb from -1n to 4n parametrically.
Plot graph in append mode.

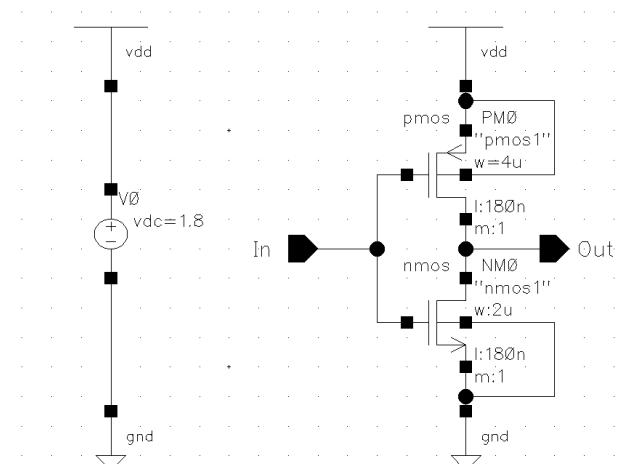


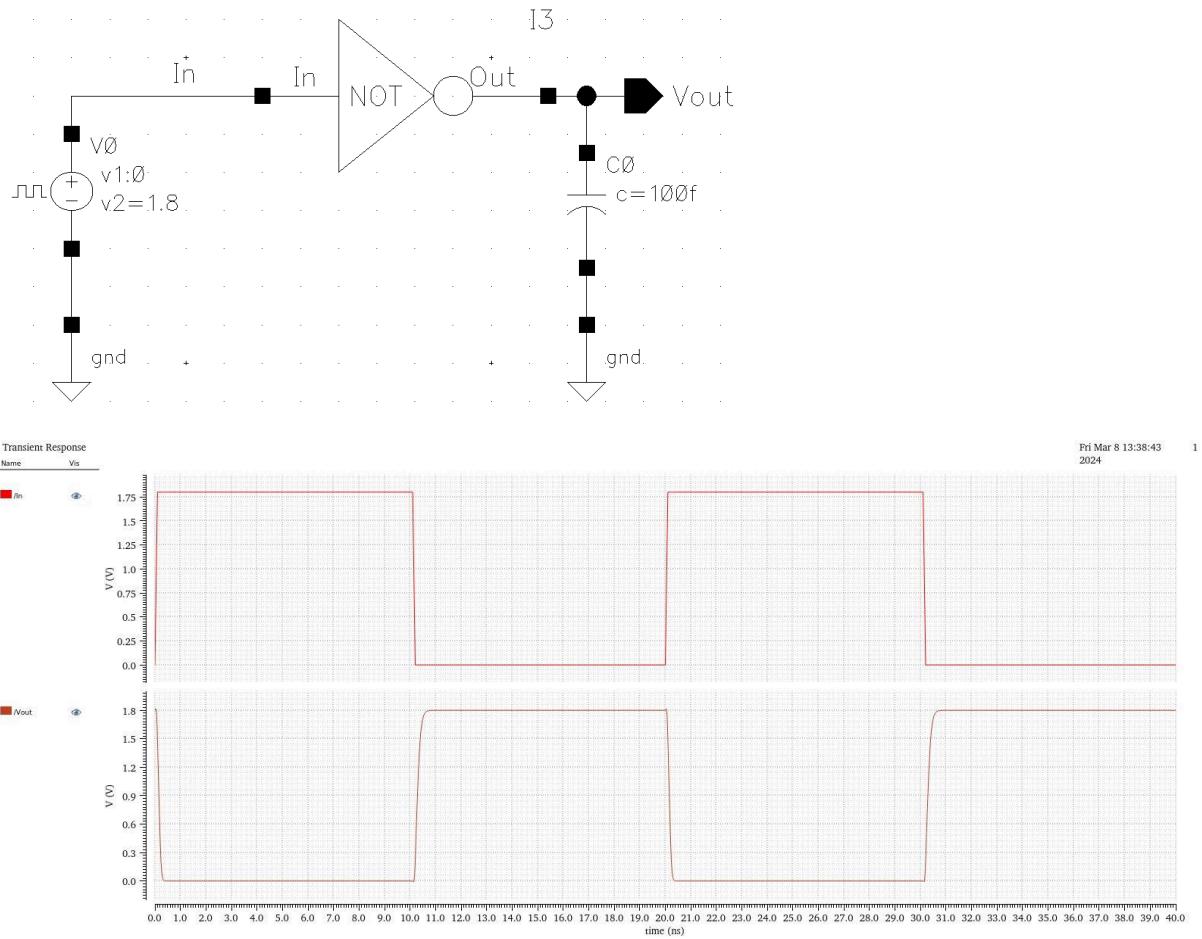
8. Design and simulate latch based clock gating circuits for the following blocks:

a. 8 bit shift register

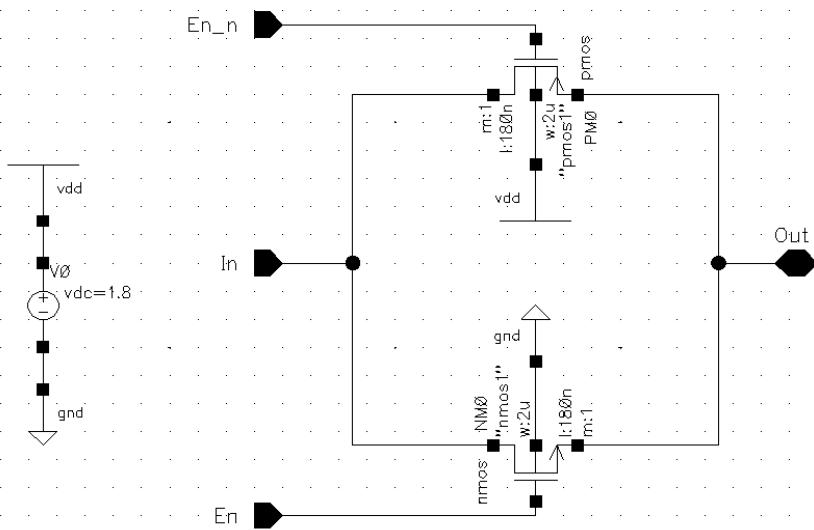
b. 4 bit synchronous counter

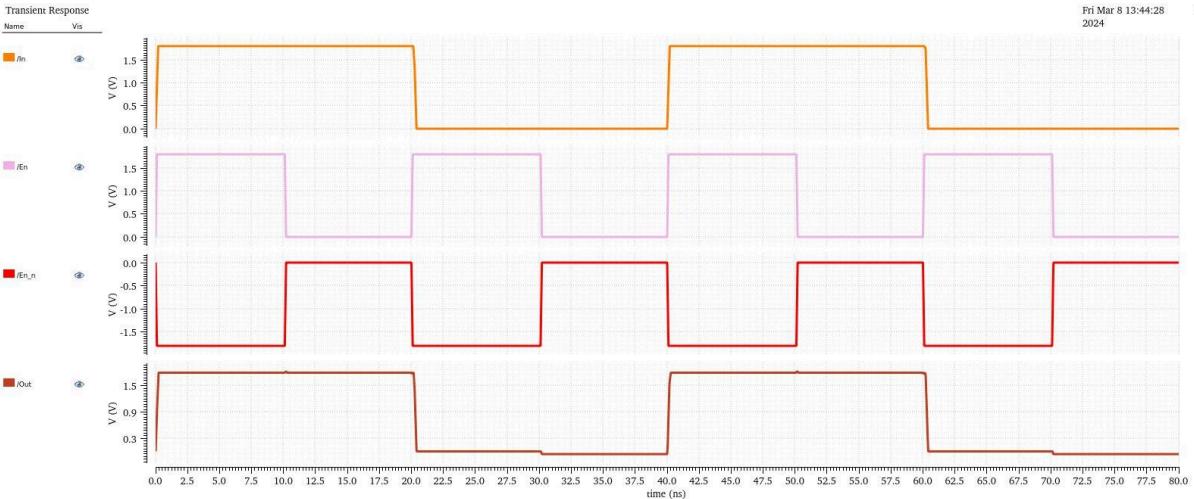
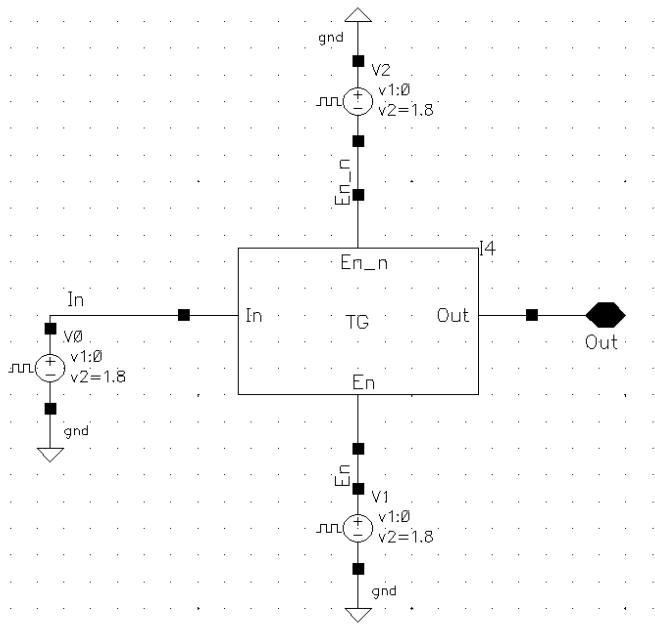
1. Design Inverter



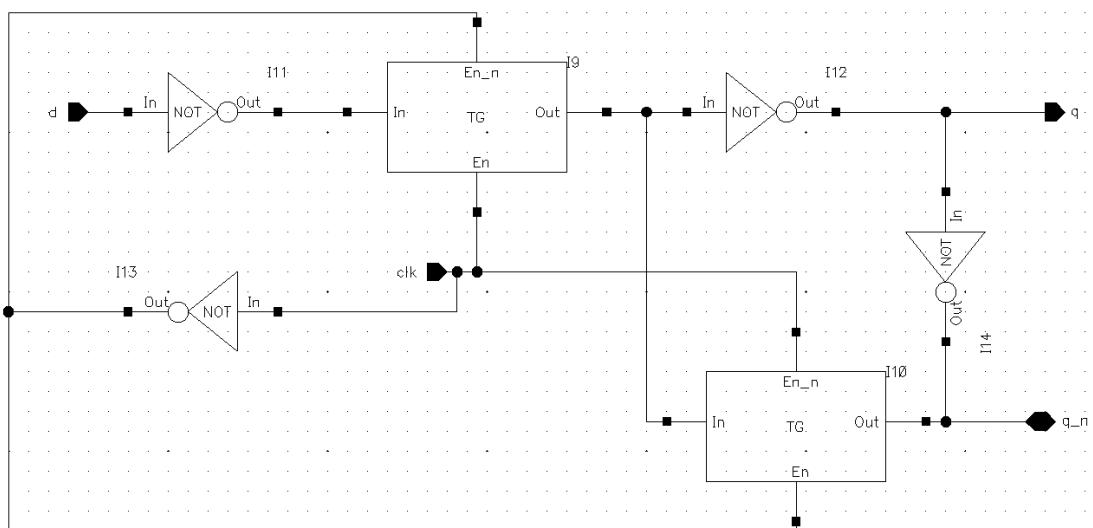


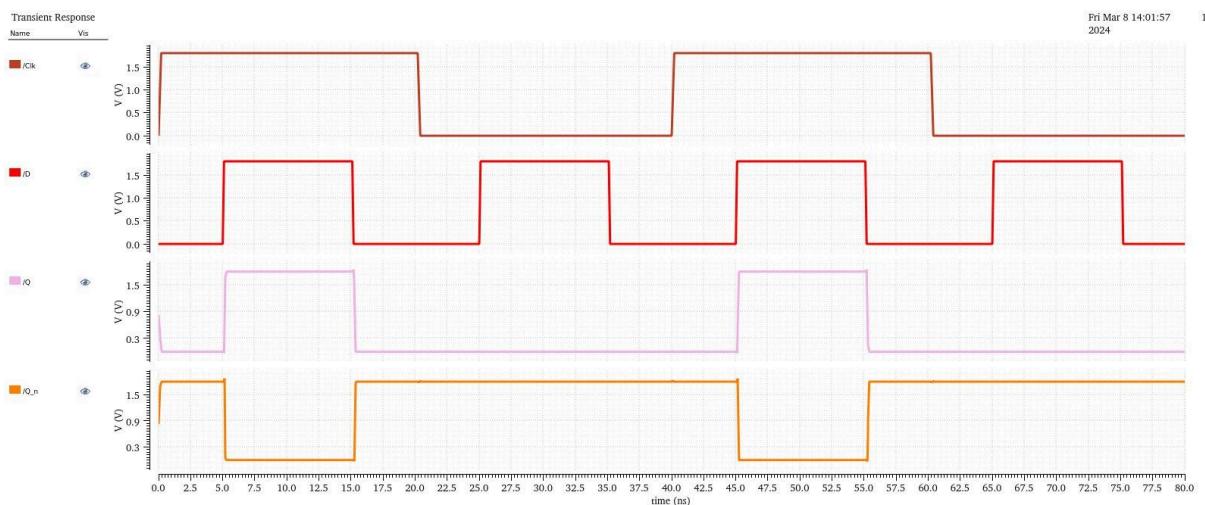
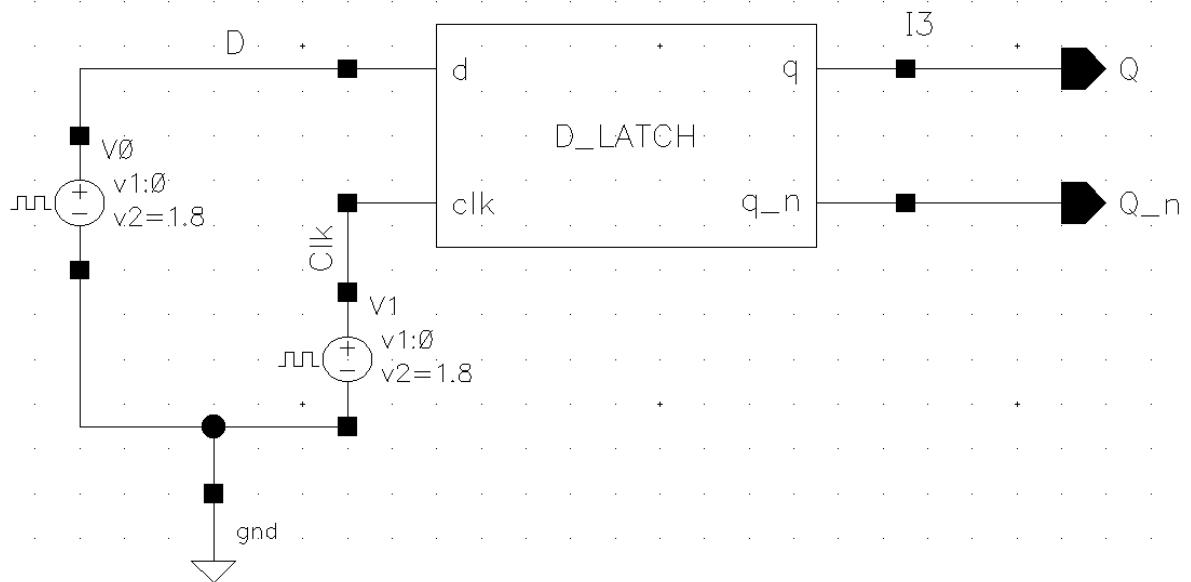
2. Design Transmission Gate



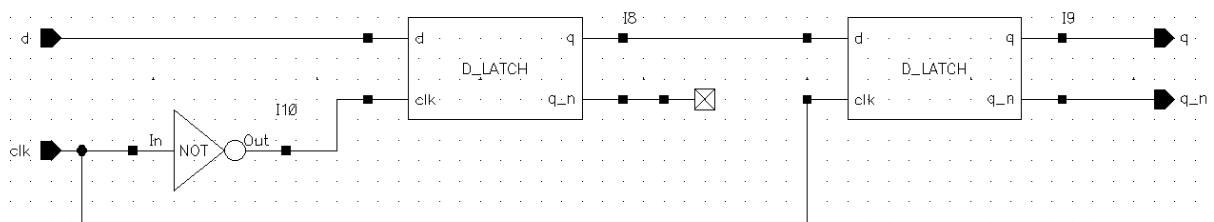


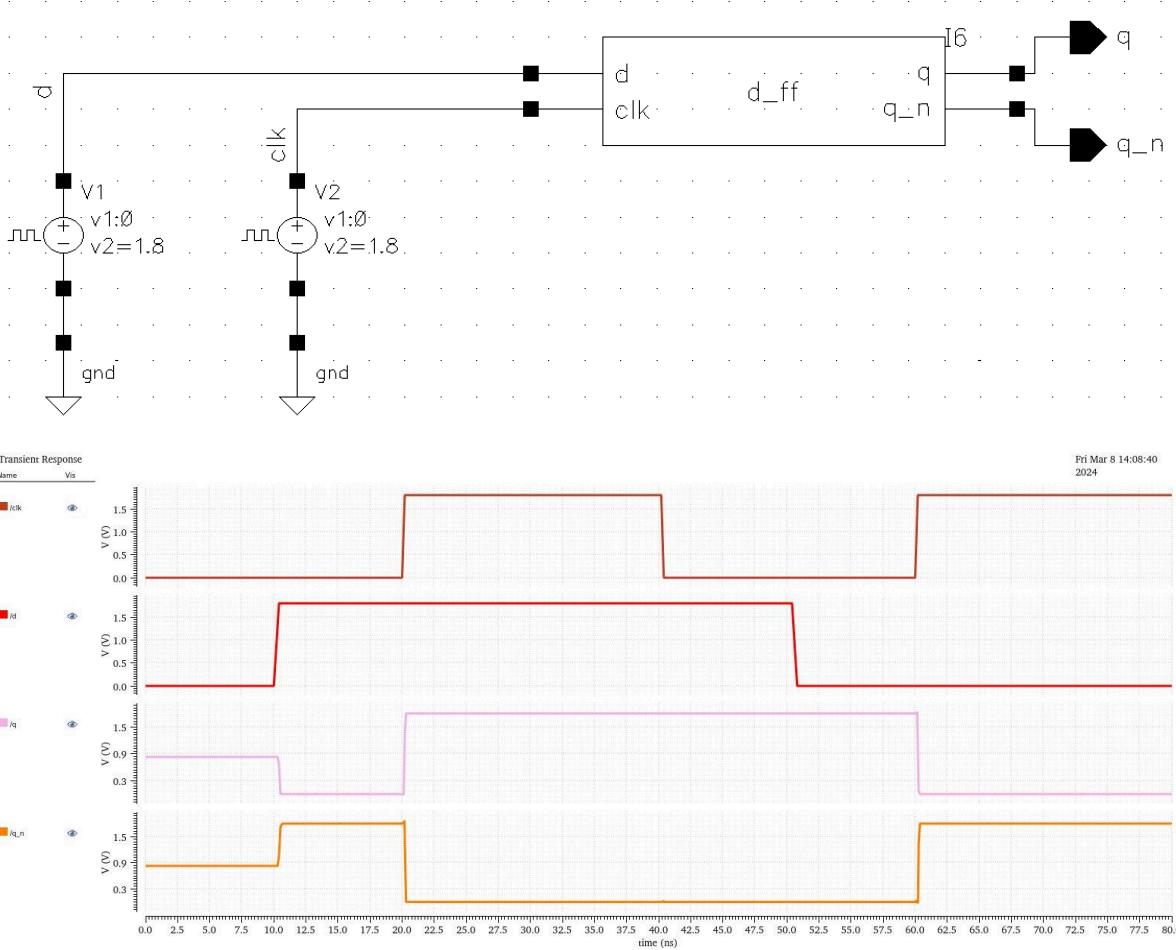
3. Design D Latch





4. Design D Flip Flop





5. Design XOR Gate
 6. Design T Flip Flop
 7. Design AND Gate
 8. Design Synchronous Counter
9. Design the following Level shifter circuits. Assume your own VDDH and VDDL values.
- a. High to low voltage
 - b. Low to high voltage
10. Apply possible low power techniques you have learnt in the course and design any low power digital module (either RTL or transistor level), compare the power and other parameters with and without low power design techniques.