# MPCA Lab: working on Pipeline and Cache simulator

**Task1:**
**5 stage pipeline Simulator.**
**Link :** MIPS Five Stage Pipeline (umass.edu)

Consider the following instructions. Execute these instructions using 5 stage pipeline - MIPS architecture simulator.

```
ADD  R0, R1, R2
SUB   R3, R0, R4
FP_LOAD F1, Offset,R1
FP_ADD F5,F1,F1
```

Observe the following and note down the results.
Check whether there is data dependency among the instructions?

-If yes, then, how many stall states have been introduced?
-If data forwarding is applied how many stall states have been reduced?
-Mention the total number of clock cycles used with and without data forwarding.

**Task2:**
**Cache Simulator:**
**Link:** ParaCache Main Menu (ntu.edu.sg)

1. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

(a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address using direct mapped Cache.

(b) When a program is executed, the processor reads data sequentially from the following word addresses:
128, 144, 2176, 2180, 128, 2176
All the above addresses are shown in decimal values (Convert the address to hexadecimal equivalent of the decimals given above and submit in the simulator). Assume that the cache is initially empty.
For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

2. For the above mentioned problem, calculate and execute for 4way set associativity and fully associative mapping technique. For each technique

randomly generate ten addresses and indicate whether the cache access will result in a hit or a miss. Assume block replacement policy as random.

**Task3:**
**Use Arm Simulator**

Given a ‘c’ code convert it in its equivalent Arm Code and execute in ARM simulator

1) x = (a + b) - c
2) z = (a << 2) | (b & 15)

Note: For all above three tasks show the calculation if any, write the code if any and paste the screenshot of the output.