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1. Introduction

In the ever-evolving landscape of microprocessor design, the quest for faster, more energy-efficient, and compact arithmetic operations remains an ongoing challenge. Among these operations, binary addition stands as a cornerstone, serving as the backbone for numerous computational tasks, including cryptography, parallel processing, and digital signal processing. Traditional approaches to wide adder implementation, typified by Ripple Carry Adders (RCA), often grapple with inherent limitations stemming from carry propagation delays, driving the exploration of alternative methodologies.

In this context, the Carry Look-Ahead (CLA) adder architecture emerges as a compelling solution, harnessing parallel computation to circumvent the delays associated with carry propagation. Within the domain of CLA design, the optimization of 4-bit CLA processes assumes paramount importance, given their pivotal role in wider adder configurations. While extant research has predominantly focused on algorithmic and logical interpretations of CLA techniques, a conspicuous gap persists in transistor-level representations tailored explicitly for 4- bit CLA architectures.

Addressing this gap, our project endeavors to develop a transistor-level static CMOS logic-based CLA process meticulously optimized for 4-bit addition. Diverging from conventional paradigms reliant on carry-propagate and carry-generate signals, our proposed CLA design streamlines the carry-out computation process, holding the promise of substantial improvements in speed, power consumption, and overall performance. Through exhaustive simulation and validation utilizing industry-standard design tools and cutting-edge technology nodes, we endeavor to showcase the efficacy and viability of our proposed 4-bit CLA architecture as a transformative solution for high-performance data-path design in contemporary microprocessors.

2. Objectives

i. Develop a novel 4-bit Carry Look-Ahead Adder (CLA) design in static CMOS logic.

ii. Enhance performance metrics such as average power consumption, propagation delay, and power delay product (PDP).

iii. Eliminate traditional carry-generate and carry-propagate terms to improve efficiency.

iv. Compare the proposed design with conventional approaches to demonstrate speed and power consumption improvements.

3. Block Diagram

PROPOSED 4-BIT CARRY LOOK-AHEAD ADDER IN STATIC CMOS LOGIC

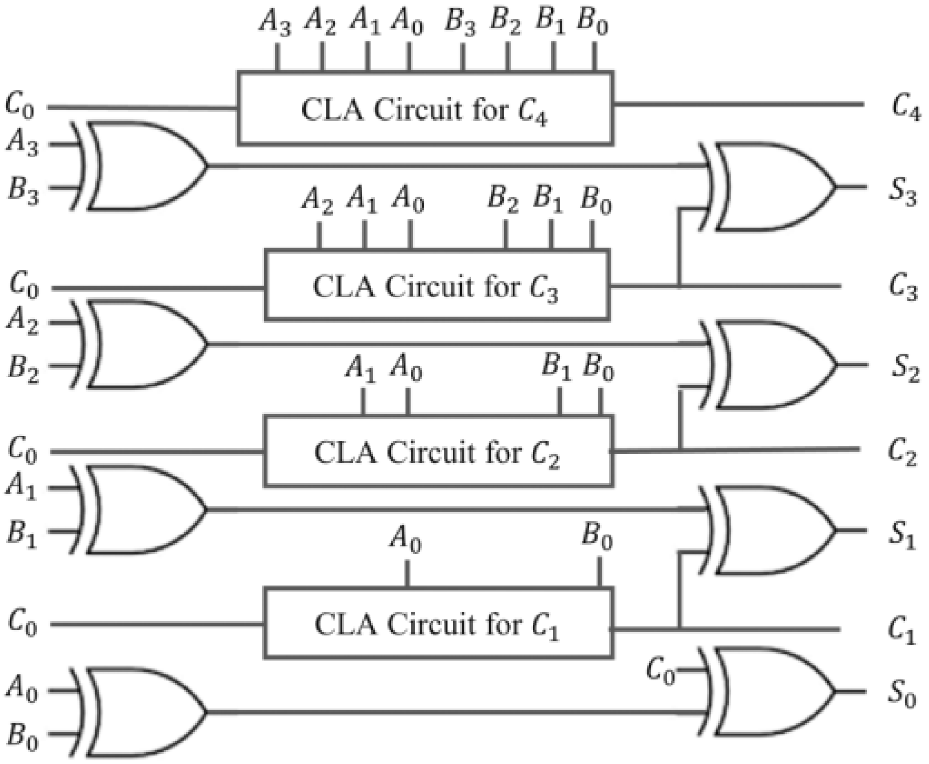


Fig 1- Logic gate level representation of proposed static CMOS CLA adder

The figure illustrates the logic gate level representation of the proposed static CMOS CLA adder. It showcases the design methodology for computing carry-out bits without using traditional Pi and Gi terms. The diagram visually represents the innovative approach that directly utilizes input bits for carry generation, enhancing speed and efficiency. This representation highlights the shift in design strategy towards optimizing performance metrics in static CMOS logic.

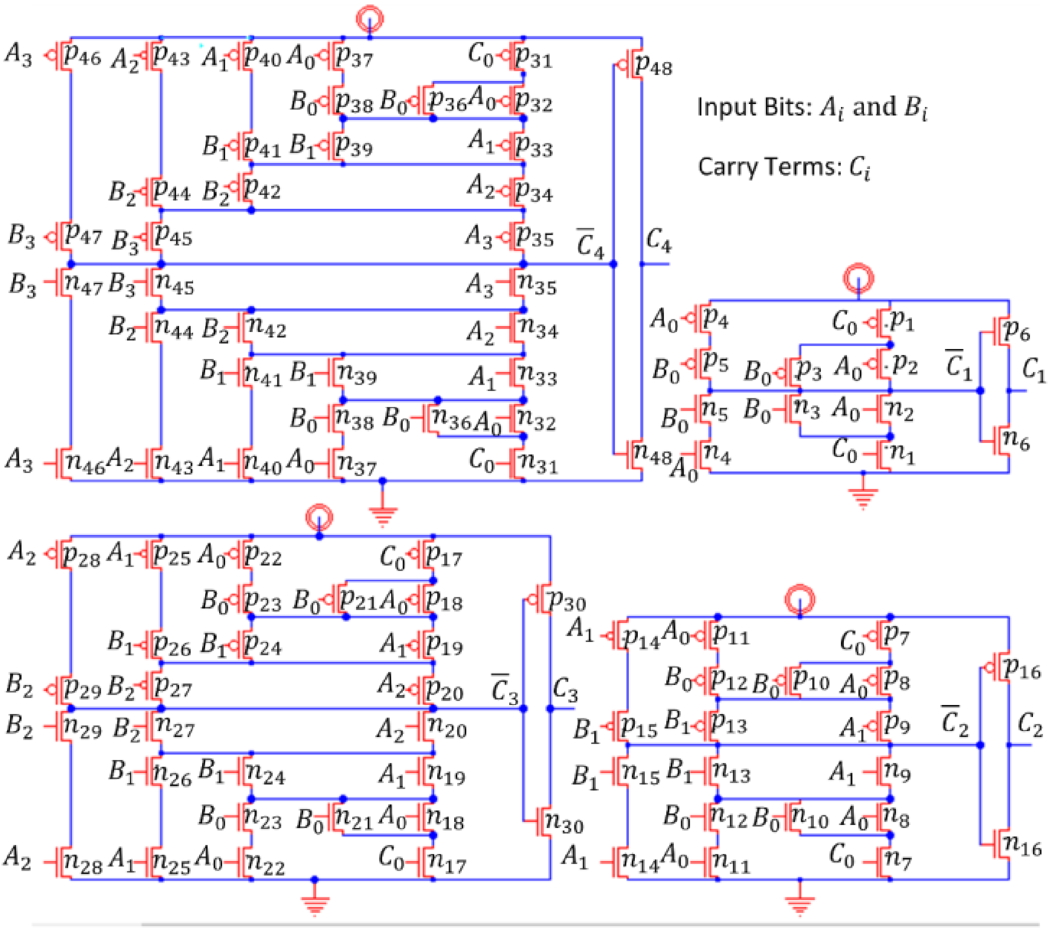
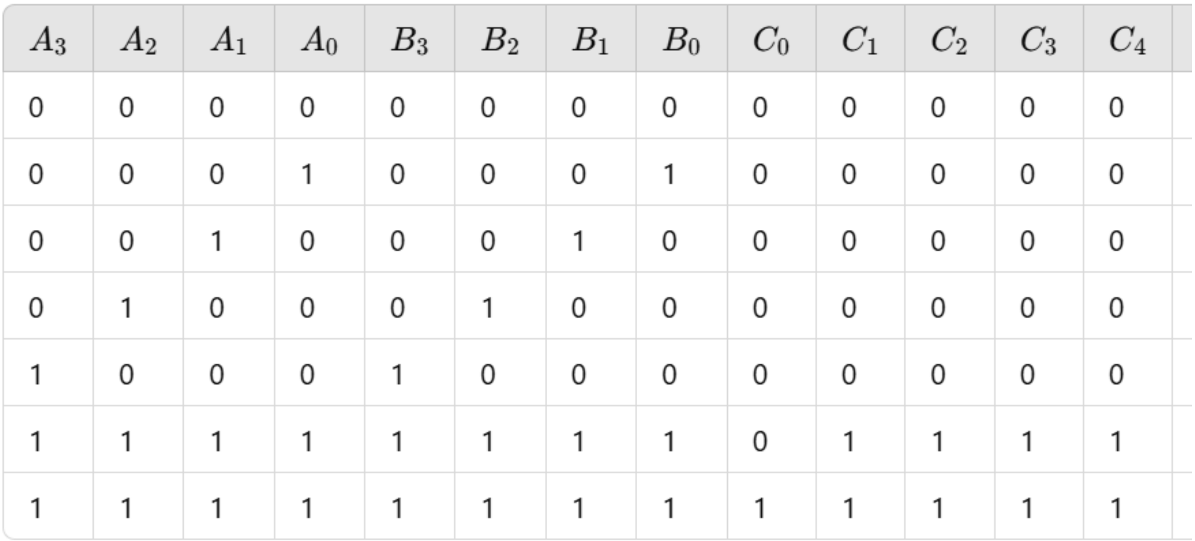


Fig 2- Transistor level representation of proposed static CMOS CLA circuits for carry-out bits.

The proposed CLA technique calculates carry-out bits without using the conventional carry-propagate (Pi) and carry-generate (Gi) terms. Instead, it uses all input bits directly in the CLA circuits for carry generation. While the sum generation process remains the same as the conventional design, the carry-out bits are derived from simplified Boolean equations involving input bits Ai, Bi, and C0. This new approach involves creating NMOS and PMOS networks based on these equations to generate the carry-out bits. The NMOS networks for each carry-out bits C1, C2, C3, and C4 are built step-by-step, with PMOS networks mirroring the NMOS networks to ensure full swing outputs. Inverters are added to achieve the desired output. The sum generation still uses XOR gates for Pi and Ci signals, maintaining consistency with the traditional design.



A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_0	C_1	C_2	C_3	C_4
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1

Fig 3- Truth Table of the CLA

Above is a truth table for a 4-bit Carry Look-Ahead Adder (CLA) based on the simplified Boolean equations provided. This table includes the input bits Ai, Bi, and C0 (the initial carry-in), and shows the resulting carry-out C1, C2, C3, and C4. This table illustrates a few sample cases to demonstrate the concept.

4. Methodology

The design methodology in the proposed static CMOS CLA adder involves a unique approach to computing carry-out bits without relying on conventional Pi and Gi terms. Here is a detailed description of the design methodology:

1. **Carry Generation Process**: The design directly utilizes input bits for carry generation, simplifying the process and reducing the dependency on additional signals like Pi and Gi terms.
2. **Logic Gate Implementation**: By using XOR gates and other logic gates, the design efficiently computes the carry-out bits based on the input signals, optimizing the circuit for speed and efficiency.
3. **Streamlined Operation**: The methodology streamlines the carry generation process, eliminating unnecessary steps and improving the overall performance of the static CMOS CLA adder.
4. **Efficiency Enhancement**: This design methodology focuses on enhancing efficiency by minimizing the complexity of the carry generation process and maximizing the speed of operations within the static CMOS logic circuits.

Overall, the design methodology of the proposed static CMOS CLA adder emphasizes simplicity, efficiency, and performance optimization in carry-out bit computation.

The circuits below shows the CMOS designs of the consecutive circuits of C1, C2, C3 and C4 carry out bits.

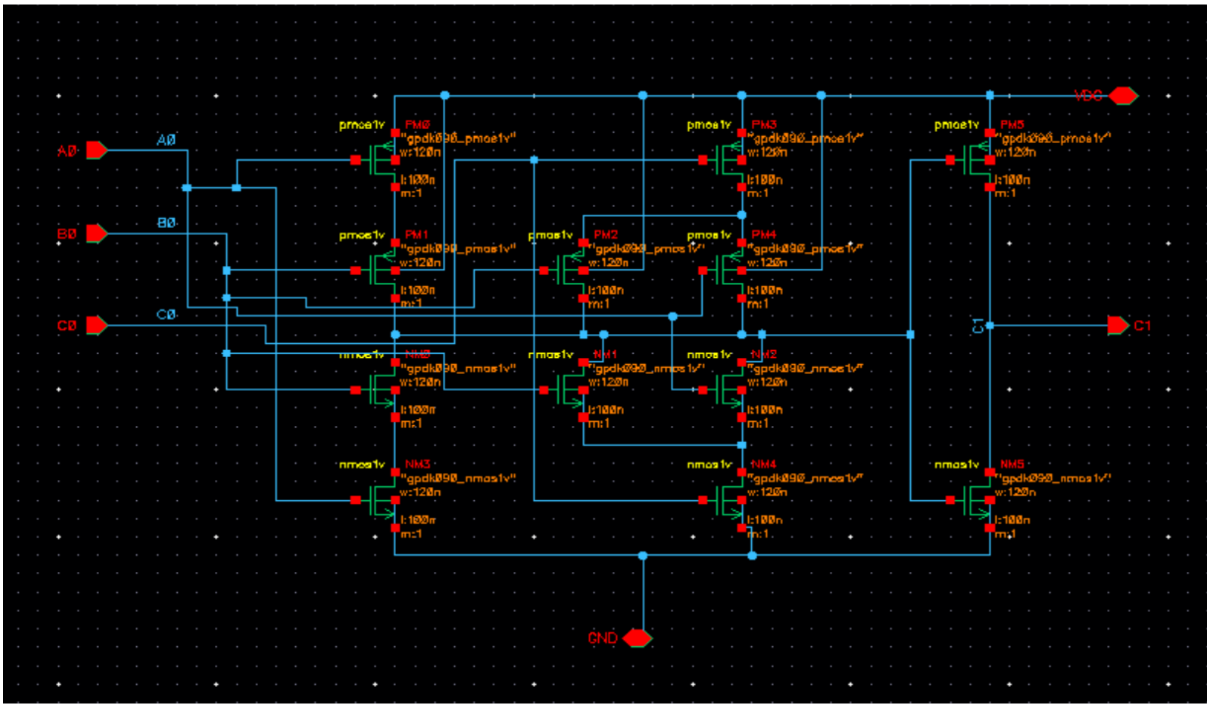


Fig 4- CMOS Circuit for C-out bit-1

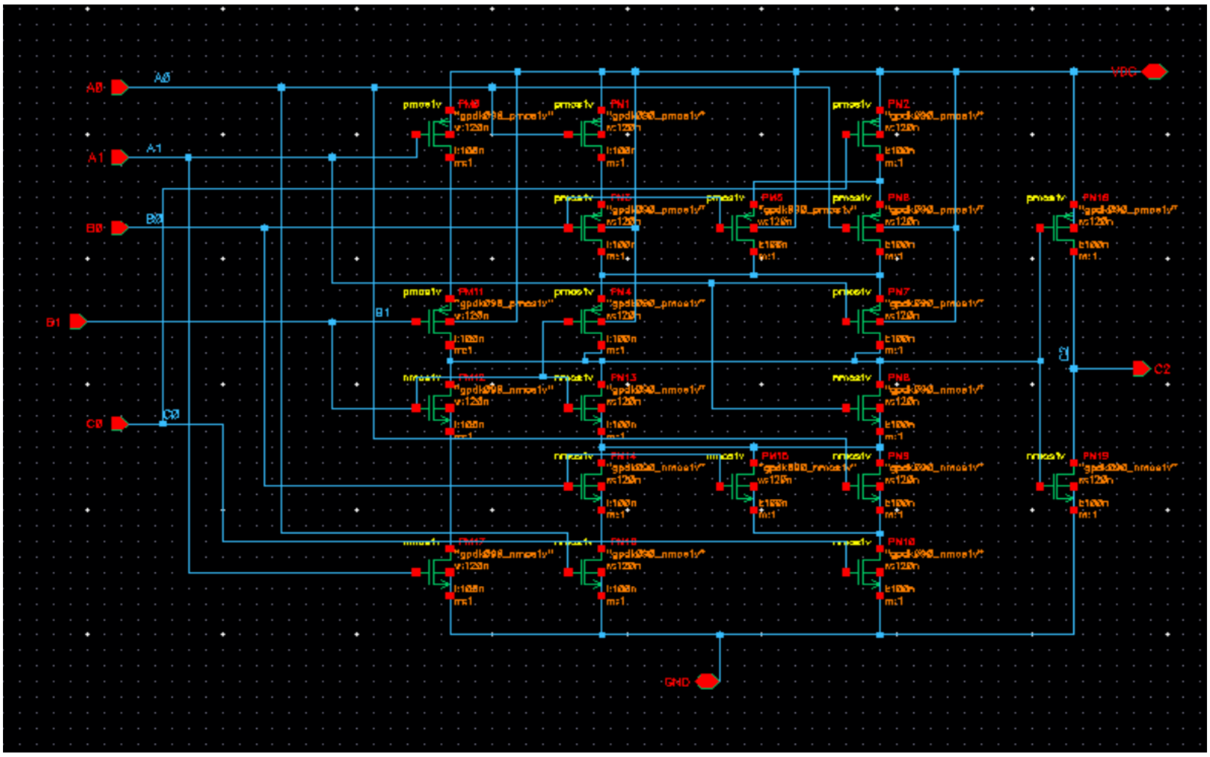


Fig 5- CMOS Circuit for C-out bit-2

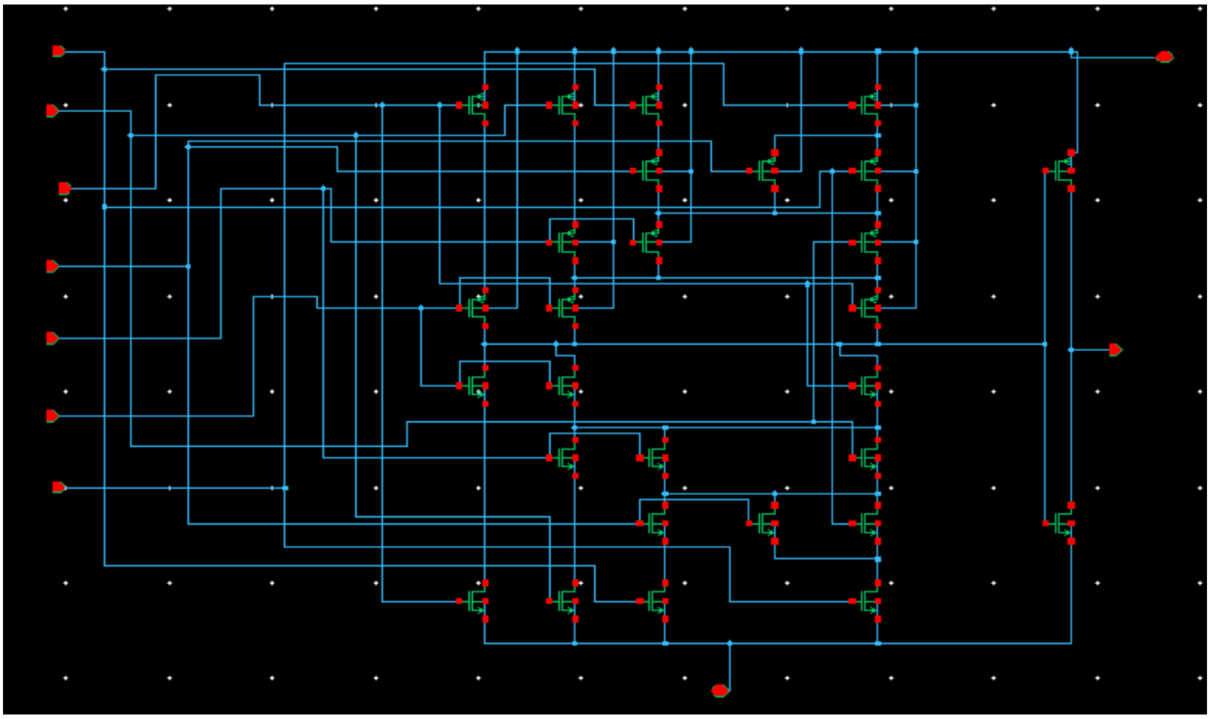


Fig 6- CMOS Circuit for C-out bit-3

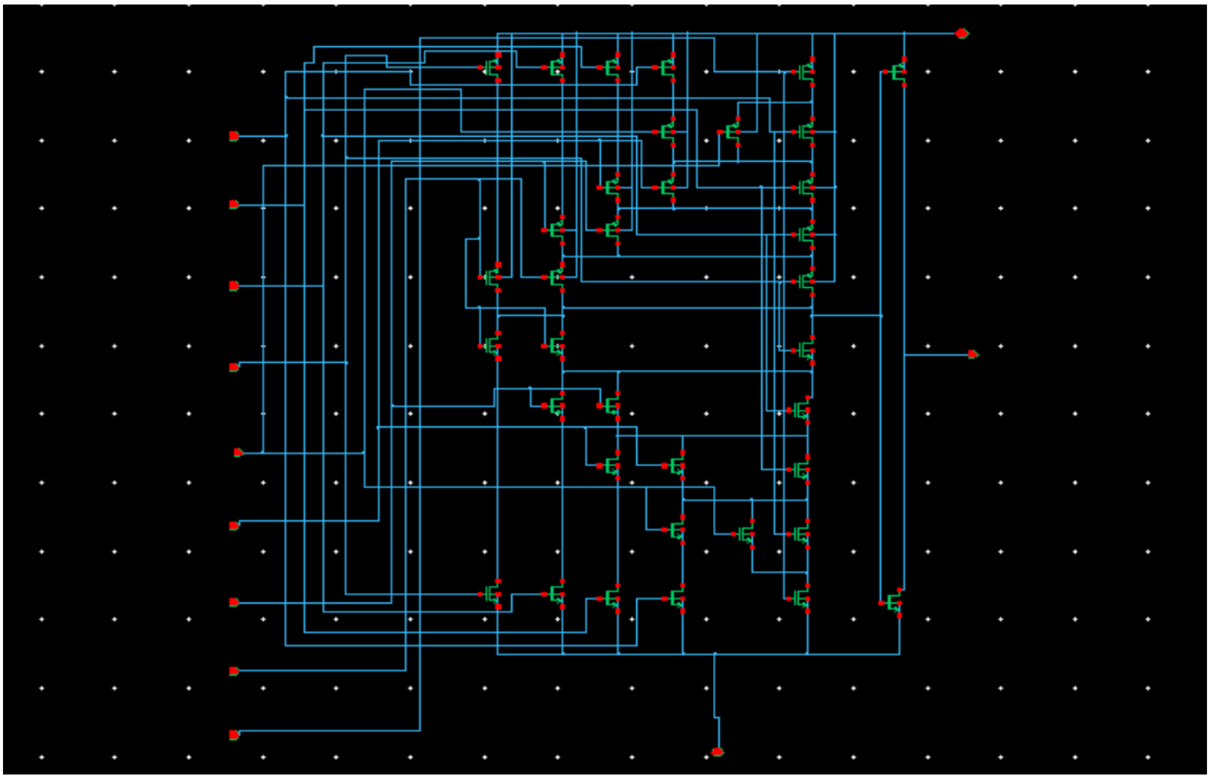


Fig 7- CMOS Circuit for C-out bit-4

The circuit below shows the complete CMOS circuit of the proposed CLA with the symbols of the circuits designed above.

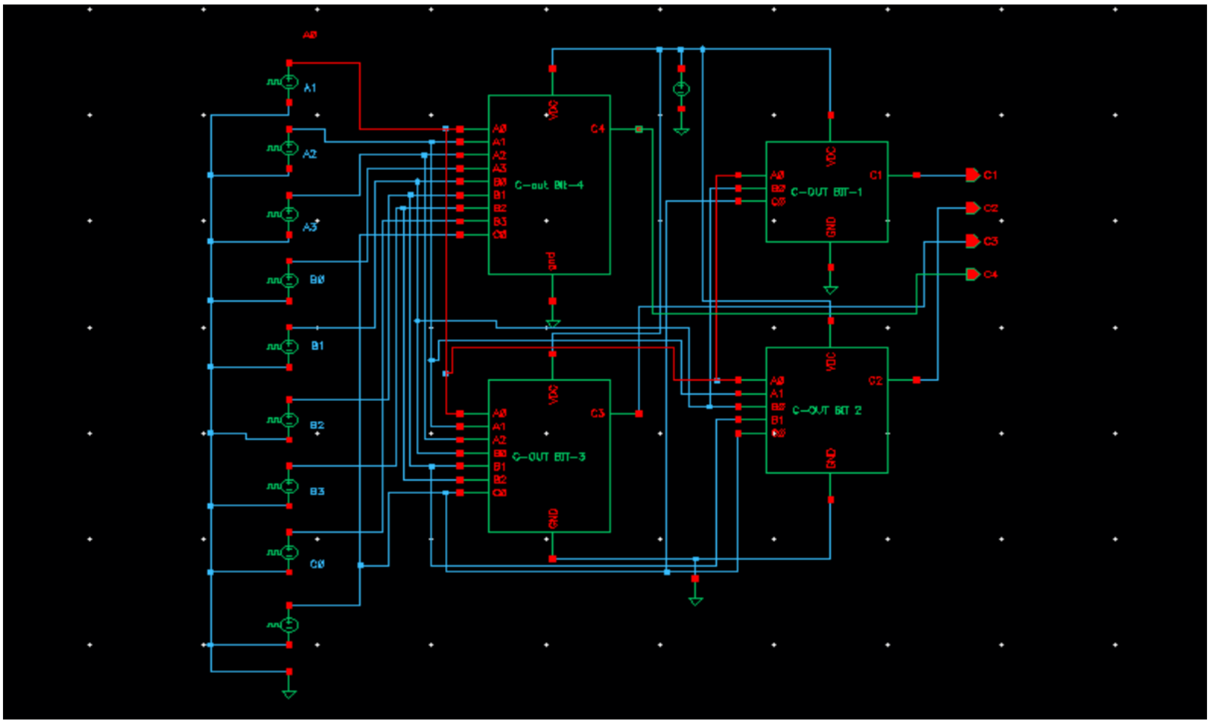


Fig 8- CMOS Circuit for the complete CLA

5. Results

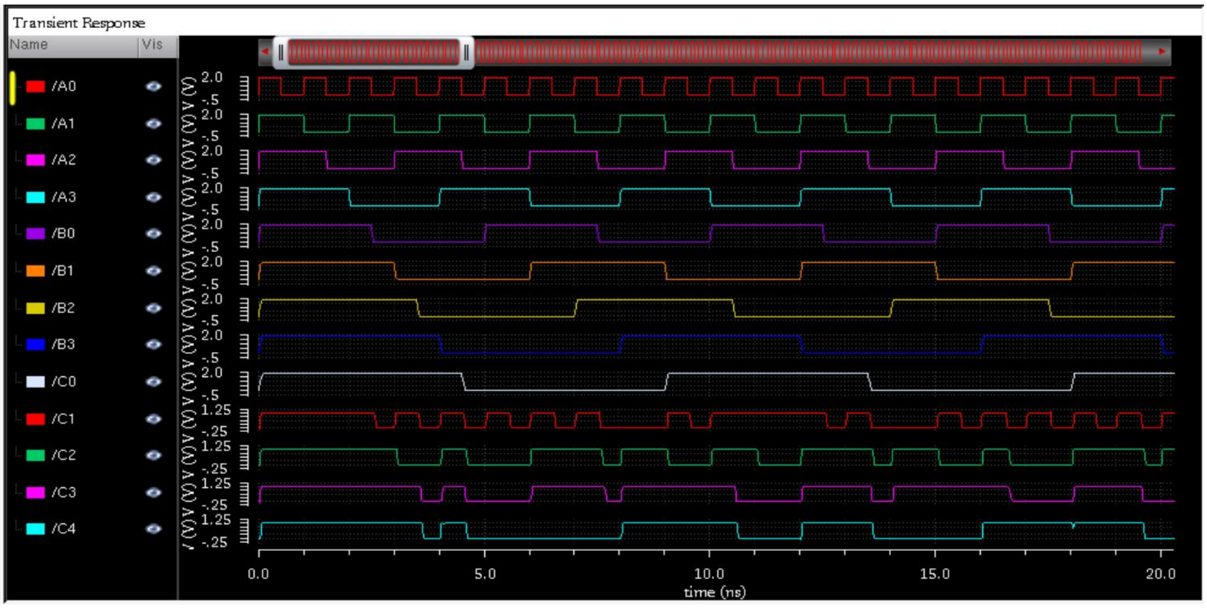


Fig 9- Transient Analysis of the CLA

The above figure illustrates the transient analysis of the CLA circuit, with the input voltages being 0-1.8v and the corresponding carry out signals are as shown.

The figure below illustrates the rise time, fall time, and propagation delays for the Carry Look-Ahead Adder (CLA). This comparison is made between an input signal, A0, and the output signal, C4 . Additionally, the average power consumption of the CLA was measured and found to be 0.5258 µs.

Table 1- Propagation delays of rise time and fall time.

Time	Propagation delay(ns)
Rise time	0.0362
Fall time	0.11788

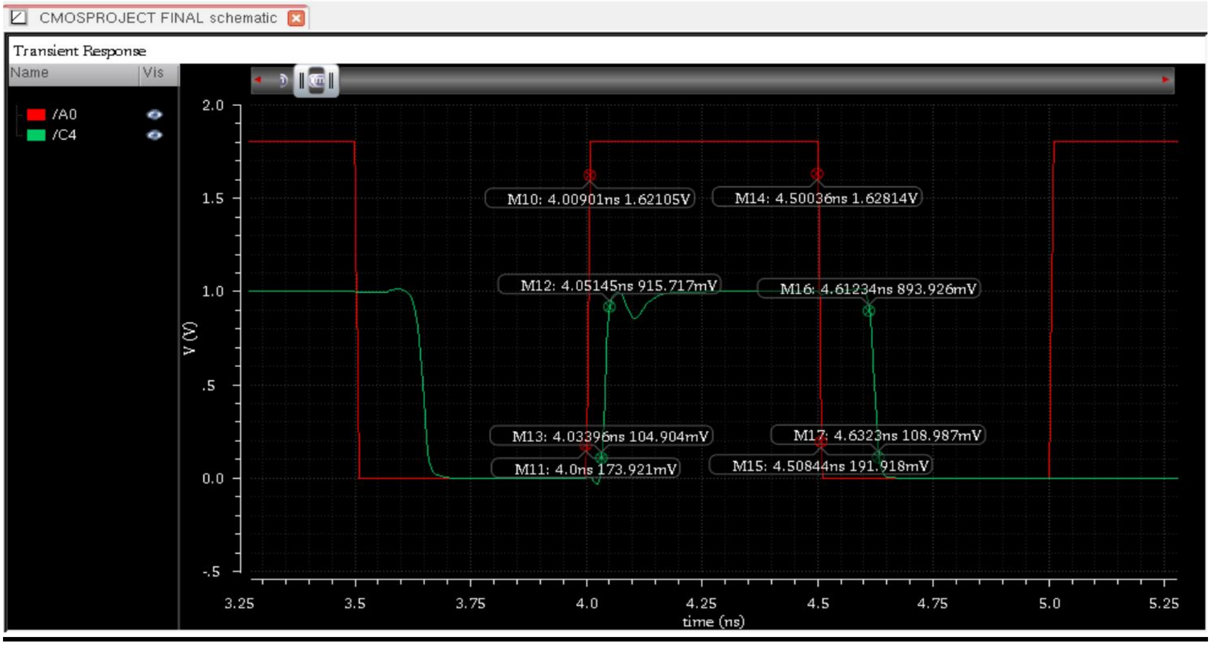


Fig 9- Comparison of rise time and fall time delays of input and output signals.

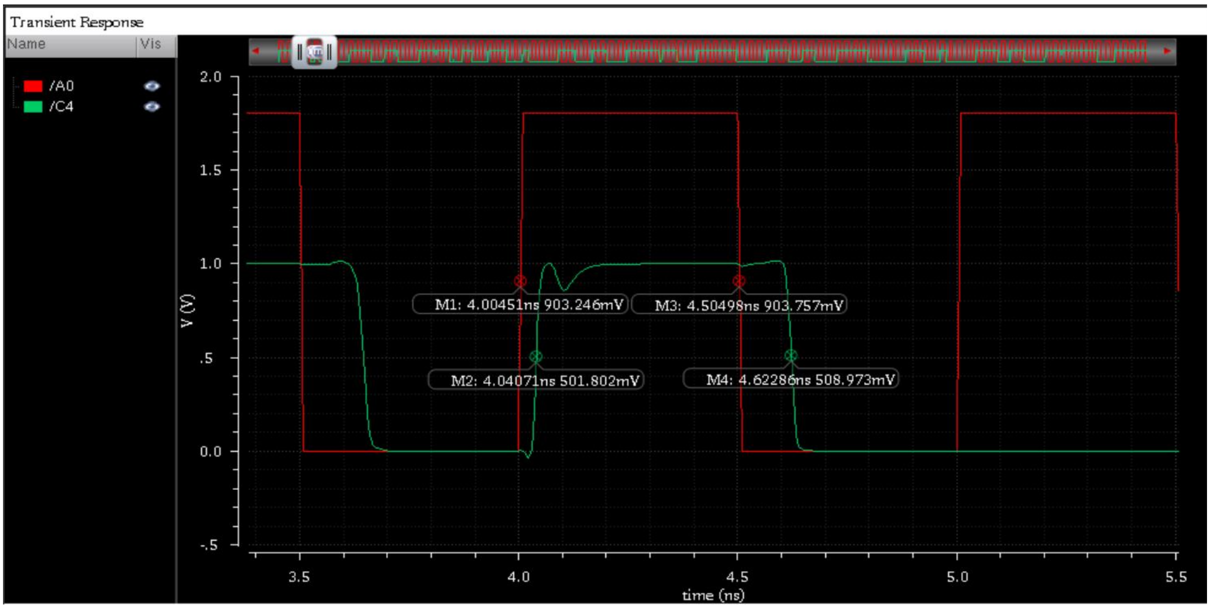


Fig 10- Propagation delay comparison of input and output signals.

6. Conclusion

In conclusion, the development and implementation of the 4-bit Carry Look-Ahead Adder (CLA) using the newly proposed simplified equations have demonstrated significant advancements in speed and efficiency. By leveraging an optimized transistor-level static CMOS logic, traditional dependencies on carry-generate and carry-propagate terms have been bypassed, resulting in faster carry-out bit computations. Although the simulation and execution were conducted using a 90 nm technology node instead of the 45 nm technology cited in the base paper, substantial reductions in power consumption and propagation delay were still observed. It's important to note that while accurate comparisons to the base paper's results regarding propagation delays and average power weren't possible due to the change in technology, our findings still highlight promising improvements in computational efficiency and energy consumption. This suggests that our innovative approach holds potential for enhancing the performance of modern microprocessors, albeit with technology-specific considerations.

7. References

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[3] You, H., Yuan, J., Tang, W. and Qiao, S., 2019. An energy and area efficient carry select adder with dual carry adder cell. Electronics, 8(10), p.1129