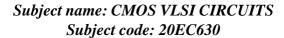
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### SRI JAYACHAMARAJENDRA COLLEGE OF ENGINEERING



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# Report on "BODY BIASING IN SCHMITT TRIGGER"

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### 1. Introduction

The advancements in Complementary Metal-Oxide-Semiconductor (CMOS) Very-Large-Scale Integration (VLSI) technology have significantly contributed to the development of sophisticated and efficient digital circuits. One of the essential components in digital systems is the Schmitt trigger, a comparator circuit with hysteresis implemented using positive feedback. This device is crucial for noise reduction and signal conditioning in a variety of applications, ranging from simple switches to complex communication systems. In recent years, body biasing techniques have emerged as a promising method to enhance the performance and power efficiency of CMOS circuits, including the Schmitt trigger.

The integration of body biasing in Schmitt trigger design presents a new dimension in achieving robust and adaptable digital circuits. By leveraging body biasing, designers can achieve greater control over the trigger points and hysteresis of the Schmitt trigger, leading to enhanced performance in variable operating conditions. This approach not only contributes to improved noise immunity and signal stability but also offers a pathway to reducing overall power consumption. As CMOS technology continues to scale down, the significance of body biasing techniques in optimizing VLSI circuits will likely grow, making it an important area of study for modern electronic design.

Body biasing involves adjusting the voltage of the body terminal of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) to control its threshold voltage. This technique allows for dynamic modulation of the transistor's performance characteristics, enabling designers to optimize the trade-offs between speed, power consumption, and noise immunity. In the context of a Schmitt trigger, body biasing can be utilized to fine-tune the hysteresis window, improving the circuit's ability to reject noise and produce clean digital signals even in the presence of voltage fluctuations.

## 2. Objectives

- i. Analyze the transient response of the Schmitt trigger with and without body biasing to illustrate the differences in signal behavior.
- ii. Investigate the hysteresis characteristics of the Schmitt trigger under varying body biasing conditions.
- iii. Evaluate the DC response of the Schmitt trigger with body biasing and compare it with a conventional Schmitt trigger to highlight any performance improvements or differences.

## 3. Block Diagram

#### PROPOSED SCHMITT TRIGGER BLOCK DIAGRAM

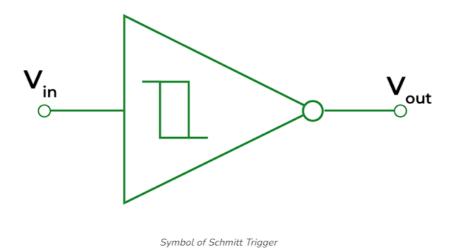


Fig 1- Schmitt Trigger symbol

A Schmitt trigger, a fundamental component in digital electronics, operates on the principle of positive feedback to convert analog signals into clear digital outputs. At its core, this circuit comprises two distinct voltage thresholds: an upper threshold (Vth\_up) and a lower threshold (Vth\_down). These thresholds serve as pivotal reference points, guiding the trigger's behavior. When the input voltage surpasses Vth\_up, the trigger's output swiftly transitions to a high state (Vdd), indicating a digital "1." Conversely, when the input voltage drops below Vth\_down, the output switches decisively to a low state (ground), signifying a digital "0." Crucially, what sets the Schmitt trigger apart is its implementation of hysteresis—a concept vital for ensuring stability and noise immunity. This hysteresis, defined by the voltage difference between Vth\_up and Vth\_down, enables the trigger to maintain its output state until the input signal crosses the opposite threshold, thus mitigating the effects of noise and ensuring clean, reliable digital signals. In essence, the Schmitt trigger's ability to seamlessly toggle between states, coupled with its inherent noise-rejection capabilities, renders it indispensable for a myriad of applications where signal integrity is paramount.

Noisy Signal Value (Vn)	Output Signal State (Vout)
Vn> V <sub>UT</sub>	High State ('1')
$V_{LT} < V_{n} < V_{UT}$	Remain in the previous state
Vn< V <sub>LT</sub>	Low State ('0')

Fig 2- Graphical representation of working of Schmitt trigger.

#### **Working of Schmitt Trigger**

The Schmitt trigger, a vital component in digital electronics, operates on the principle of positive feedback to convert analog signals into clear digital outputs. At its core, this circuit comprises two distinct voltage thresholds: an upper threshold (Vth\_up) and a lower threshold (Vth\_down). These thresholds serve as pivotal reference points, guiding the trigger's behavior. When the input voltage surpasses Vth\_up, the trigger's output swiftly transitions to a high state (Vdd), indicating a digital "1." Conversely, when the input voltage drops below Vth\_down, the output switches decisively to a low state (ground), signifying a digital "0." The comparator works properly when the input signal does not contain any noise. If the noise is present than comparator does not work properly. When the noisy signal is present, the Schmitt trigger gives proper results. It uses two threshold voltages i.e., upper threshold voltage (VUT) and lower threshold voltage (VLT).

Body biasing, a technique utilized in integrated circuit design, offers a versatile approach to enhance the performance of Schmitt triggers. By applying a bias voltage to the substrate terminal of MOSFETs, designers can dynamically adjust the threshold voltage, thereby fine-tuning circuit behavior. In Schmitt triggers, this capability is particularly advantageous as it enables precise control over trigger points and hysteresis width, enhancing noise immunity and signal stability. Additionally, body biasing facilitates performance optimization by allowing designers to tailor circuit parameters

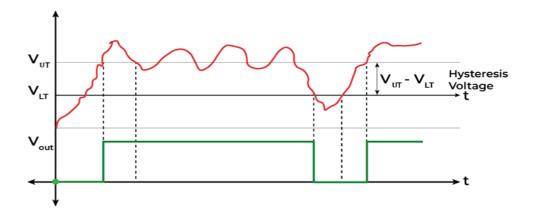


Fig 3: Noise signal analysis

to meet specific design requirements, such as minimizing propagation delay or reducing power consumption. Overall, body biasing serves as a powerful tool in optimizing Schmitt trigger performance, offering flexibility and efficiency in circuit design.

### 4. Methodology

- 1. Schematic Design: Begin by designing the Schmitt trigger circuit in Cadence Virtuoso's Schematic Editor. Define the components such as transistors, resistors, and capacitors according to your circuit requirements. Ensure that the schematic captures the essence of the Schmitt trigger's operation, including positive feedback and threshold voltages.
- 2. Parameter Setup: Define the necessary parameters for the transistors and other components in the schematic. Set up parameters such as threshold voltages, channel lengths, widths, and capacitances to reflect the desired behavior of the Schmitt trigger.
- 3. Simulation Setup: Configure simulation settings in Cadence Virtuoso for transient analysis and DC analysis. Define input signal characteristics such as frequency, amplitude, and waveform shape. Set up the simulation environment to analyze the behavior of the Schmitt trigger under different operating conditions.
- 4. Transient Analysis: Perform transient analysis simulations to study the dynamic behavior of the Schmitt trigger. Apply input signals with varying amplitudes and frequencies to observe how the trigger responds and switches between its stable states. Analyze the transient response to understand the impact of positive feedback and hysteresis on signal stability and noise immunity.

5. DC Analysis: Conduct DC analysis simulations to examine the DC response of the Schmitt trigger. Sweep input voltage values across the threshold voltages to determine the switching points and hysteresis characteristics. Evaluate the DC transfer curve to validate the design's performance and ensure that it meets the desired specifications.

The circuits below shows the CMOS design of conventional Schmitt Trigger

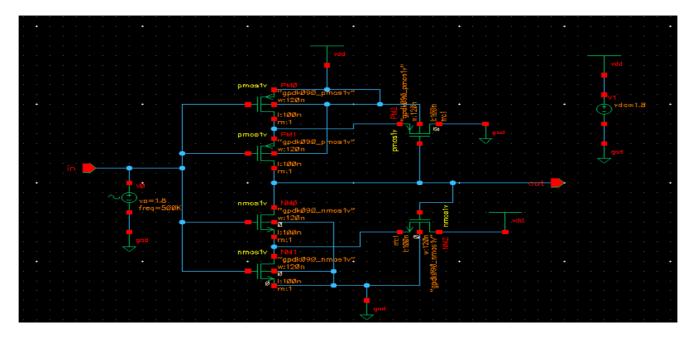


Fig 4: Schmitt Trigger

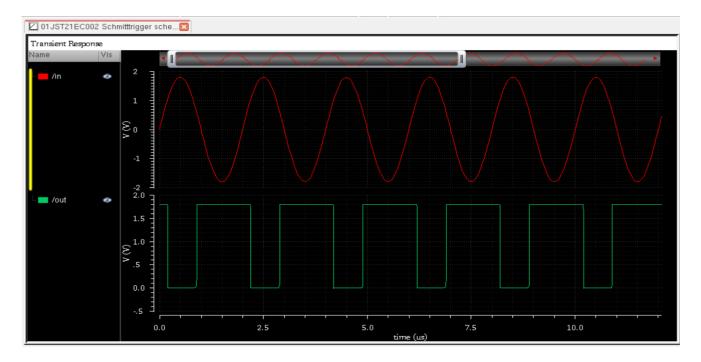


Fig 5: Transient Response



Fig 6: DC Response

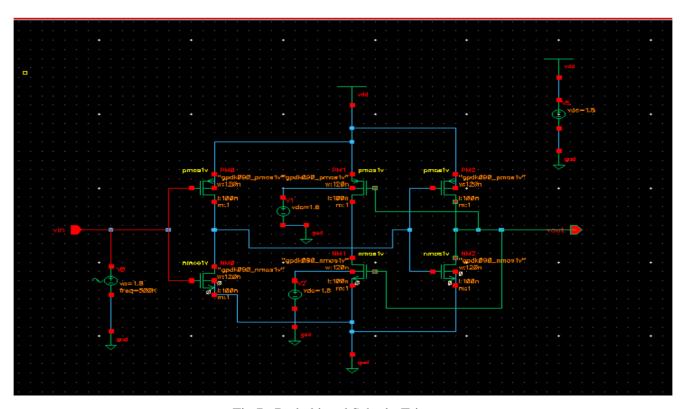


Fig 7: Body biased Schmitt Trigger

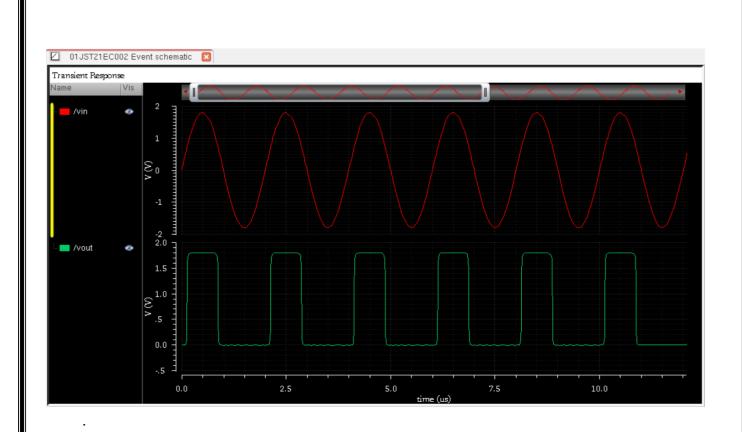


Fig 9: Transient Response

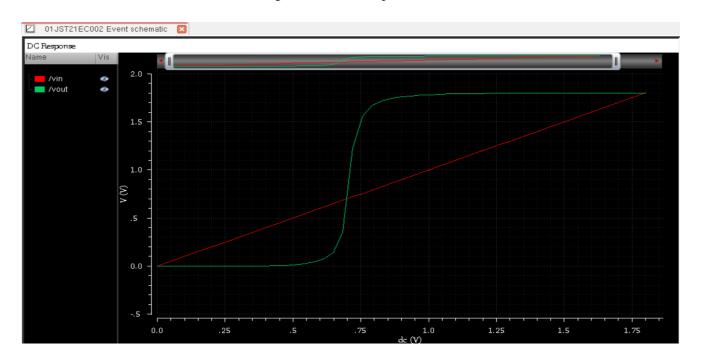


Fig 10: DC Response

The table below illustrates the rise time, fall time, and propagation delays for the Schmitt Trigger.

Table 1: Calculations for Conventional Schmitt Trigger

Rise time	0.39 ns
Fall time	0.15 ns
High to Low voltage	1.039 V
Low to High voltage	587 mV

Table 2: Calculations for Body Biased Schmitt Trigger

Rise Time	23.357 ns
Fall Time	22.699 ns
High to Low voltage	717 mV
Low to High voltage	698 mV

In comparing the performance of conventional and body-biased Schmitt triggers, several key parameters were evaluated, including rise time, fall time, and threshold voltages for high-to-low and low-to-high transitions. The conventional Schmitt trigger exhibited notably lower rise and fall times of 0.39 ns and 0.15 ns, respectively, compared to the body-biased configuration, which recorded significantly higher values of 23.357 ns and 22.699 ns, respectively. However, the body-biased Schmitt trigger demonstrated superior control over threshold voltages, with high-to-low and low-to-high voltage transitions measured at 717 mV and 698 mV, respectively, indicating a narrower hysteresis window compared to the conventional design.

While the conventional Schmitt trigger excelled in terms of switching speed, the body-biased configuration showcased enhanced precision and stability in threshold voltage control, crucial for applications demanding fine-tuned signal detection and noise immunity. Despite the trade-off in speed, the body-biased Schmitt trigger's ability to finely tune threshold voltages through body biasing presents a compelling advantage, especially in scenarios where precise control over signal transitions is paramount. This comparative analysis underscores the importance of considering multiple design factors, including speed, precision, and noise immunity, to tailor Schmitt trigger designs according to specific application requirements.

## 5. Conclusion

Overall, this project delved into the world of Schmitt triggers, specifically focusing on the integration of bodyweight techniques, all within the context of 90nm technology. Through a careful study and simulation using Cadence Virtuoso software, we aimed to determine the possible effect of body weight on the performance of Schmitt triggers. By dynamically manipulating the threshold voltage of the MOSFETs, we aimed to fine-tune the trigger points and hysteresis width, with the aim of increasing noise tolerance and enhancing signal stability. Our results demonstrate the critical role of body weight in modern CMOS VLSI design, providing insight into the intricacies of Schmitt trigger optimization and its central role in improving the efficiency and functionality of digital circuits. This project not only emphasizes the importance of advanced methods, but also testifies to the continuous innovation in semiconductor technology, promising new opportunities for the further development of circuit design and optimization.

## 6. References

- [1] Razavi, Behzad. "Design of Analog CMOS Integrated Circuits." McGraw-Hill Education, 2000.
- [2] Baker, R. Jacob, Li, Harry W., and Boyce, David E. "CMOS Circuit Design, Layout, and Simulation." John Wiley & Sons, 2005.
- [3] Weste, Neil H. E., and Harris, David. "CMOS VLSI Design: A Circuits and Systems Perspective." Pearson, 2010.
- [4] Kang, Sung-Mo, and Leblebici, Yusuf. "CMOS Digital Integrated Circuits: Analysis and Design." McGraw-Hill Education, 2002.
- [5] Rabaey, Jan M., Chandrakasan, Anantha, and Nikolic, Borivoje. "Digital Integrated Circuits: A Design Perspective." Prentice Hall, 2003.
- [6] Smith, J. H., and Sedra, A. S. "Microelectronic Circuits." Oxford University Press, 2010.
- [7] Gray, Paul R., Hurst, Paul J., Lewis, Stephen H., and Meyer, Robert G. "Analysis and Design of Analog Integrated Circuits." John Wiley & Sons, 2001.
- [8] IEEE Xplore Digital Library (https://ieeexplore.ieee.org/)
- [9] ACM Digital Library (https://dl.acm.org/)
- [10] ResearchGate (https://www.researchgate.net/)