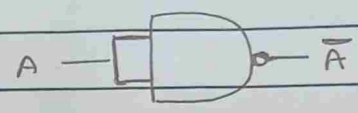


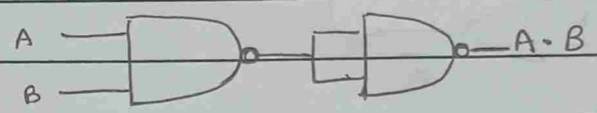
MISSION 1:

(a) NOT gate



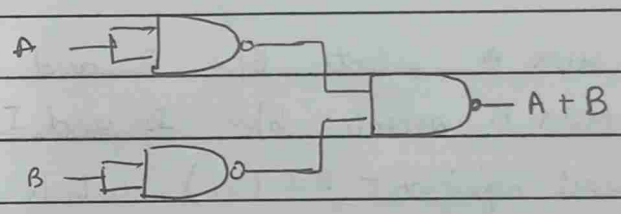
$$\bar{A} = \overline{A \cdot A}$$

(b) AND gate



$$A \cdot B = \overline{\overline{A} \cdot \overline{B}}$$

(c) OR gate



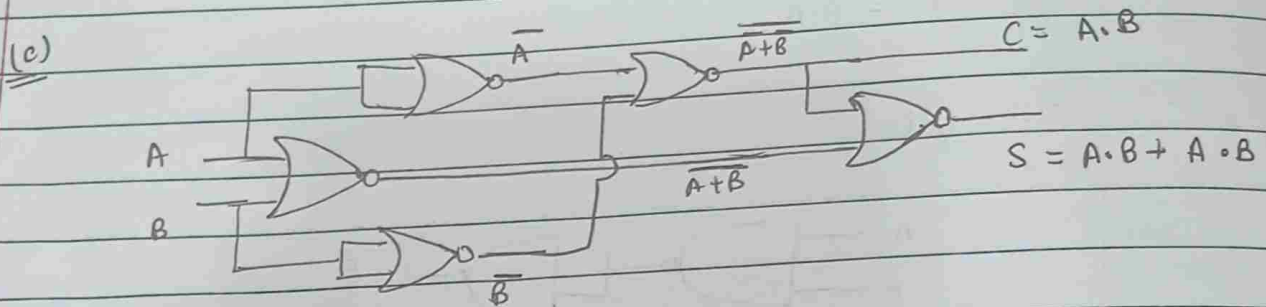
$$A + B = \overline{\overline{A} \cdot \overline{B}}$$

MISSION 2 :-

(a)	A	B	Sum	Carry
	0	0	0	0
	0	1	1	0
	1	0	1	0
	1	1	0	1

(b) sum bit (s) = $A \text{ XOR } B$
 $= A \oplus B = A \cdot \bar{B} + \bar{A} \cdot B$

carry bit (c) = $A \cdot B$



MISSION 3:

First level : MUX A selects b/w I_0 and I_1
 (selection of inputs) MUX B selects b/w I_2 and I_3
 Least significant Bit (S_0) controls both MUX A & MUX B.

Second level : outputs of MUX A \Rightarrow inputs to the second
 (final selection) and MUX B 2 to 1 MUX

$S_1 S_0$	MUX A output (Y_A)	MUX B Y_B	Y	Result
0 0	selects I_0	selects I_2	Y_A	I_0
0 1	selects I_1	" I_3	Y_A	I_1
1 0	selects I_0	" I_2	Y_B	I_2
1 1	selects I_1	" I_3	Y_B	I_3

MISSION 4:

(a) We need '2' D flip flops

Reasoning: A pattern detector for '111' needs to remember the sequence of the last few inputs. The state of the circuit should represent how much of the target pattern ("111") has been successfully matched so far.

S_0 No 1s matched
 S_1 one consecutive '1' matched
 S_2 Two consecutive '1s' matched.

This requires three distinct states (S_0, S_1, S_2)

No. of flip flops for M states = N ; $2^N \geq M$

(M=3) $2^1 = 2$ (X)
 $2^2 = 4$ (✓)

Therefore $N=2 \Rightarrow$ Two D flip flops are required.

(b)	state	Q_1, Q_0
	S_0	0 0
	S_1	0 1
	S_2	1 0
	Unused	1 1

~~Q_1~~ →

Q_1 (MSB), Q_0 (LSB) → outputs of two flip flops

state Table:

current state	$Q_1 Q_0$	Input X	Next state	$Q_1^+ Q_0^+$	output P
S_0	00	0	S_0	00	0
S_0	00	1	S_1	01	0
S_1	01	0	S_0	00	0
S_1	01	1	S_2	10	0
S_2	10	0	S_0	00	0
S_2	10	1	S_2	10	1
S_3	11	0	S_0	00	0
S_3	11	1	S_0	00	0

