A) HALF ADDER Code:-

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end HA;

architecture Behavioral of HA is

begin

sum<= a xor b;

carry<= a and b;

end Behavioral;

HALF ADDER Test Bench:-

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_tb is

-- Port ( );

end HA\_tb;

architecture Behavioral of HA\_tb is

component HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end component;

signal a,b,sum,carry:STD\_LOGIC;

begin

U1: HA port map(a,b,sum,carry);

process

begin

a<='0';

b<='0';

wait for 100ns;

a<='0';

b<='1';

wait for 100ns;

a<='1';

b<='0';

wait for 100ns;

a<='1';

b<='1';

wait for 100ns;

end process;

end Behavioral;