FULL ADDER CODE

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity full\_adder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end full\_adder;

architecture Behavioral of full\_adder is

begin

s <= a xor b xor cin;

cout <= (a and b) or (b and cin ) or (cin and a);

end Behavioral;

C) RCA Code :-

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity RCA is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

Sum : out STD\_LOGIC\_VECTOR (3 downto 0);

Cout : out STD\_LOGIC;

Cin : in STD\_LOGIC);

end RCA;

architecture Behavioral of RCA is

COMPONENT full\_adder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end COMPONENT;

signal temp:std\_logic\_vector(3 downto 0);

begin

u1: full\_adder port map(a(0),b(0),cin,sum(0),temp(0));

u2: full\_adder port map(a(1),b(1),temp(0),sum(1),temp(1));

u3: full\_adder port map(a(2),b(2),temp(1),sum(2),temp(2));

u4: full\_adder port map(a(3),b(3),temp(2),sum(3),cout);

end Behavioral;

RCA Test Bench:-

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity RCA\_tb is

-- Port ( );

end RCA\_tb;

architecture Behavioral of RCA\_tb is

component RCA is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

Sum : out STD\_LOGIC\_VECTOR (3 downto 0);

Cout : out STD\_LOGIC;

Cin : in STD\_LOGIC);

end component;

signal a,b,sum : std\_logic\_vector(3 downto 0);

signal cout,cin : std\_logic;

begin

u1: RCA port map(a,b,sum,cout,cin);

process

begin

a<="0101";

b<="1010";

cin<='1';

wait for 200 ns;

a<="1101";

b<="1000";

cin<='0';

wait for 200 ns;

end process;

end Behavioral;