Northwestern Polytechnic University

EE488 - Computer Architecture
Homework Assignment #2

Due day: 10/6/2021

Instruction:

1. **Push the answer sheet to Github in word file**
2. **Overdue homework submission could not be accepted.**
3. **Takes academic honesty and integrity seriously (Zero Tolerance of Cheating & Plagiarism)**

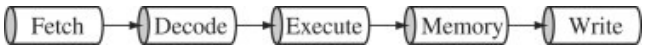
1. Discuss how stack architecture computer works by giving example. And compare the pros and cons between stack-based virtual machine and register-based virtual machine (1.5~2 pages)

Answer :

The computers CPU architecture that are implemented using stack data structure . It can stated as a group of memory locations in the read and write memory for the temporary storage of binary information during the execution of the program and is used to store addresses and data when the microprocessor branches to a subroutine. collection of data that can be enter as **Last In First Out (LIFO)** method. LIFO is the maximum used method in computer design. The essential architecture are the stack pointer, SP, and the program counter, PC. The register that stores the address of the topmost memory location of the stack is called stack pointer ,The main and most important part of computer architecture is pipelining structure .The pipelining can be carried out in two ways based on basic microcontroller architecture.

Three step

Five Step



Three step structure is as follows :-

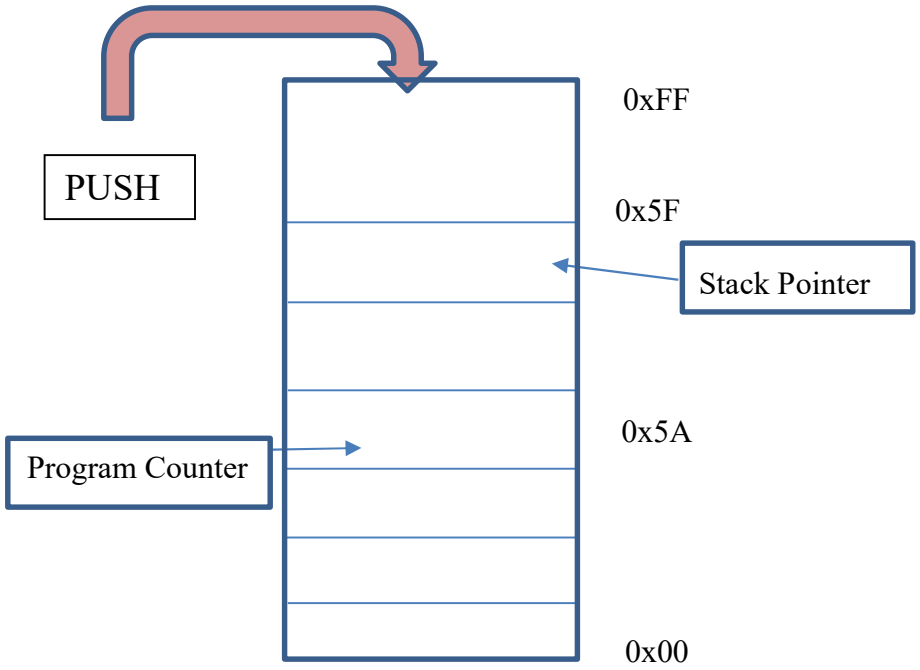
Instruction 1	**FETCH**	**DECODE**	**EXECUTE**		
Instruction 2	⟷		**FETCH**	**DECODE**	**EXECUTE**
Instruction 3	⟷				**FETCH**

Five step structure is as follows :-

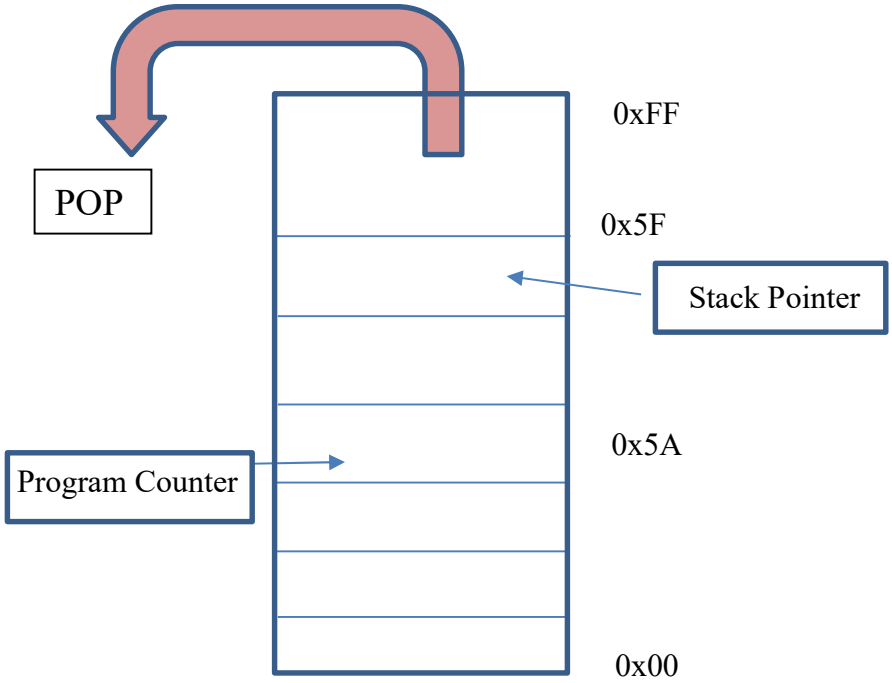
Inst'n 1	FETCH	DECODE	EXECUTE	MEMORY	WRITE					
Inst'n 2		FETCH	DECODE	EXECUTE	MEMORY	WRITE				
Inst'n 3			FETCH	DECODE	EXECUTE	MEMORY	WRITE			
Inst'n 4				FETCH	DECODE	EXECUTE	MEMORY	WRITE		
Inst'n 5					FETCH	DECODE	EXECUTE	MEM	WRITE	

For fetching new instruction, the memory stack needs a register that will let the processor the address the address to next instruction. This register is known as program counter. These register help in manipulation of stack elements .The main operation of adding of adding and removing the operands is performed by two operations namely PUSH and POP.

PUSH : This instruction is used to insert the operand at top of stack



POP : This instruction is used to remove the operand from top of stack



Example for Push and pop :mov r0,#2
push {r0}
mov r0,#3
pop {r0}

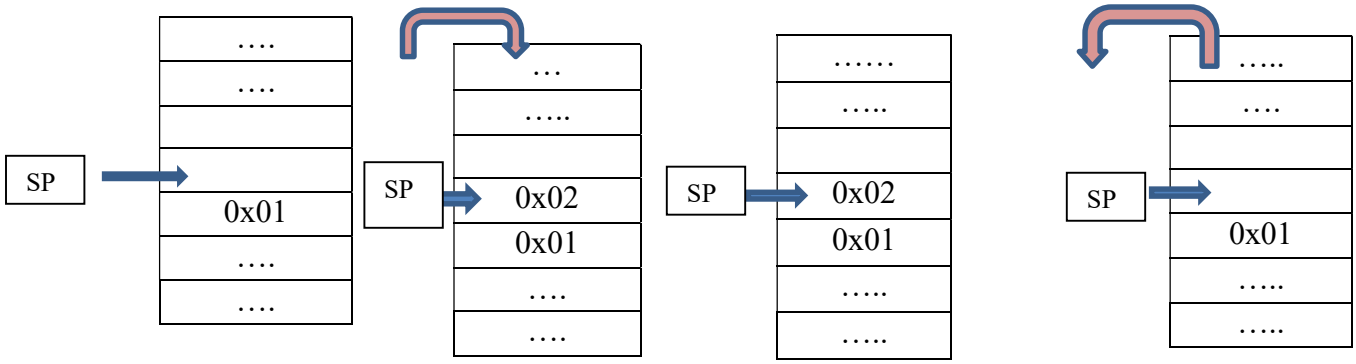
RO	R1	R2
0x00000000	0x00000000	0x00000000

mov r0,#2
R0=0x00000002

push {r0}
0x02

mov r0,#3
R0=0x00000003

pop{r0}
0x02



The cost of executing a Virtual Machine in an interpreter consists of three components:

- Dispatch instruction
- Access operands
- Perform compute

Dispatching the instruction consists of fetching the coming instruction from memory followed by adjacent segment of code implementing the instruction. This task can be performed in lesser instruction set than stack-based implementation. Consider an example, c=a+b which can be performed in stack virtual machine as load b ,load a, add ,store c. Whereas , in a register based virtual machine this can be carried out in one simple instruction ADD c,a,b. So it can be stated that register virtual machines can significantly reduce the count of instructions for a code.

Some reports shows that register based Virtual machine takes around 47% less instructions than stack based virtual machine,

As the register based VM directly assigns register to implement a segment the code 25 % larger than stack VM .

This results in cost of instruction fetching to rise but this rise occupies only 1.07% of machine loads/instruction which is negligible.

Considering the overall performance of register based virtual machine requires an approximate of 32.3% lesser time to implement primary benchmarks.

2. Processor is one of most important components in computing system. Its performance can make big impact to the whole system. Discuss about processor design metrics and benchmarking tools (1.5~2 pages)

Answer : Design Metrices -

Benchmarks and design metrics used for evaluating performance were always the issues discussed in market. Many improvements are made through ,since 1988 in benchmarks. Earlier that year performance was evaluated with small benchmarks as kernels that were extracted from applications like Lawrence Livermore Loops, Dhrystone and Whetstone benchmarks etc. The Standard Performance Evaluation Cooperative (SPEC) and Transactions Processing Council (TPC) established in 1988 brought up several improved benchmarking guidelines.As shown below , Performance evaluation can be divided on the basis of :-

- Performance Modeling
- Performance Measurement

<table>
<tr><td rowspan="4">Performance Measurement</td><td colspan="2">Microprocessor On-chip Performance Mornitoring Counter</td></tr>
<tr><td colspan="2">Off- chip Hardware Monitoring</td></tr>
<tr><td colspan="2">Software Monitoring</td></tr>
<tr><td colspan="2">Microcoded Instrumentation</td></tr>
<tr><td rowspan="8">Performance Modeling</td><td rowspan="5">Simulation</td><td>Trace Driven Simulation</td></tr>
<tr><td>Execution Driven Simulation</td></tr>
<tr><td>Complete System Simulation</td></tr>
<tr><td>Event Driven Simulation</td></tr>
<tr><td>Software Profiling</td></tr>
<tr><td rowspan="3">Analytical Modeling</td><td>Probabilistic Models</td></tr>
<tr><td>Queueing Models</td></tr>
<tr><td>Markov Models</td></tr>
<tr><td></td><td>Petri Net Models</td></tr>
</table>

The performance measurement can be further divided based on – On-chip , Off-chip , Software Monitoring and Micro-coded instrumentation. Performance Modelling can be classified into Simulation and Analytical Modeling .

Simulation Modeling can be implemented as Trace , Execution Complete system ,Event driven simulation and Software profiling.

Analytical Modelling can be Probabilistic, Queueing ,Markov and petri Net models. It is very important for a hardware level designer to take into consideration the following performance metrices like execution time and productivity .Execution time being the most important parameter is the product of instructions ,cycles per instruction (cpi) and the clock time period. Throughput of an application is a more important metric, especially in server systems. In servers that serve the banking industry, airline industry, or other similar business, what is important is the number of transactions that could be completed in unit time. MIPS i.e Millions of Instructions Per Second and MFLOPS i.e Million of Floating-Point Operations Per Second are the popular parameters of performance .

Performance metrices determines how well the processor performs. When you command the processor to execute the specific instruction and time the processor takes to give you the result , is called as response time(execution time). If we wish to improve

performance, we need to reduce our execution time. Performance is inversely proportional to execution time.

Performance = 1/ Execution time

When CPU X is n times faster than Y,

$$\frac{\text{performance}_X}{\text{performance}_Y} = \frac{\text{execution\_time}_Y}{\text{execution\_time}_X} = n$$

In some case the processor is carrying out two instructions at the same time .When it receives an interrupt or some instruction that makes it to jump and run the other program, making it leave the program it is currently on . Irrespective of this interrupt situation we only consider the current program and the time taken by CPU to on that particular program.
This CPU execution time for a program can be calculated by multiplying the total number of clock cycles and the clock cycle time. Each program is made up of a number of instructions and each instruction takes a number of clock cycles to execute.

$$\text{CPU execution time for a program} = \frac{\#\text{ CPU clock cycles for a program}}{\text{clock rate}}$$

or

$$\text{CPU execution time for a program} = \#\text{ CPU clock cycles for a program} \times \text{clock cycle time}$$

Being related as above, the performance can be improved by reducing the length of the clock cycle time or the number of clock cycles required for a program for execution.Clock cycle time is basically the time utilized to in one operation or pipelining stage.
The clock rate (MHz or GHz) is inversely proportional to clock cycle time (clock period) **CC = 1 / CR.**

Benchmark tools –
The benchmark used for performance calculation should represent the application that is installed and used in real application. The benchmark vary as per the sector of work from transaction to multimedia.
Below are the examples of benchmark tools in different sector:

- CPU benchmarks :
  -Uniprocessor
  -Parallel Processor
  Example :Uniprocessor => Java Grande Forum, ASCI SPEC 200
  Parallel processor => NASPAR
- Multimedia ,Embedded, DSP
  Example : EEMBC , Media bench.
- Java
  -Client

-Server
-Scientific

Examples : Client => Caffeine mark
Server =>Volano mark
Scientific=>SciMark

- Transaction , Processing
  -On-line transaction processing
  -Decision support system
  Examples : Transaction processing council C,TPC-R
- Web Server
  Example : VolanodMark ,SPEC web99
- Personal computer
  Example : Ziff Davis Win Bench ,3D MarkMAX99,Bapco SysMark