



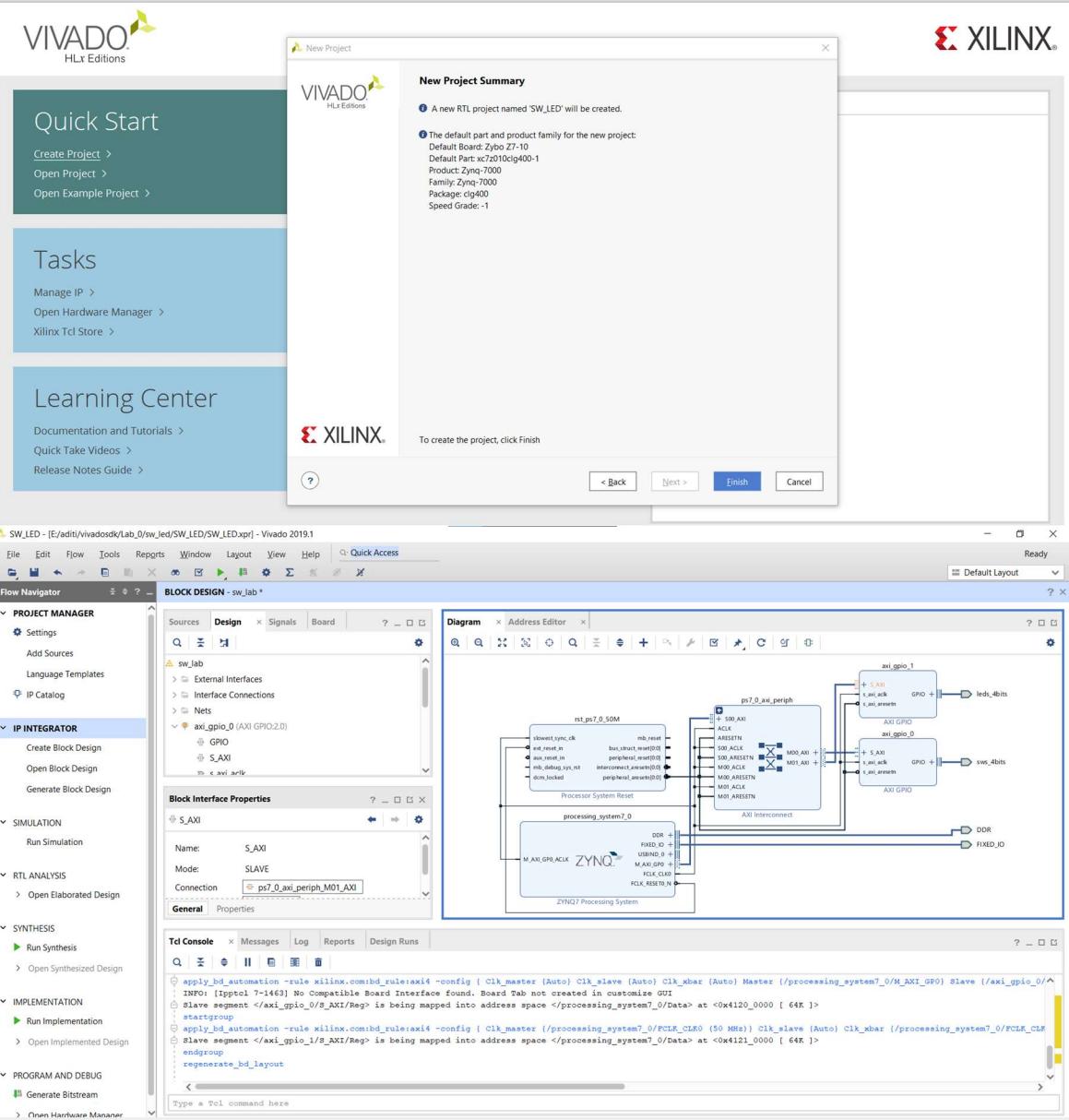
San Francisco Bay University

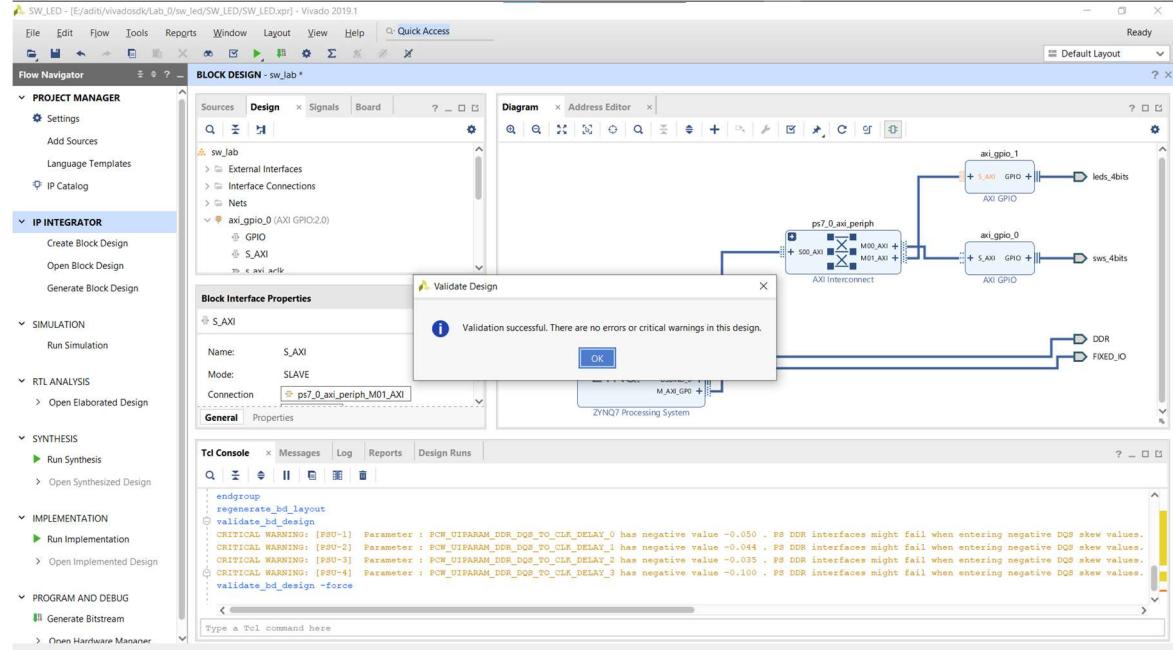
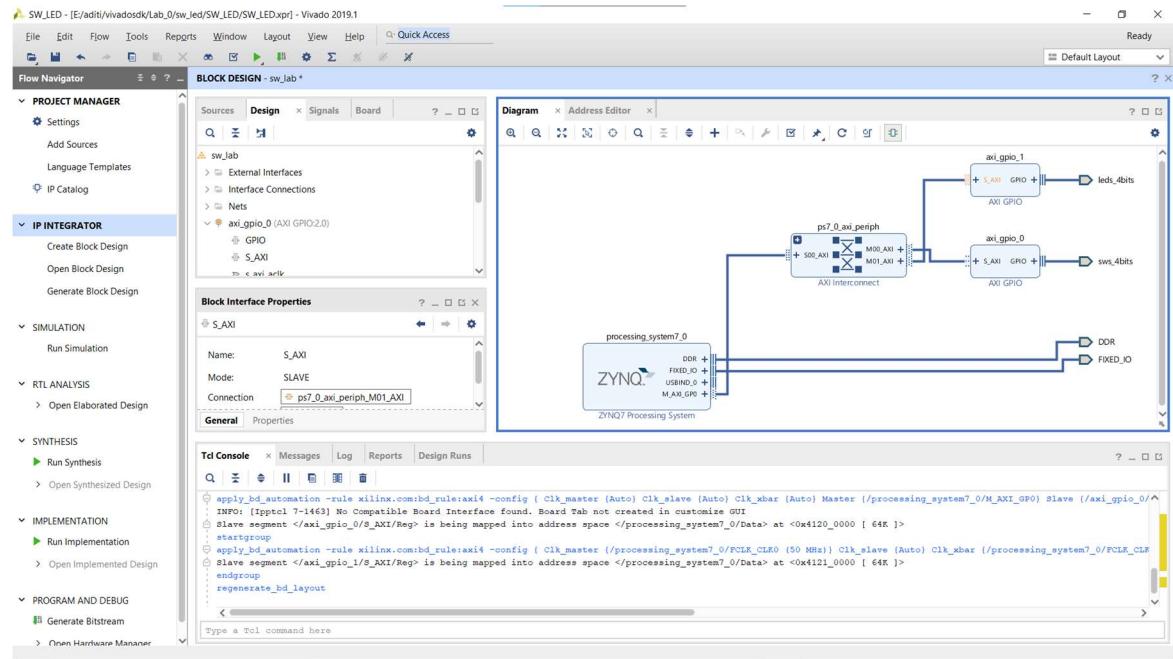
EE553 - System on Chip (SoC) Design Homework Assignment #3

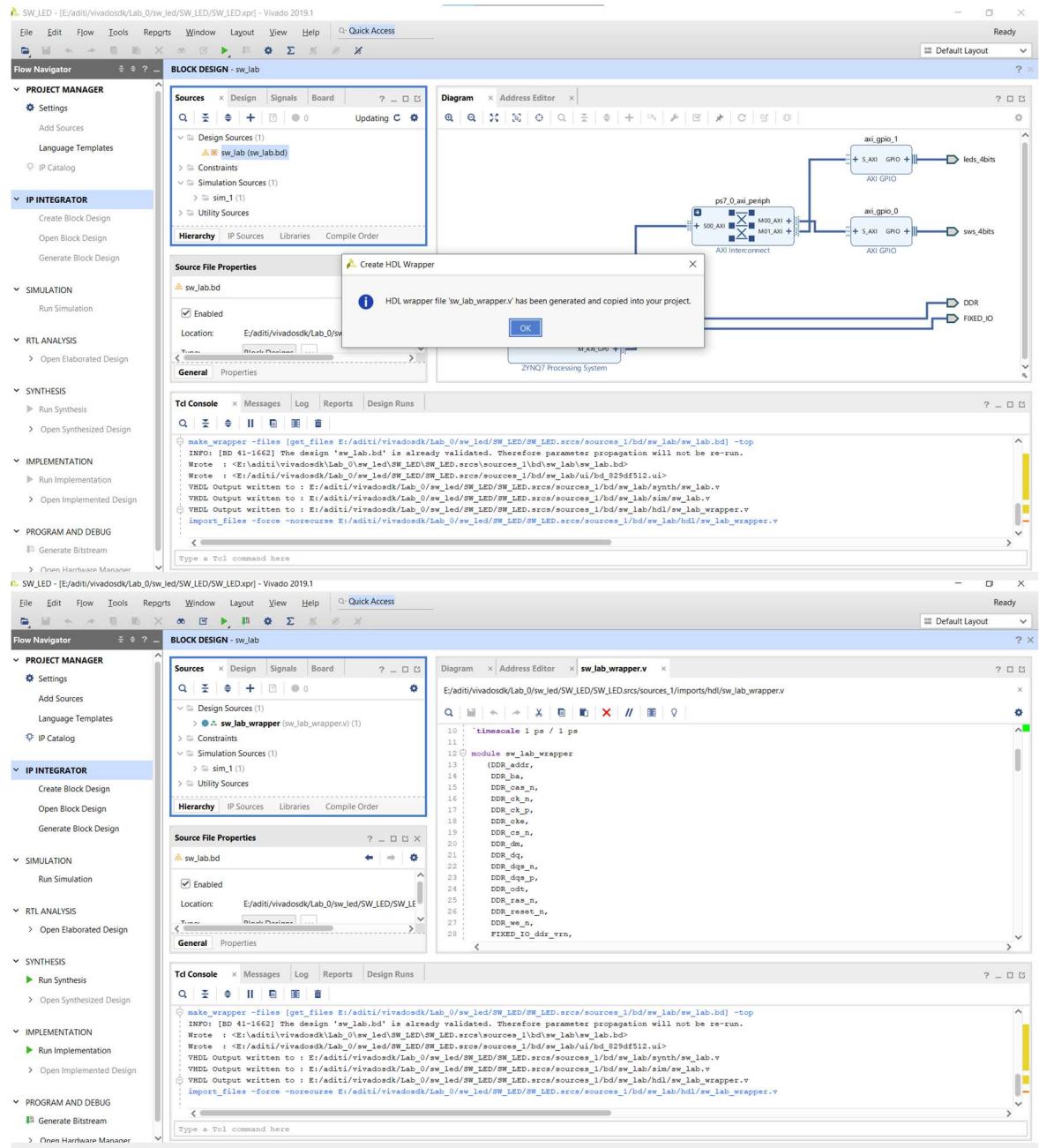
Due day: 3/16/2022

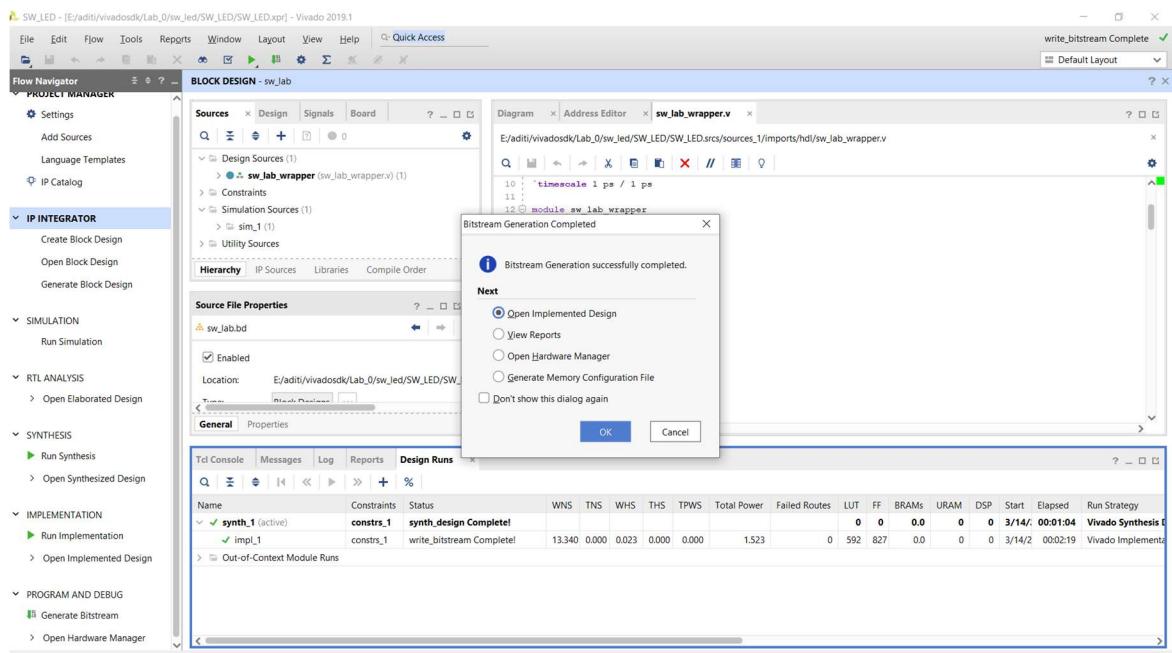
Instruction:

- 1. Push the answer sheet to Github**
 - 2. Overdue homework submission could not be accepted.**
 - 3. Takes academic honesty and integrity seriously (Zero Tolerance of Cheating & Plagiarism)**
-
1. Implement switch controlled / push button controlled LEDs without the interrupt on Zybo Z7-10 board following the instructions in lab manuals on Canvas week#9 module
Switch controlled LED –

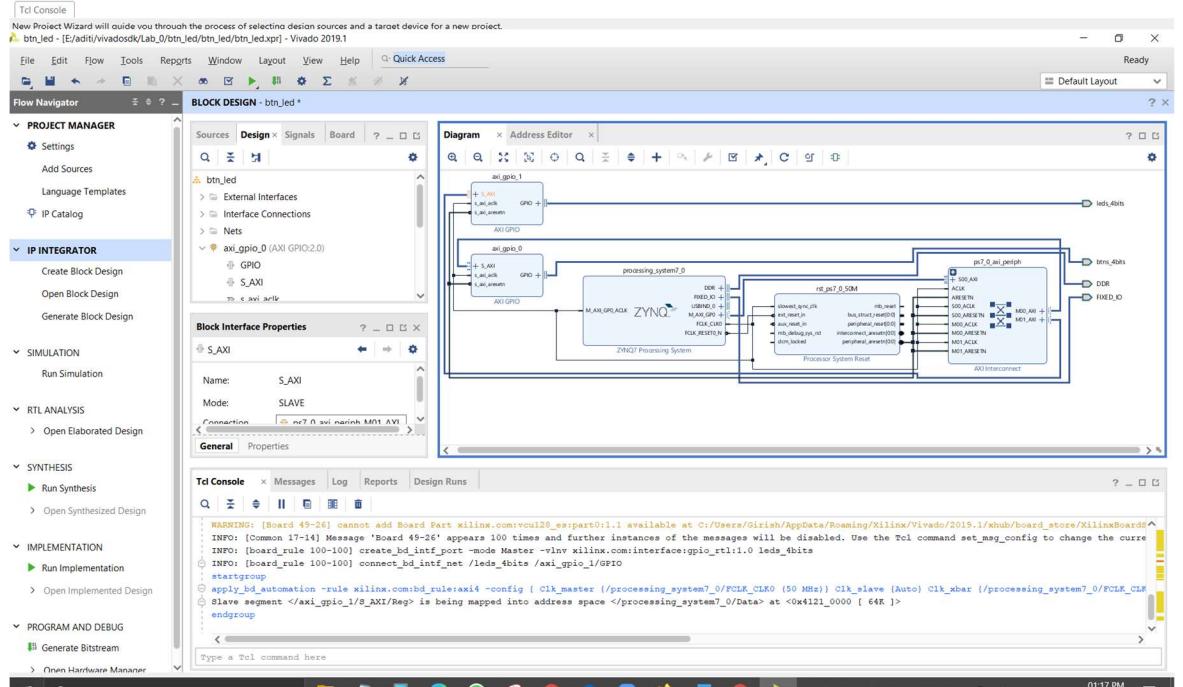
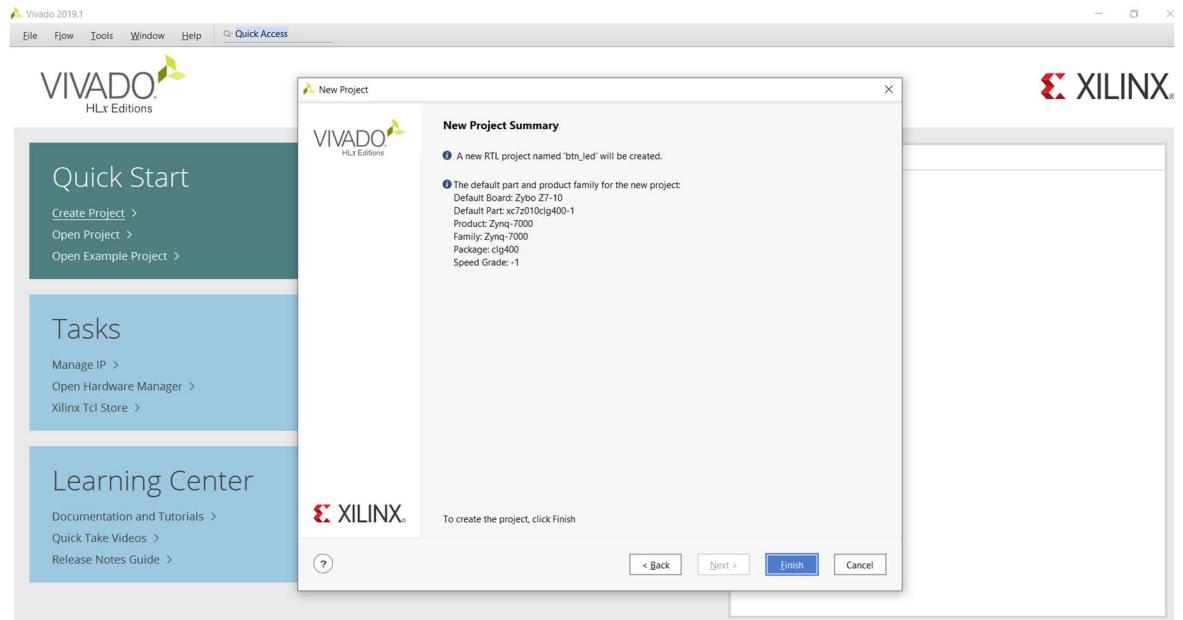


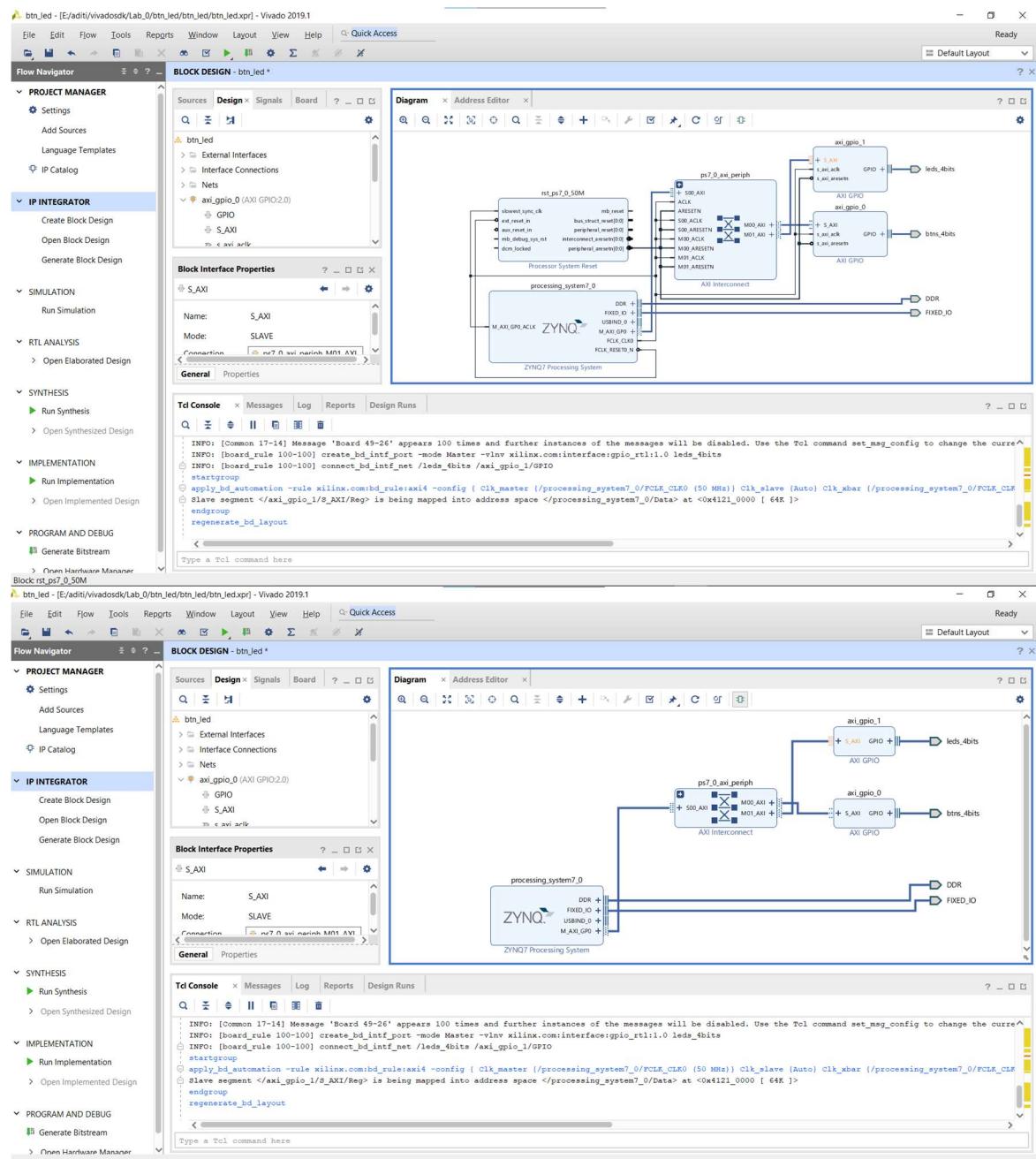


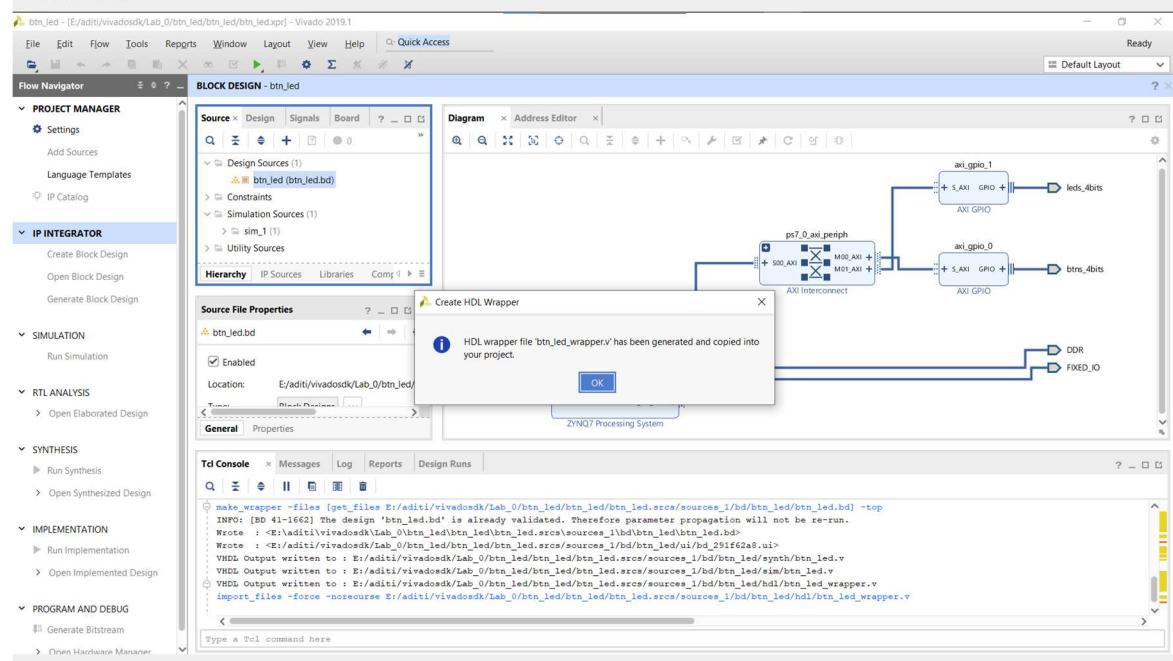
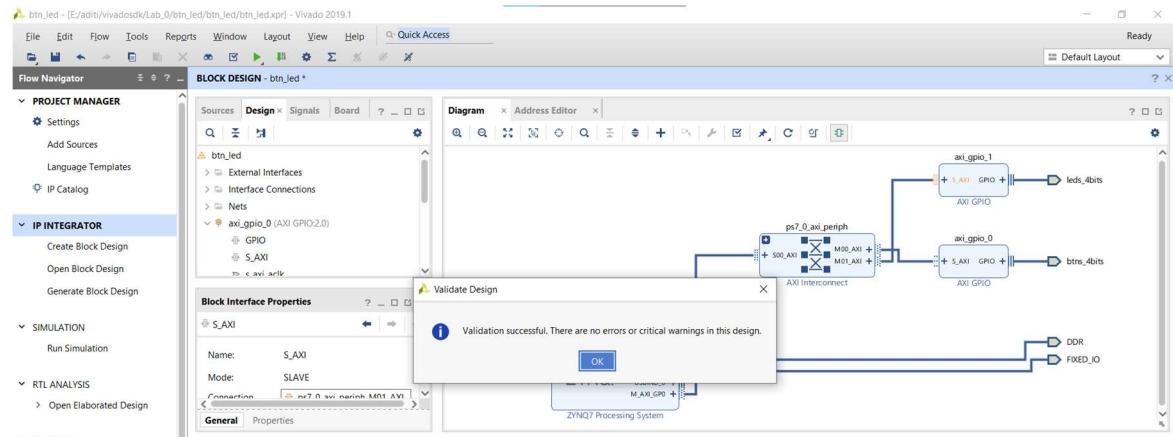


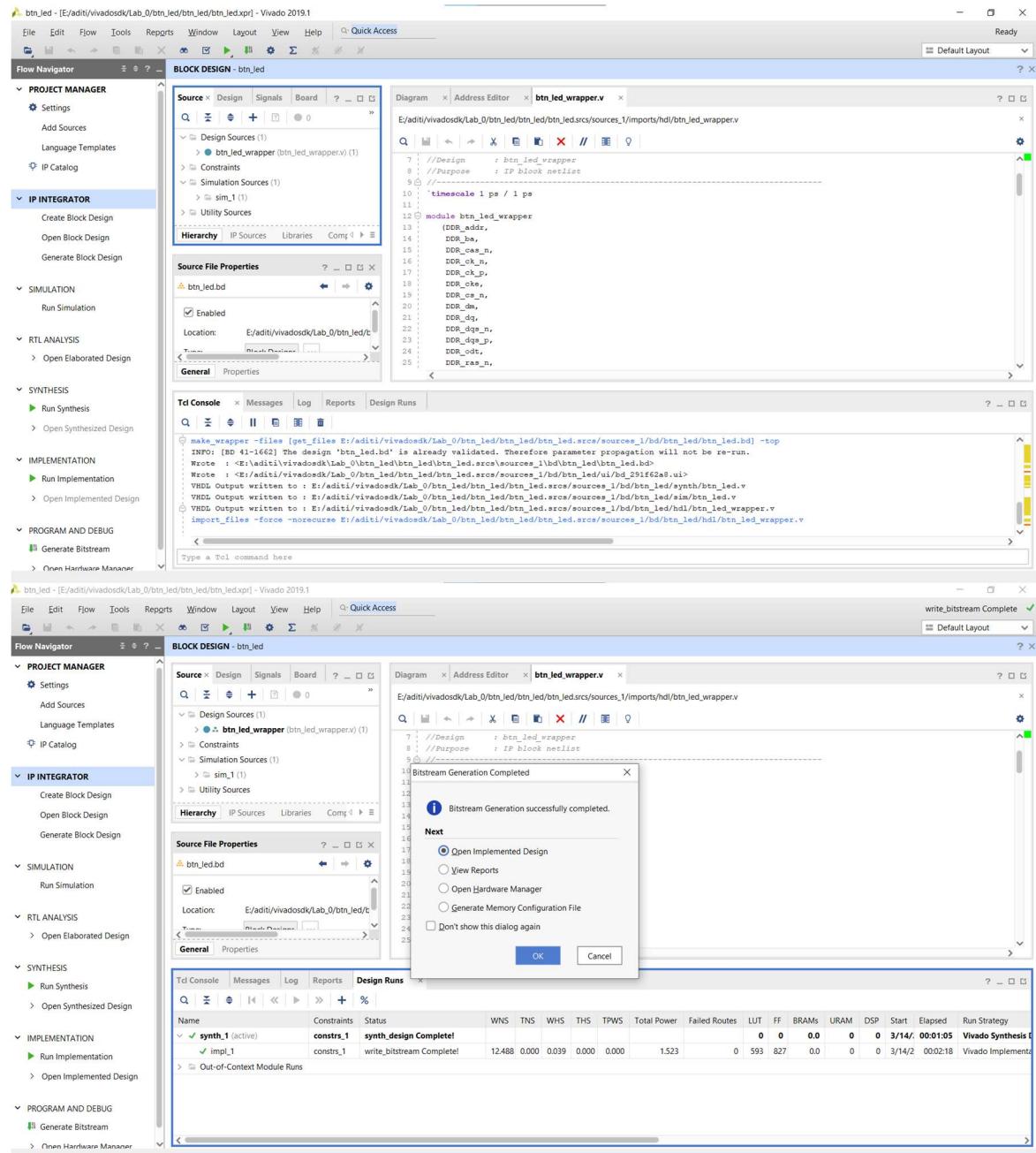


Button LED implementation









```

btn_led.sdk - C/C++ - btn_application/src(btn_led.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer system.hdf system.mss btn_led.c
  bin application
    > Binaries
    > Includes
    > Debug
  > src
    > btn_led.c
    > Iscript.tid
    > README.txt
    > Xilinx.spc
  > bin.application_bsp
  > bin_led_wrapper_hw_platform_0
    > board
      > btn_led_wrapper.bit
      > ps7_init.gplc
      > ps7_init.gplh
      > ps7_init.c
      > ps7_init.h
      > ps7_init.tcl
      > system.hdf
  > bin.application_bsp
  > bin_led_wrapper_hw_platform_0
    > board
      > btn_led_wrapper.bit
      > ps7_init.gplc
      > ps7_init.gplh
      > ps7_init.c
      > ps7_init.h
      > ps7_init.tcl
      > system.hdf

  #include "xparameters.h"
  #include "xgpio.h"
  #include "xstatus.h"
  #include "xil_printf.h"

  /* Definitions */
  #define BTNS_DEVICE_ID      XPAR_AXI_GPIO_0_DEVICE_ID
  #define LEDS_DEVICE_ID      XPAR_AXI_GPIO_1_DEVICE_ID

  #define LED_CHANNEL          1
  #define BTNS_CHANNEL         1

  XGpio btn, led;

  int main()
  {
    int Status;
    int btn_value;
    int delay;

    /* GPIO button initialization */
    Status = XGpio_Initialize(&btn, BTNS_DEVICE_ID);
    if (Status != XST_SUCCESS) {
        return XST_FAILURE;
    }

    /* GPIO led initialization */
    Status = XGpio_Initialize(&led, LEDS_DEVICE_ID);
    if (Status != XST_SUCCESS) {
        return XST_FAILURE;
    }
}

  
```

Target Connections

- Hardware Server
- Linux TCF Agent
- QEMU TcfGdbClient

Problems Tasks Console Properties SDK Terminal

CDT Build Console [bin_application]

```

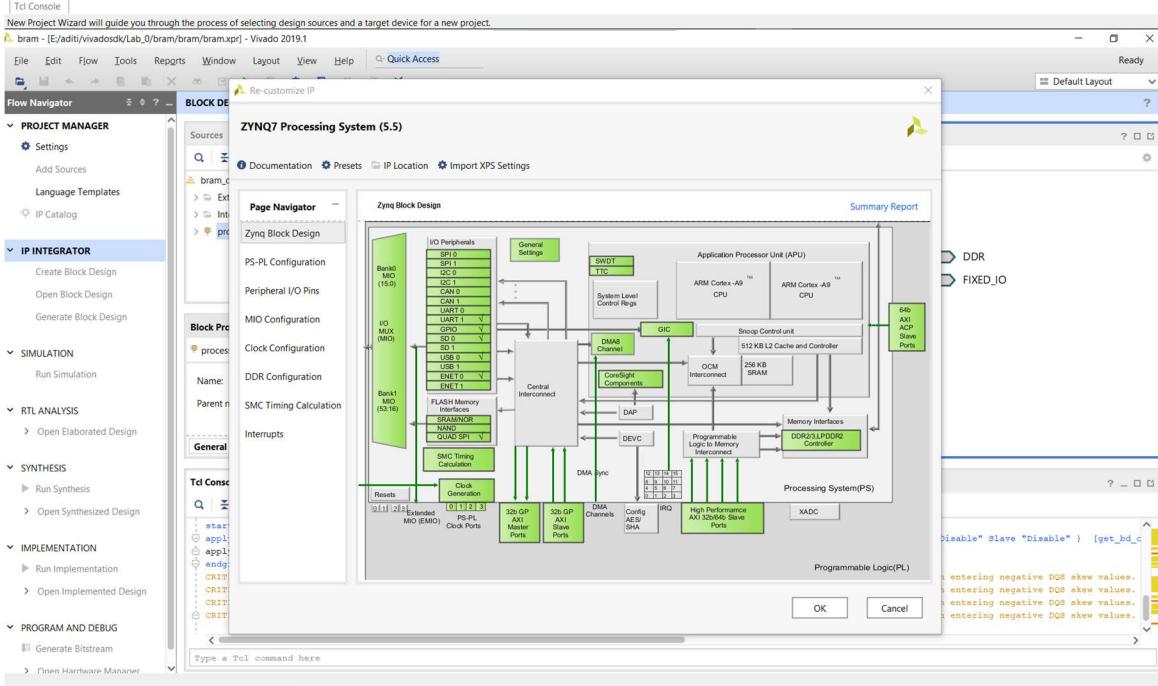
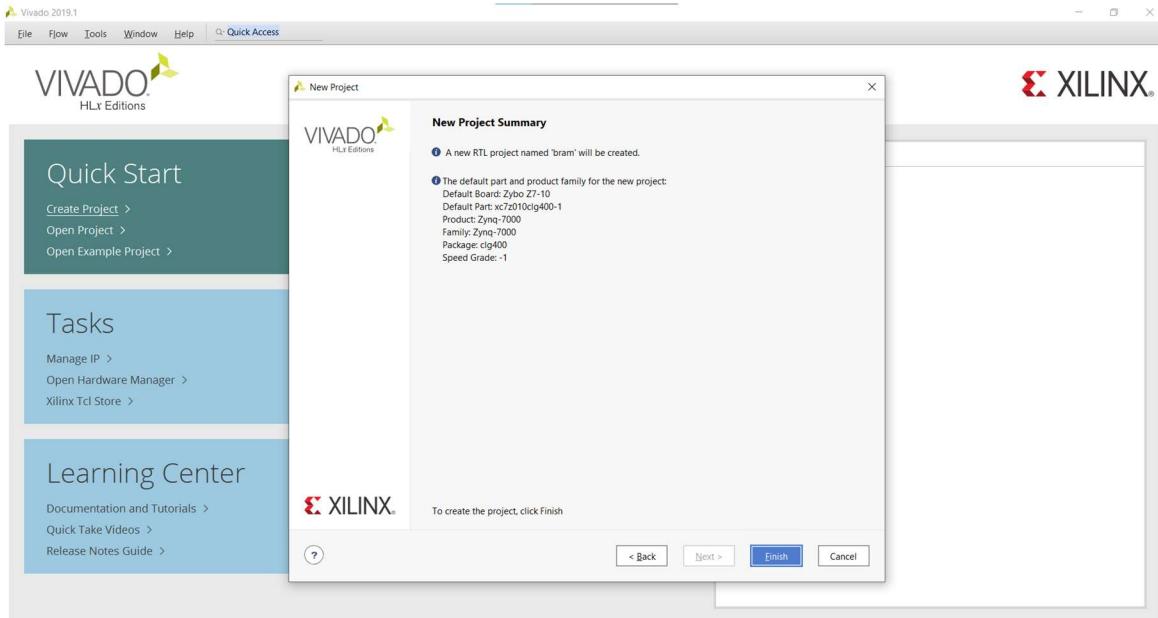
make pre-build main-build
a9-linaro-pre-build-step
.
make: Nothing to be done for 'main-build'.
13:38:52 Build Finished (took 412ms)
  
```

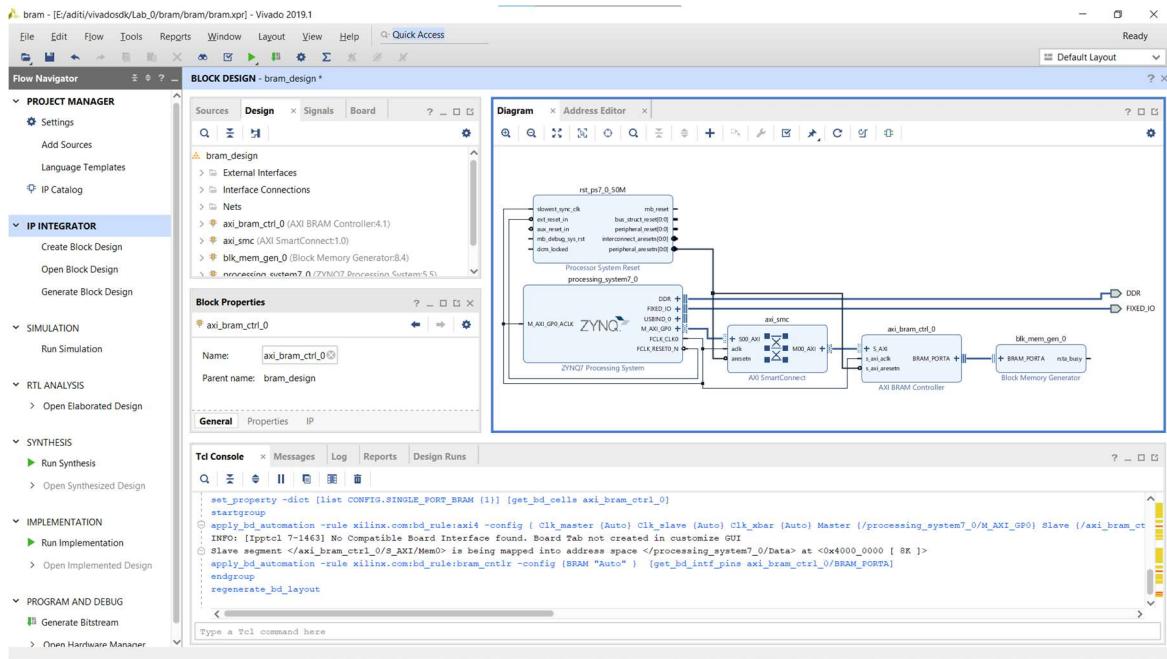
SDK Log

```

13:34:42 INFO : Registering command handlers for SDK TCF services
13:34:42 INFO : Launching XSCC server: xsct.bat -interactive E:\aditi\vviv
13:34:42 INFO : XSCC server has started successfully.
13:34:42 INFO : Successfully done setting XSCC server connection channel
13:34:47 INFO : Successfully done setting SDK workspace
13:34:47 INFO : Processing command line option -hwspec E:/aditi/vivadosdk
  
```

2. Complete BRAM memory read and write operations on Zybo Z7-10 board following the instructions in lab manuals on Canvas week#9 module





bram - [E:\aditi\viavadosdk\Lab_0\bram\bram.xpr] - Vivado 2019.1

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

BLOCK DESIGN - bram_design*

Diagram

```

graph LR
    ZYNQ[processing_system7_0] --> AXI_SMC[AXI SmartConnect]
    AXI_SMC --> AXI_BRAM[AXI BRAM Controller]
    AXI_BRAM --> DDR[DDR]
    AXI_BRAM --> BMG[Block Memory Generator]
    BMG --> DDR
  
```

Tcl Console

```

startgroup
set_property -dict {list CONFIG.PCW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.PCW_SPI1_PERIPHERAL_ENABLE {1} CONFIG.PCW_SPI1_SPI1_IO {MIO 10 .. 15}} [get_bd_cells processing_system7_0]
CRITICAL WARNING: [FSU-1] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_0 has negative value -0.050 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-2] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-3] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-4] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 . PS DDR interfaces might fail when entering negative DQS skew values.
endgroup
regenerate_bd_layout
  
```

bram - [E:\aditi\viavadosdk\Lab_0\bram\bram.xpr] - Vivado 2019.1

Flow Navigator

- PROJECT MANAGER
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BLOCK DESIGN - bram_design*

Diagram

Address Editor

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 1G)					
axi_bram_ctrl_0	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF

Tcl Console

```

startgroup
set_property -dict {list CONFIG.PCW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.PCW_SPI1_PERIPHERAL_ENABLE {1} CONFIG.PCW_SPI1_SPI1_IO {MIO 10 .. 15}} [get_bd_cells processing_system7_0]
CRITICAL WARNING: [FSU-1] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_0 has negative value -0.050 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-2] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-3] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [FSU-4] Parameter : PCW_UIFARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 . PS DDR interfaces might fail when entering negative DQS skew values.
endgroup
regenerate_bd_layout
  
```

Top Window (Validation):

The validation process was successful, indicating no errors or critical warnings.

Bottom Window (HDL Wrapper Generation):

An HDL wrapper file named 'bram_design_wrapper.v' has been generated and copied into the project.

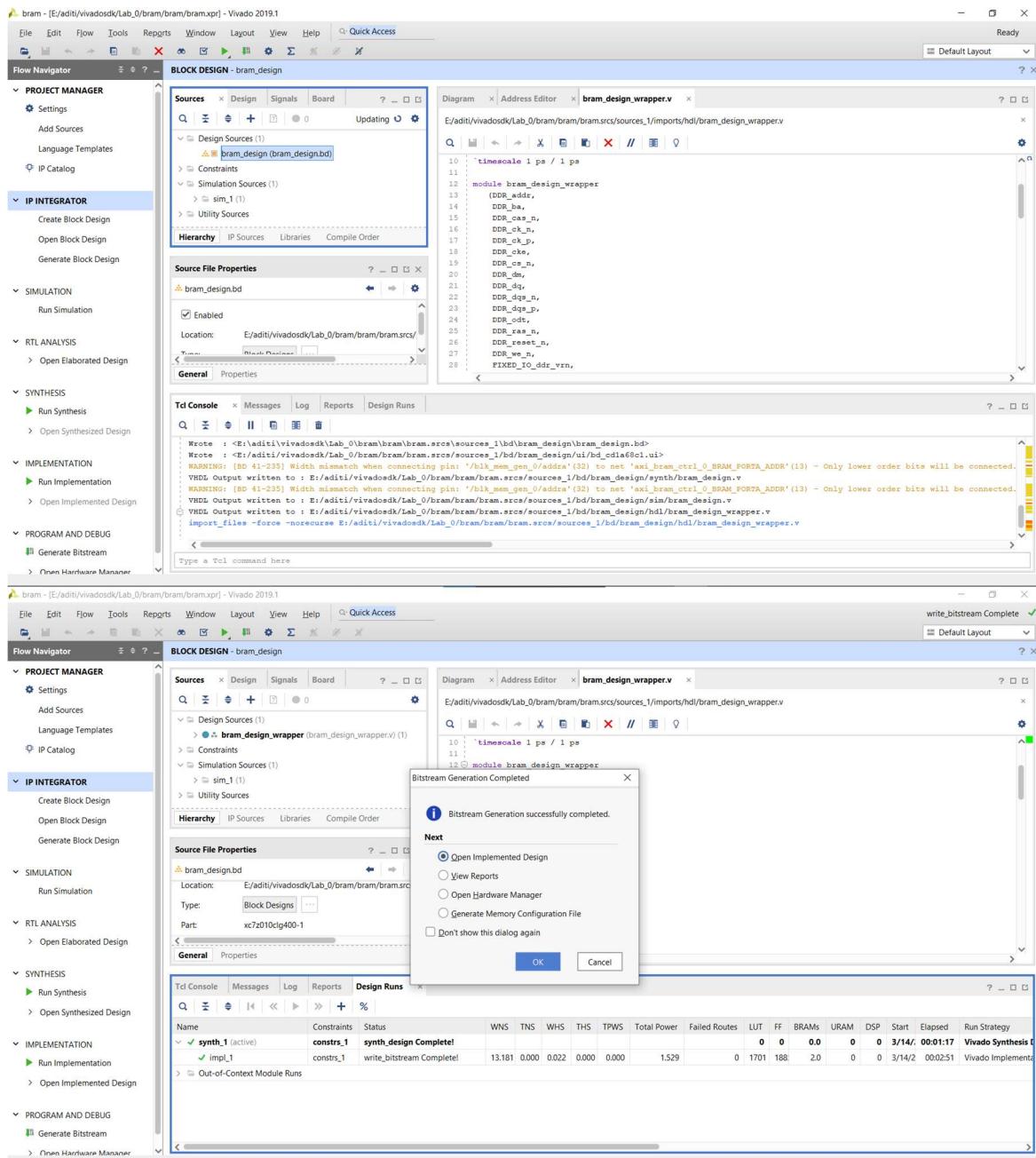
Tcl Console Output:

```

CRITICAL WARNING: [PSU-3] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 . PS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-4] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 . PS DDR interfaces might fail when entering negative DQS skew values.
INFO: [Iptpl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
WARNING: [BD 41-2180] Resetting the memory initialization file of </blk_mem_gen_0> to default.
validate_bd_design: Time (s): cpu = 00:00:12 ; elapsed = 00:00:16 . Memory (MB): peak = 1903.406 ; gain = 26.617
validate_bd_design -force
INFO: [Iptpl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
WARNING: [BD 41-2180] Resetting the memory initialization file of </blk_mem_gen_0> to default.

```

The Tcl console shows the validation and wrapper generation process along with some informational and warning messages related to board interface compatibility and memory initialization.



bram.sdk - C/C++ - bram_application/src/bramcode.c - Xilinx SDK

File Edit Navigate Search Project Run Xilinx Window Help

Project Explorer system.hdf system.mss bramcode.c

```

int word1; // integers are 32 bits wide!
int word2; // integers are 32 bits wide!
int word3; // integers are 32 bits wide!

Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0, 0x0B);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 1, 0xFF);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 2, 0x34);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 3, 0x8C);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 4, 0xEF);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 5, 0xBE);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 6, 0xAD);
Xil_Out8(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 7, 0xDE);

Xil_Out16(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x10, 0x1209);
Xil_Out16(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x12, 0xFE31);
Xil_Out16(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x14, 0x6587);
Xil_Out16(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x16, 0xAAA);

Xil_Out32(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x20, 0x1234abcd);

while(1)
{
    word1 = Xil_In32(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR);
    word2 = Xil_In32(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 4);
    word3 = Xil_In32(XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + 0x20);

    printf("Word1 = 0x%08x\n", word1);
    printf("Word2 = 0x%08x\n", word2);
}

```

Problems Tasks Console Properties SDK Terminal

Target Connections Connected to: Serial (COMA, 115200, 0, 8)

Word1 = 0x8c34ffab
Word2 = 0xdeadbeef
Word3 = 0x1234abcd

SDK Log

```

stop
ps7_init
ps7_init: /opt/Xilinx/Vivado/2018.2/filter {name == "ARM#0" && jtag_cable_name == "Digital fast processor targets"} -> ps7_init
targets -set -nocase -filter {name == "ARM#0" && jtag_cable_name == "Digital fast processor targets"} -> ps7_init
-----End of Script-----

```

