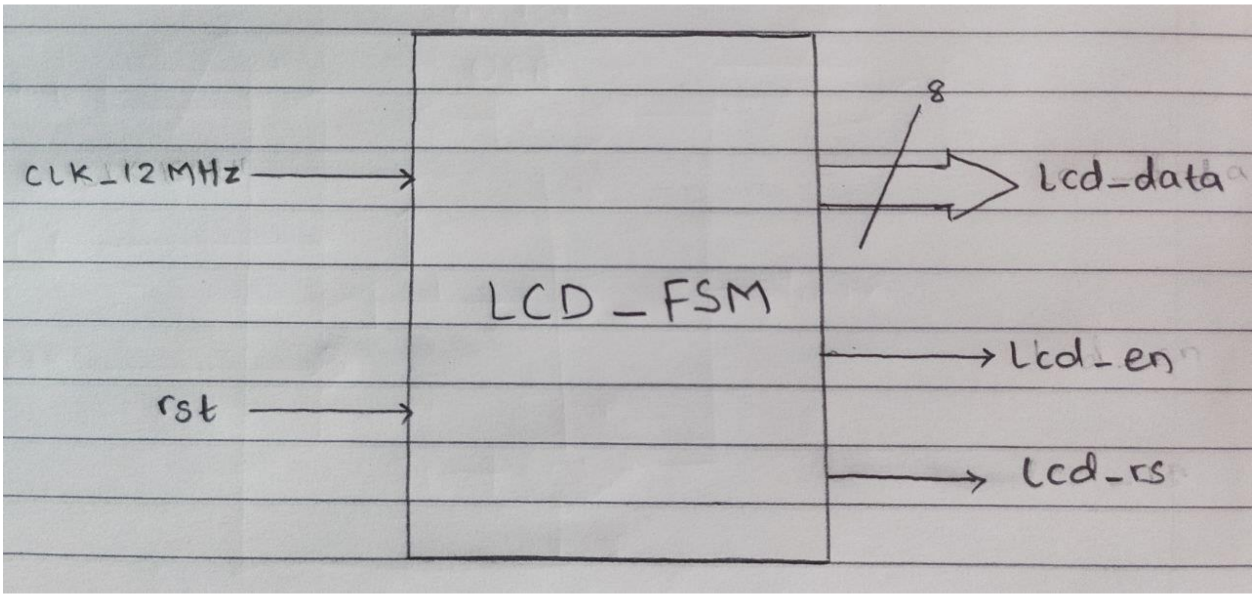
Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	A.5
Assignment Name	:	FPGA-LCD Interfacing
Date Of Performance	:	

BLOCK DIAGRAM



FUNCTION TABLE

rst	clk_12MHz / 65536	lcd_data	lcd_rs	lcd_en
1	x	38h	0	x
0	↑	06h	0	↑
0	↑	0Ch	0	↑
0	↑	01h	0	↑
0	↑	50h (P)	1	↑
0	↑	49h (I)	1	↑
0	↑	43h (C)	1	↑
0	↑	54h (T)	1	↑
0	↑	20h ( )	1	↑

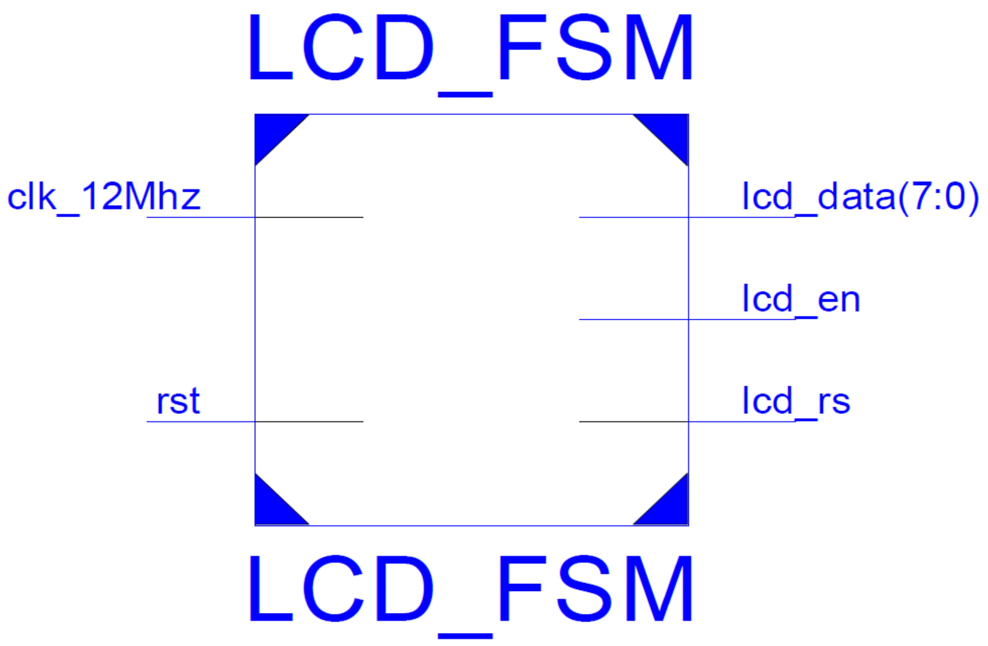
MAIN VHDL MODEL (MVM)

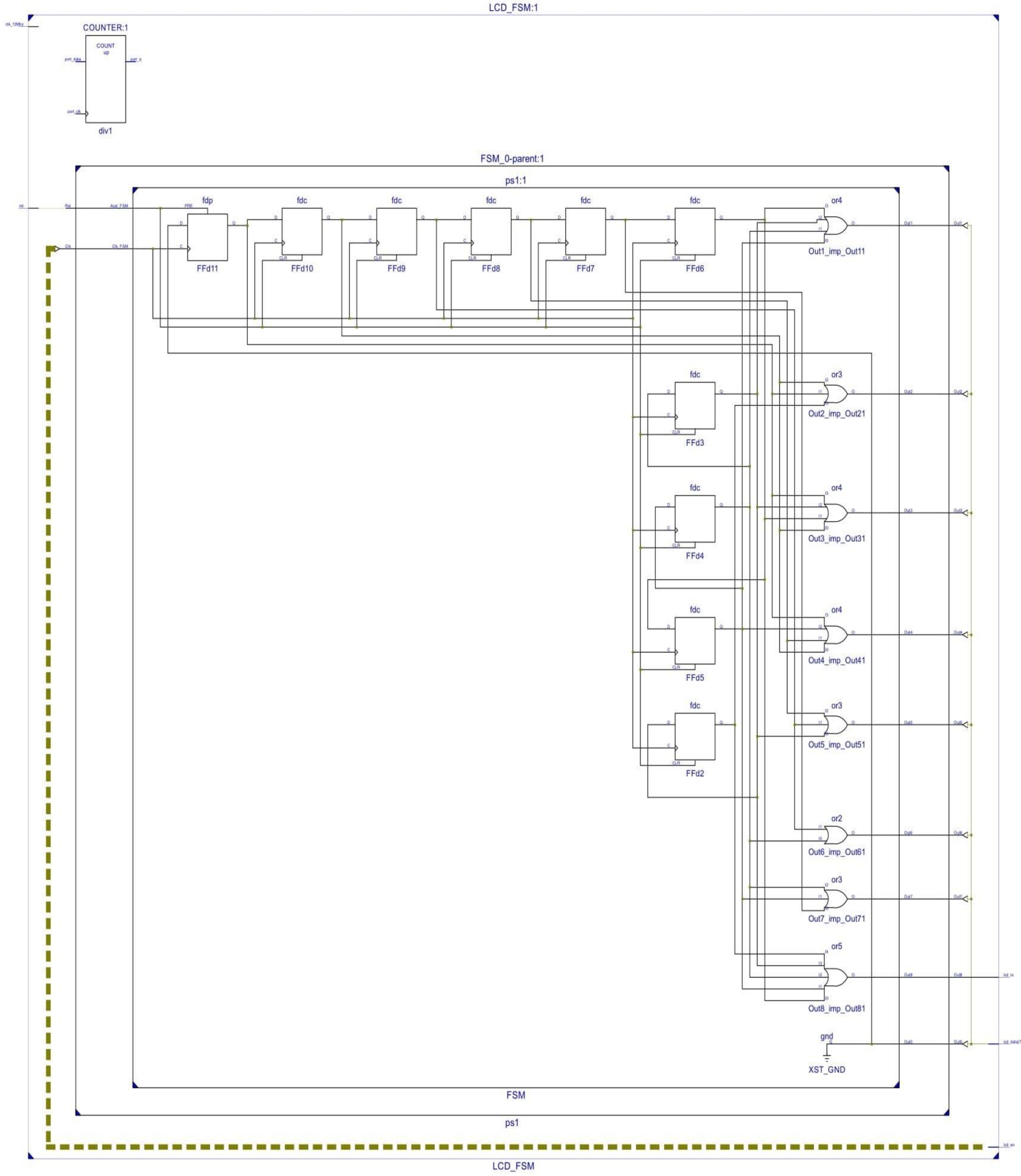
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity LCD_FSM is
Port (     rst : in std_logic;                     -- reset
        clk_12Mhz : in std_logic;             -- high freq. clock
        lcd_rs : out std_logic;                -- LCD RS control
        lcd_en : out std_logic;                -- LCD Enable
        lcd_data : out std_logic_vector(7 downto 0));       -- LCD Data port
end LCD_FSM;

architecture Behavioral of LCD_FSM is

signal div : std_logic_vector(15 downto 0); --- delay timer 1
signal clk_fsm,lcd_rs_s: std_logic;
-- LCD controller FSM states
type state is (reset,func,mode,cur,clear,d0,d1,d2,d3,d4,hold);
signal ps1,nx      : state;
signal dataout_s  : std_logic_vector(7 downto 0); --- internal data command multiplexer

begin

----- clk divider --------------------------------
process(rst,clk_12Mhz)
begin
if(rst = '1')then
          div <= (others=>'0');
elsif( clk_12Mhz'event and clk_12Mhz ='1')then

          div <= div + 1;
          end if;

end process;
--------------------------------------------------
clk_fsm <= div(15);

----- Presetn state Register -----------------------
process(rst,clk_fsm)
begin
if(rst = '1')then
          ps1      <= reset;
elsif (rising_edge(clk_fsm)) then
          ps1      <= nx;

end if;
end process;
```

```
----- state and output  decoding process
process(ps1)
begin
case(ps1) is

        when reset =>
                        nx      <= func;
                        lcd_rs_s        <= '0';
                        dataout_s       <= "00111000";          -- 38h

        when func       =>
                        nx      <= mode;
                        lcd_rs_s        <= '0';
                        dataout_s       <= "00111000";          -- 38h

        when mode       =>
                        nx      <= cur;
                        lcd_rs_s        <= '0';
                        dataout_s       <= "00000110";          -- 06h

        when cur        =>
                        nx      <= clear;
                        lcd_rs_s        <= '0';
                        dataout_s       <= "00001100";          -- 0Ch  curser at starting point of
line1

        when clear=>
                        nx      <= d0;
                        lcd_rs_s        <= '0';
                        dataout_s       <= "00000001";          -- 01h

        when d0         =>
                        lcd_rs_s        <= '1';
                        dataout_s       <= "01010000";          -- P ( Decimal = 80 , HEX = 50 )
                        nx      <= d1;

        when d1         =>
                        lcd_rs_s        <= '1';
                        dataout_s       <= "01001001";          -- I ( Decimal = 73 , HEX = 49 )
                        nx      <= d2;

        when d2         =>
                        lcd_rs_s        <= '1';
                        dataout_s       <= "01000011";          -- C ( Decimal = 67 , HEX = 43 )
                        nx      <= d3;

        when d3         =>
                        lcd_rs_s        <= '1';
                        dataout_s       <= "01010100";          -- T ( Decimal = 84 , HEX = 54 )
                        nx      <= d4;
```

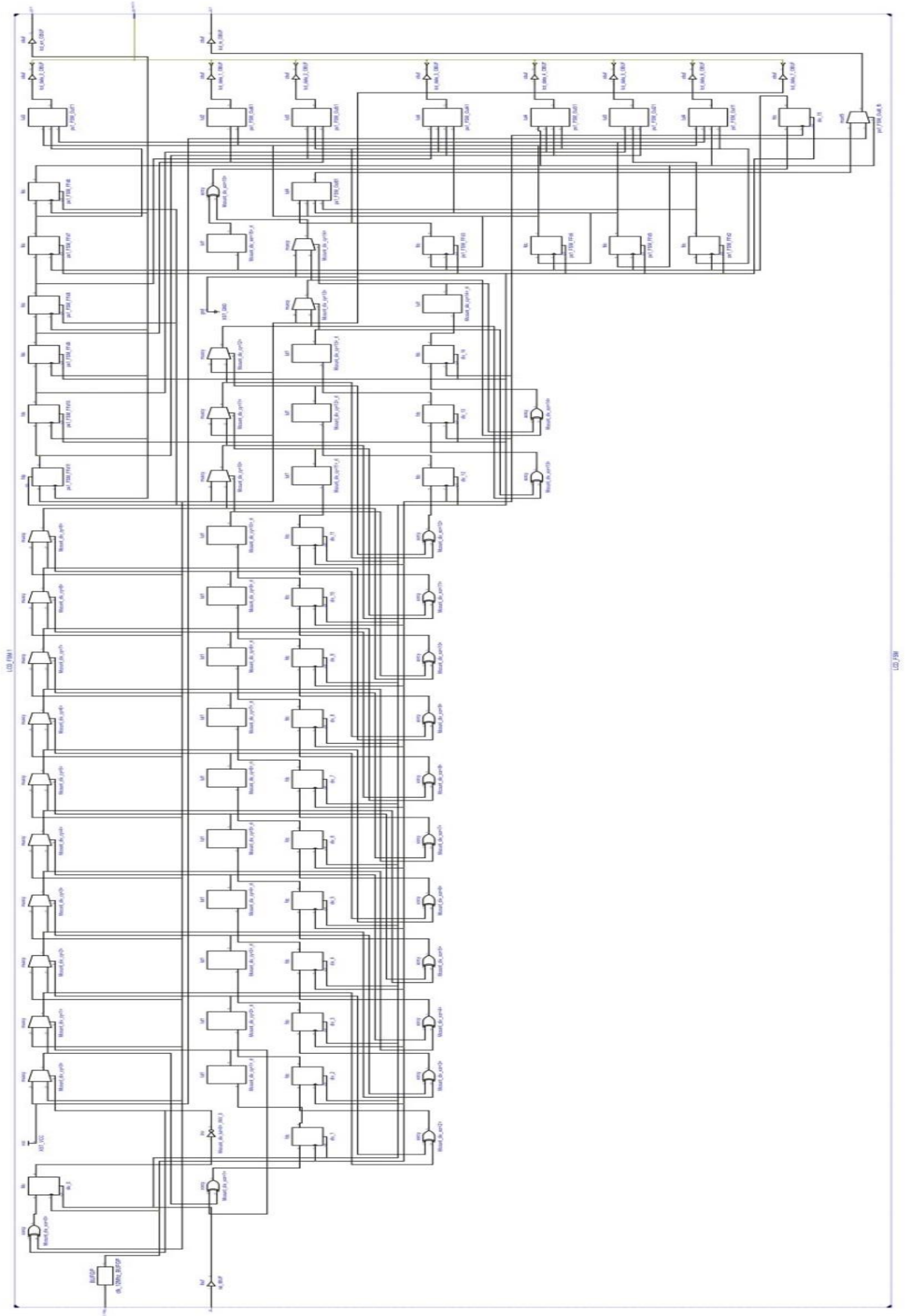
```
          when d4       =>
                        lcd_rs_s      <= '1';
                        dataout_s     <= "00100000";          -- space ( Decimal = 32 , HEX = 20 )
                        nx      <= hold;

          when hold     =>
                        lcd_rs_s      <= '0';
                        dataout_s     <= "00000000";         -- hold  ( Decimal = 32 , HEX = 00 ) ,
NULL
                        nx      <= hold;

when others=>
                        nx      <= reset;
                        lcd_rs_s      <= '0';
                        dataout_s     <= "00000001";          -- CLEAR ( Decimal = 1 , HEX = 01 )
end case;
end process;


lcd_en <= clk_fsm;
lcd_rs <= lcd_rs_s;
lcd_data <= dataout_s;

end Behavioral;
```

RTL SCHEMATIC:




LCD_FSM:1
clk_12Mhz
COUNTER:1
COUNT
up
port_data
port_q
port_clk
div1
FSM_0-parent:1
ps1:1
rst
Rst
Acst_FSM
Clk
Clk_FSM
fdp
PRE
FFd11
fdc
FFd10
FFd9
FFd8
FFd7
FFd6
FFd3
FFd4
FFd5
FFd2
D
C
Q
CLR
or4
Out1_imp_Out11
or3
Out2_imp_Out21
or4
Out3_imp_Out31
or4
Out4_imp_Out41
or3
Out5_imp_Out51
or2
Out6_imp_Out61
or3
Out7_imp_Out71
or5
Out8_imp_Out81
gnd
XST_GND
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out0
lcd_rs
lcd_data(7:0)
lcd_en
FSM
ps1
LCD_FSM

TECHNOLOGY SCHEMATIC



SYNTHESIS REPORT

a) Device Utilization Summary:

```
=========================================================================
*                      Final Report                           *
=========================================================================
Final Results
RTL Top Level Output File Name     : LCD_FSM.ngr
Top Level Output File Name         : LCD_FSM
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 12

Cell Usage :
# BELS                             : 58
#      GND                         : 1
#      INV                         : 1
#      LUT1                        : 15
#      LUT2                        : 1
#      LUT3                        : 3
#      LUT4                        : 4
#      MUXCY                       : 15
#      MUXF5                       : 1
#      VCC                         : 1
#      XORCY                       : 16
# FlipFlops/Latches                : 26
#      FDC                         : 25
#      FDP                         : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 11
#      IBUF                        : 1
#      OBUF                        : 10
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                      15  out of   2448     0%
 Number of Slice Flip Flops:            26  out of   4896     0%
 Number of 4 input LUTs:                24  out of   4896     0%
 Number of IOs:                         12
 Number of bonded IOBs:                 12  out of    158     7%
 Number of GCLKs:                        1  out of     24     4%
```

b) TIMING REPORT:

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

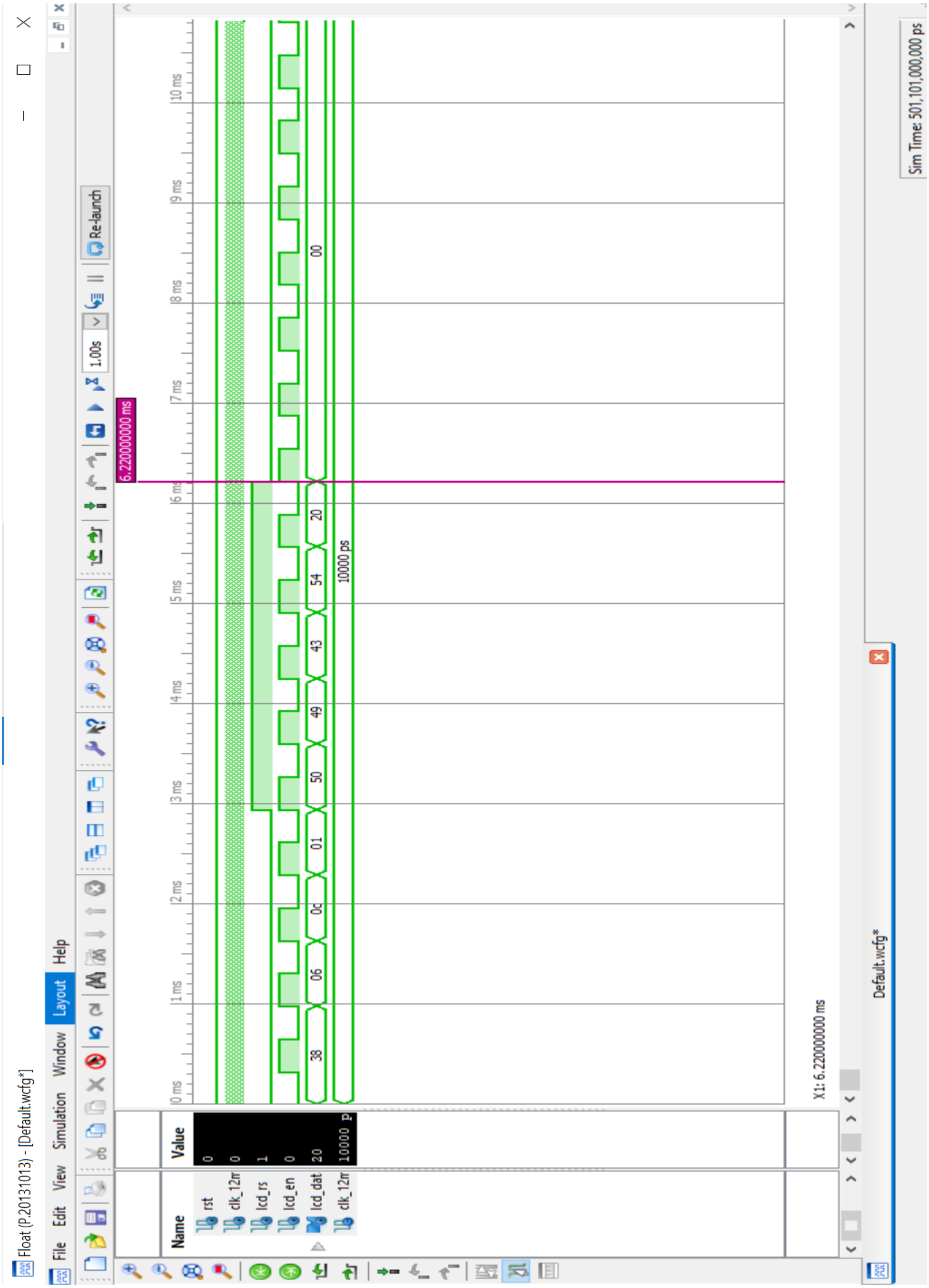
```
   FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
   GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk_12Mhz                          | BUFGP                  | 16    |
div_15                             | NONE(ps1_FSM_FFd11)    | 10    |
-----------------------------------+------------------------+-------+
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST
with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these
buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst                                | IBUF                   | 26    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

  Minimum period: 3.676ns (Maximum Frequency: 272.072MHz)
  Minimum input arrival time before clock: No path found
  Maximum output required time after clock: 5.537ns
  Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

TESTBENCH VHDL MODEL (TVM)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY LCD_Test IS
END LCD_Test;

ARCHITECTURE behavior OF LCD_Test IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT LCD_FSM
   PORT(
        rst : IN  std_logic;
        clk_12Mhz : IN  std_logic;
        lcd_rs : OUT  std_logic;
        lcd_en : OUT  std_logic;
        lcd_data : OUT  std_logic_vector(7 downto 0)
       );
   END COMPONENT;


  --Inputs
  signal rst : std_logic := '0';
  signal clk_12Mhz : std_logic := '0';

           --Outputs
  signal lcd_rs : std_logic;
  signal lcd_en : std_logic;
  signal lcd_data : std_logic_vector(7 downto 0);

  -- Clock period definitions
  constant clk_12Mhz_period : time := 10 ns;

BEGIN

           -- Instantiate the Unit Under Test (UUT)
  uut: LCD_FSM PORT MAP (
         rst => rst,
         clk_12Mhz => clk_12Mhz,
         lcd_rs => lcd_rs,
         lcd_en => lcd_en,
         lcd_data => lcd_data
       );

  -- Clock process definitions
  clk_12Mhz_process :process
  begin
```

```
                         clk_12Mhz <= '0';
                         wait for clk_12Mhz_period/2;
                         clk_12Mhz <= '1';
                         wait for clk_12Mhz_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      rst <= '1';
      wait for 20 ns;

     rst <= '0';
      -- insert stimulus here

      wait;
   end process;

END;
```

ISIM WAVEFORMS



Float (P.20131013) - [Default.wcfg*]

Name	Value
rst	0
clk_12r	0
lcd_rs	1
lcd_en	0
lcd_dat	20
clk_12r	10000 p

X1: 6.220000000 ms

Sim Time: 501,101,000,000 ps

PIN-LOCKING REPORT

```
# PlanAhead Generated physical constraints

NET "clk_12Mhz" LOC = P80;
NET "rst" LOC = P204;
NET "lcd_rs" LOC = P48;
NET "lcd_en" LOC = P49;
NET "lcd_data[0]" LOC = P47;
NET "lcd_data[1]" LOC = P41;
NET "lcd_data[2]" LOC = P39;
NET "lcd_data[3]" LOC = P35;
NET "lcd_data[4]" LOC = P33;
NET "lcd_data[5]" LOC = P31;
NET "lcd_data[6]" LOC = P29;
NET "lcd_data[7]" LOC = P24;
```

CONCLUSION

Thus, we have:

1) Modeled a FPGA-LCD Interfacing using Behavioral Modeling Style.
2) Observed following Schematics: **RTL** & **Technology Schematics** generated **Post-Synthesis**.
3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers &D FFs used out of the available device resources.
4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5) Written a TESTBENCH to verify the functionality of FPGA-LCD Interfacing & verified the functionality asper the FUNCTION-TABLE, by observing ISIM Waveforms.
6) Used PlanAhead Editor for pin-locking.
7) Prototyped the FPGA **XC3S250EPQ208-5** to realize FPGA-LCD Interfacing & verified its operation by givingsuitable input combinations.