Aditya Reddy

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Education

Manipal University Jaipur **Aug 2024 – May 2028**

Bachelor of Technology in Electronics and Communication Engineering *Jaipur, India*

Projects

Low Latency Trading Gateway | C++, FIX Protocol, Lock-Free Programming **GitHub Link**

- Engineered high-performance trading gateway using lock-free queues and memory pools, reducing synchronization bottlenecks by 85%
- Implemented zero-copy FIX protocol parsing with state machines, achieving sub-2s parsing with 1.4s average latency
- Optimized tick-to-trade latency to 10–15s average with 2.8s minimum, sustaining 400+ messages at 98% execution rate
- Applied CPU pinning and cache-aligned memory allocation to eliminate scheduling delays and improve data locality

HTTP/1.1 Web Server | C, POSIX Sockets, Multithreading **GitHub Link**

- Architected custom HTTP/1.1 server in C with raw POSIX sockets and thread pool, eliminating external library dependencies
- Implemented complete HTTP request parsing, static file serving, and MIME type detection with directory traversal protection
- Achieved 11.5K+ requests/sec throughput with 8.7ms average latency under 100 concurrent clients using ApacheBench
- Designed connection pooling and keep-alive mechanisms to reduce TCP handshake overhead by 40%

Skills

- **Programming Languages:** C, C++, Python, Verilog, SystemVerilog, Assembly (RISC-V, x86)
- **Tools & Technologies:** Git, Make, Linux, GCC, Clang, Shell Scripting, Docker, LaTeX
- **Hardware & Simulation:** LTspice, GTKWave, Vivado, Verilator, Icarus Verilog, RISC-V Toolchain
- **Libraries & Frameworks:** POSIX Sockets, STL, FIX Protocol

Activities

- Volunteered at Bison Asha School for Special Needs, supporting educational activities and organizing inclusive events (2022 – 2024)