Aditya Reddy

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Education

- **Manipal University Jaipur**, Jaipur, India *2024 – 2028*
  Bachelor of Technology in Electronics and Communication Engineering *Jaipur, Rajasthan*
  Relevant Coursework: Digital Design, Signals and Systems, Linear Integrated Circuits

Projects

Low Latency Trading Gateway | *C++, FIX Protocol, Lock-Free Programming* GitHub Link

- Engineered a high-performance trading gateway in C++ using lock-free queues, memory pools, and CPU pinning to eliminate synchronization and scheduling bottlenecks.
- Implemented zero-copy FIX protocol parsing with **state machines** and **string views**, achieving **sub-2µs** parsing efficiency with **1.4µs average latency**.
- Optimized tick-to-trade latency to **10–15µs average** with **2.8µs minimum**, sustaining throughput of **400+ messages** at a **98% execution rate**.

HTTP/1.1 Web Server | *C, POSIX Sockets, Multithreading* GitHub Link

- Architected a custom HTTP/1.1 server entirely in C with raw POSIX sockets and a thread pool architecture, removing reliance on external libraries.
- Implemented complete HTTP request parsing, static file serving, MIME type detection, and robust safeguards against directory traversal exploits.
- Benchmarked with ApacheBench: sustained **11.5K+ requests/sec** and achieved **8.7ms average latency** under **100 concurrent clients**.

Activities & Extracurriculars

- Volunteered at **Bison Asha School for Special Needs**, supporting educational activities and organizing inclusive events over two years.
- Completed the **Harvard CS50P Certificate** in Python programming, focusing on problem solving, data structures, and I/O systems.
- Reached the penultimate round at **Elicit Hacks 9.0 (MUJ)**.

Technical Skills

- **Programming & HDL:** C, C++, Python, Verilog, SystemVerilog
- **Tools & Environments:** Git, Make, Linux CLI, GCC, Shell Scripting, LaTeX
- **Circuit & Simulation Tools:** LTspice, GTKWave, Vivado
- **Hardware/EDA Frameworks:** Verilator, Icarus Verilog, RISC-V Toolchain