

Aditya Reddy

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EDUCATION

- **Manipal University Jaipur**, Jaipur, India *2024 – 2028 (expected)*
Bachelor of Technology in Electronics and Communication Engineering
- **Army Public School Bolarum**, Secunderabad, India *2014 – 2023*

PROJECTS

- Criver: Minimal HTTP/1.1 Web Server** | *C, POSIX Sockets* GitHub Link
- Built a custom HTTP/1.1 web server from scratch using raw POSIX sockets and standard C, with zero external dependencies.
 - Implemented full request parsing, static file serving with MIME type detection, and directory traversal protection.
- Hamming (7,4) Error Correcting Code** | *C, Verilog* GitHub Link
- Designed a Hamming (7,4) encoder/decoder in C and Verilog to detect and correct single-bit errors in data transmission.
- Laplacian Edge Detection** | *C* GitHub Link
- Developed an image processing tool in C using the Laplacian operator to detect intensity discontinuities in grayscale images.
- Sudoku Solver and Generator** | *C* GitHub Link
- Implemented a backtracking-based Sudoku solver in C with puzzle generation and difficulty tuning capabilities.

ACTIVITIES & EXTRACURRICULARS

- **Elicit Hacks 9.0 MUJ Hackathon** *October 2024*
- **Harvard CS50P Certificate** *August 2023*
- **Volunteer – Bison Asha School** *May 2021 – August 2023*

TECHNICAL SKILLS

Programming: C, Python, Verilog, SystemVerilog, Bash
Tools and Frameworks: Git, Make, Linux CLI, GCC, Shell scripting, LaTeX, GTKWave, Verilator, Icarus Verilog, RISC-V Toolchain, Vivado

INTERESTS

Hardware-Software Co-design, RISC-V, Digital Design (HDL)