Aditya Reddy

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Education

- **Manipal University Jaipur**, Jaipur, India *2024 – 2028*
  Bachelor of Technology in Electronics and Communication Engineering *Jaipur, Rajasthan*

Projects

HTTP/1.1 Web Server | *C, POSIX Sockets, Multithreading* GitHub Link

- Built a custom HTTP/1.1 server from scratch in C using raw POSIX sockets and a thread pool architecture, with zero external dependencies.
- Implemented full HTTP request parsing, static file serving, MIME type detection, and protection against directory traversal attacks.
- Benchmarked with ApacheBench: sustained **11.5K+ requests/sec** and **8.7ms average latency** under **100 concurrent clients**.

Hamming (7,4) Error Correcting Code | *C, Verilog* GitHub Link

- Designed a Hamming (7,4) encoder/decoder in C and Verilog to detect and correct single-bit errors in data transmission.

Laplacian Edge Detection | *C* GitHub Link

- Developed an image processing tool in C using the Laplacian operator to detect intensity discontinuities in grayscale images.

Sudoku Solver and Generator | *C* GitHub Link

- Implemented a backtracking-based Sudoku solver in C with puzzle generation and difficulty tuning capabilities.

Activities & Extracurriculars

- Qualified to penultimate round at **Elicit Hacks 9.0 (MUJ)**,
- Completed the **Harvard CS50P Certificate** in Python programming, focusing on problem solving, data structures, and I/O systems.
- Volunteered at **Bison Asha School for Special Needs**, assisting in educational activities and organizing inclusive events over two years.

Technical Skills

- **Languages:** C/C++, Python, Verilog, SystemVerilog, Bash
- **Developer Tools:** Git, Make, Linux CLI, GCC, Shell scripting, LaTeX, GTKWave
- **Technologies/Frameworks:** Verilator, Icarus Verilog, RISC-V Toolchain, Vivado, GTKWave