VLSI Project

4-Input ALU:

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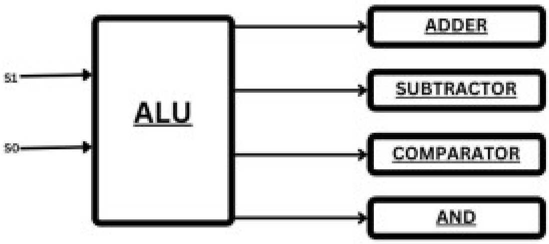
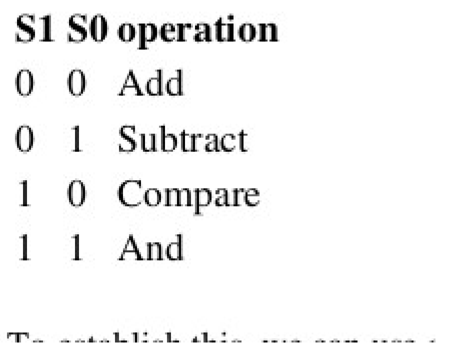
Aim:
Design an ALU that can perform a 4-Bit addition, subtraction, comparison, ANDing. Estimate the critical path, maximum delay possible in the circuit. Design the layout of your ALU, clearly indicate the location of each standard cell in the design.

Block Diagram:



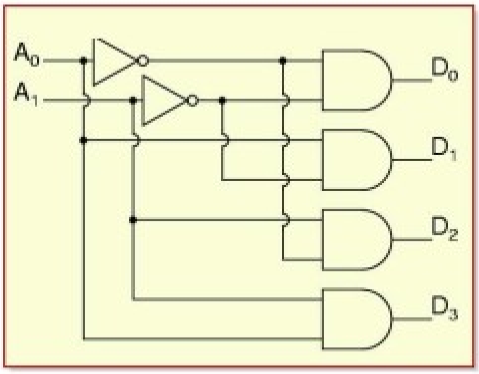
DIFFERENT COMPONENTS OF THE ALU:

1) DECODER:
To do this, we first make the decoder,



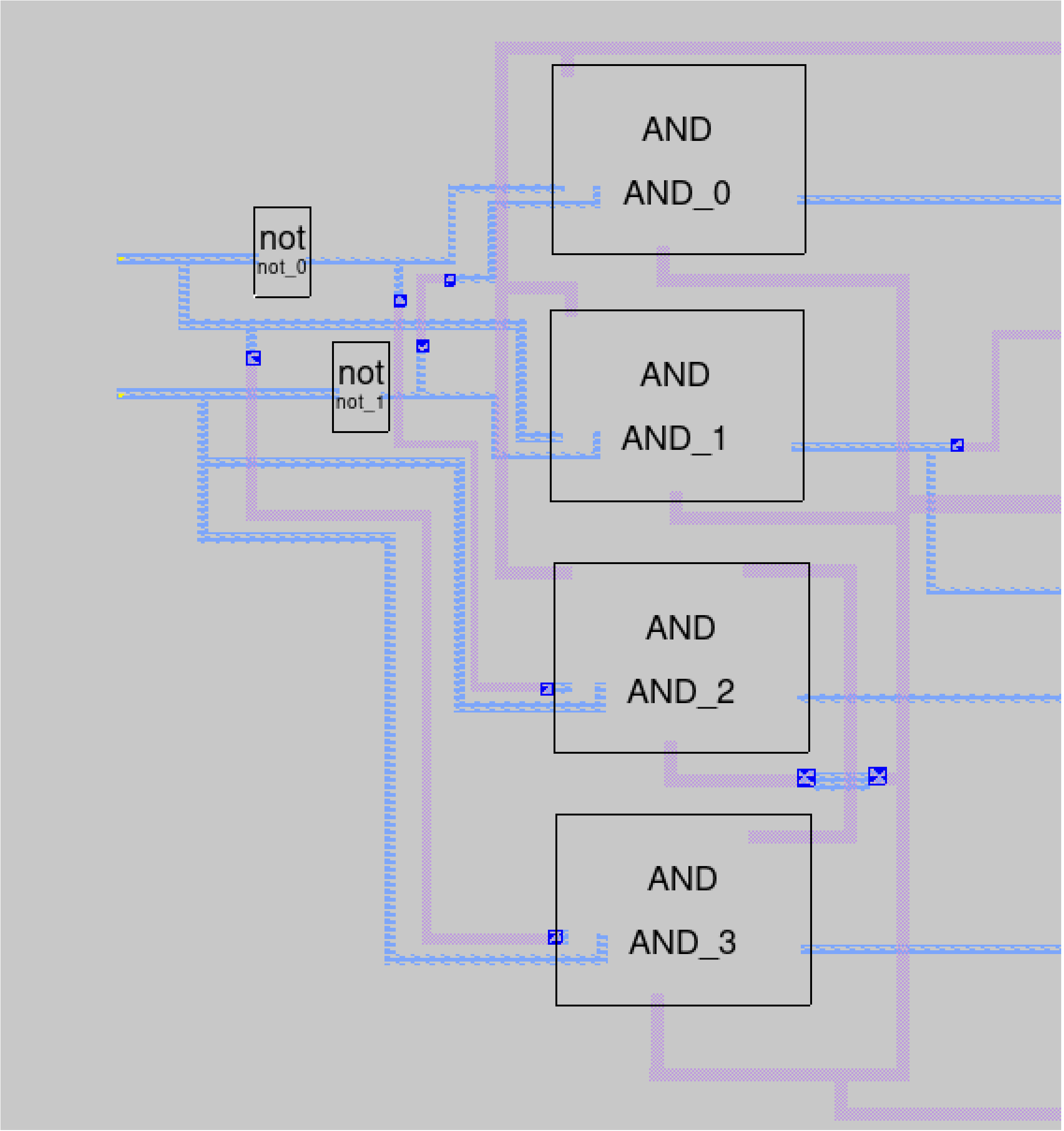
S1	S0	operation
0	0	Add
0	1	Subtract
1	0	Compare
1	1	And

To establish this, we can use a



The enables for the following circuits are as follows; D0 – Adder; D1 – Subtractor; D2 – Comparator; D3 – And.

MAGIC LAYOUT: (for decoder)



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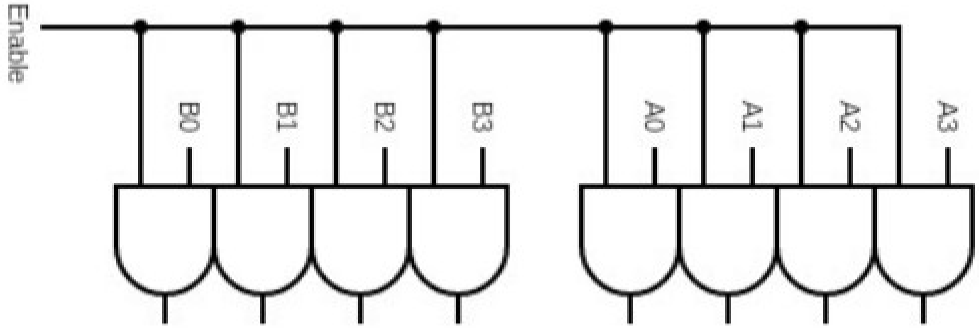
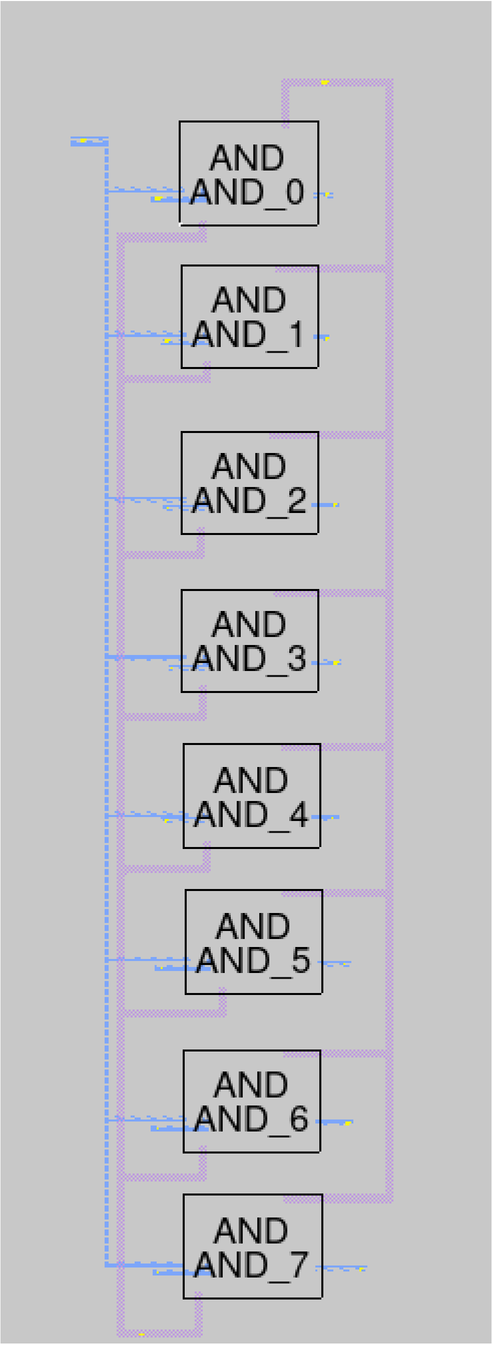
2)ENABLE block:

In the circuit, the enable block is made up of AND gates in which the 4-bits inputs in the form A3A2A1A0 AND B3B2B1B0 are given to the differnt modules when they are enabled ortherwise are given 0.



MAGIC layout for enable:



3)Differnt MODULES

Explaining the different modules:

1) when S0=0 &S1=0 (ADDER) & S0=0 &S1=1(SUBTRACTOR):

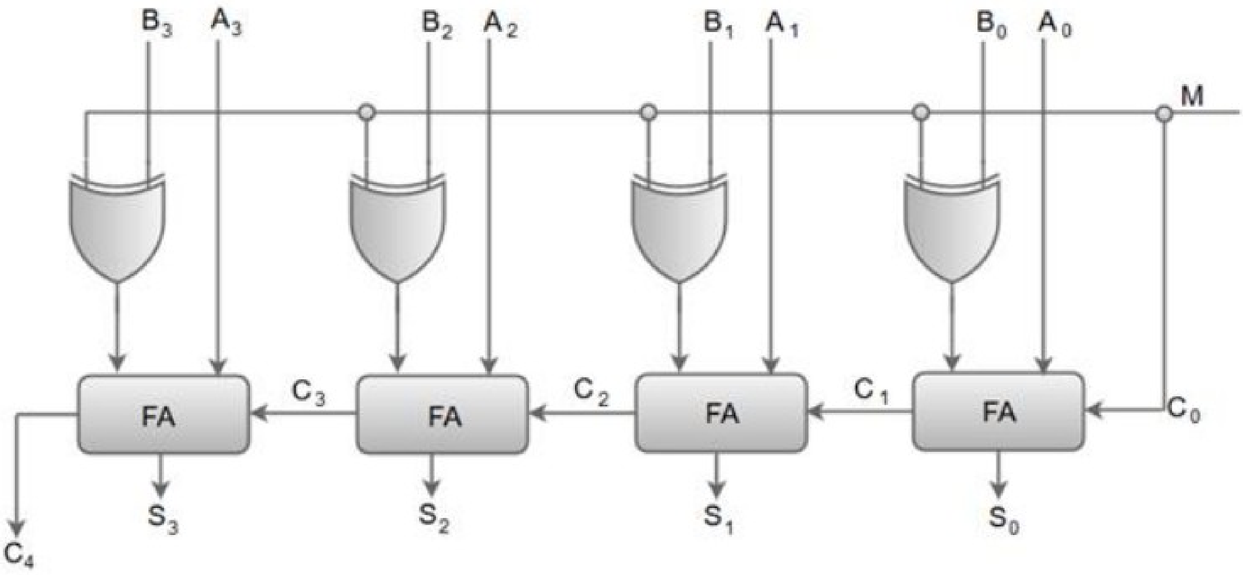
Here instead of making a separate Adder and Subtractor we can use a single block which can both act as adder and subtractor. So here we can tie out C0/M wite to S0 directly which would give us an ADDER if input is 00 and a SUBTRACTOR if out input is 01.

Adder operation is A3A2A1A1+ B3B2B1B0

Subtractor operation is A3A2A1A1- B3B2B1B0

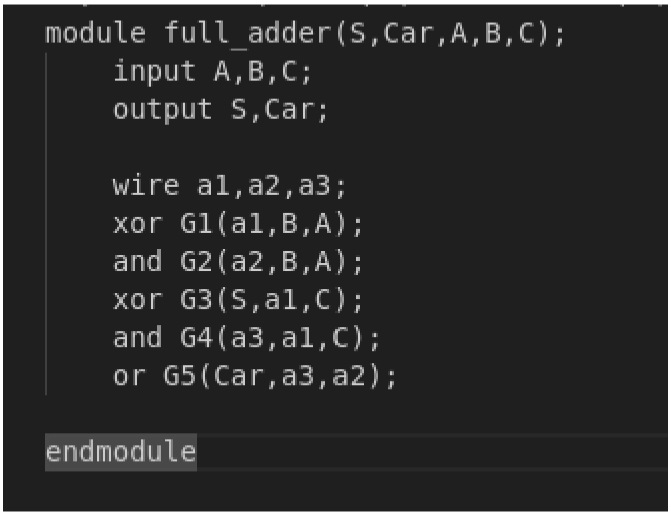
For making a 4-bit adder, we first write a code for fulladder and using the fulladder we made our 4-bit adder ciruit.

Diagram:



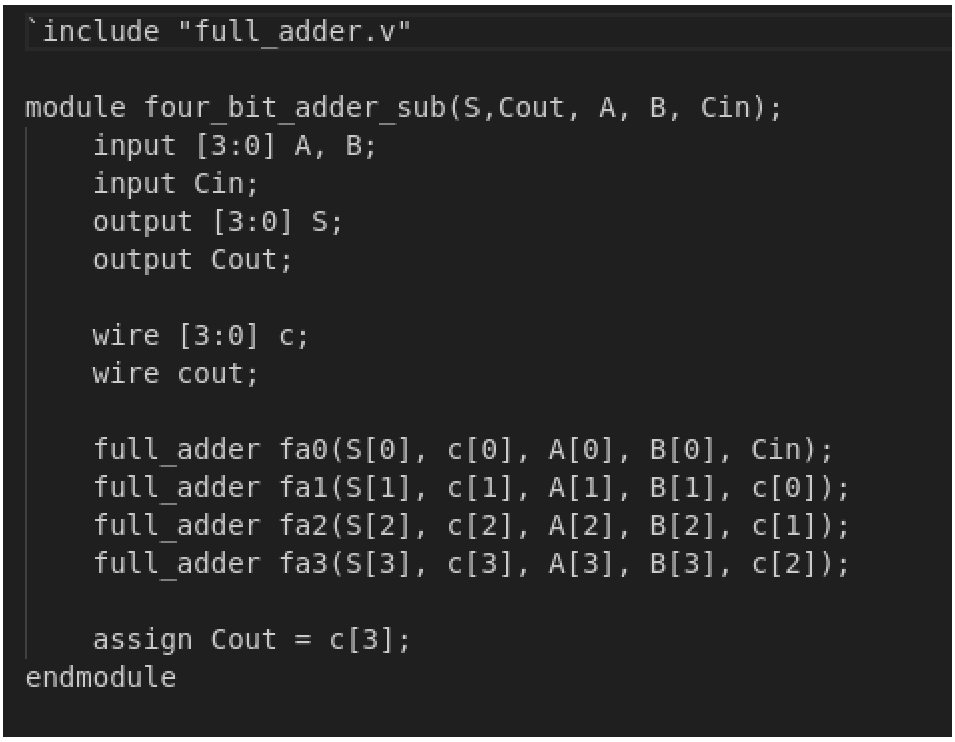
VERILOG Code:

Fulladder:



```
module full_adder(S,Car,A,B,C);
    input A,B,C;
    output S,Car;

    wire a1,a2,a3;
    xor G1(a1,B,A);
    and G2(a2,B,A);
    xor G3(S,a1,C);
    and G4(a3,a1,C);
    or G5(Car,a3,a2);

endmodule
```

4-BIT ADDER:

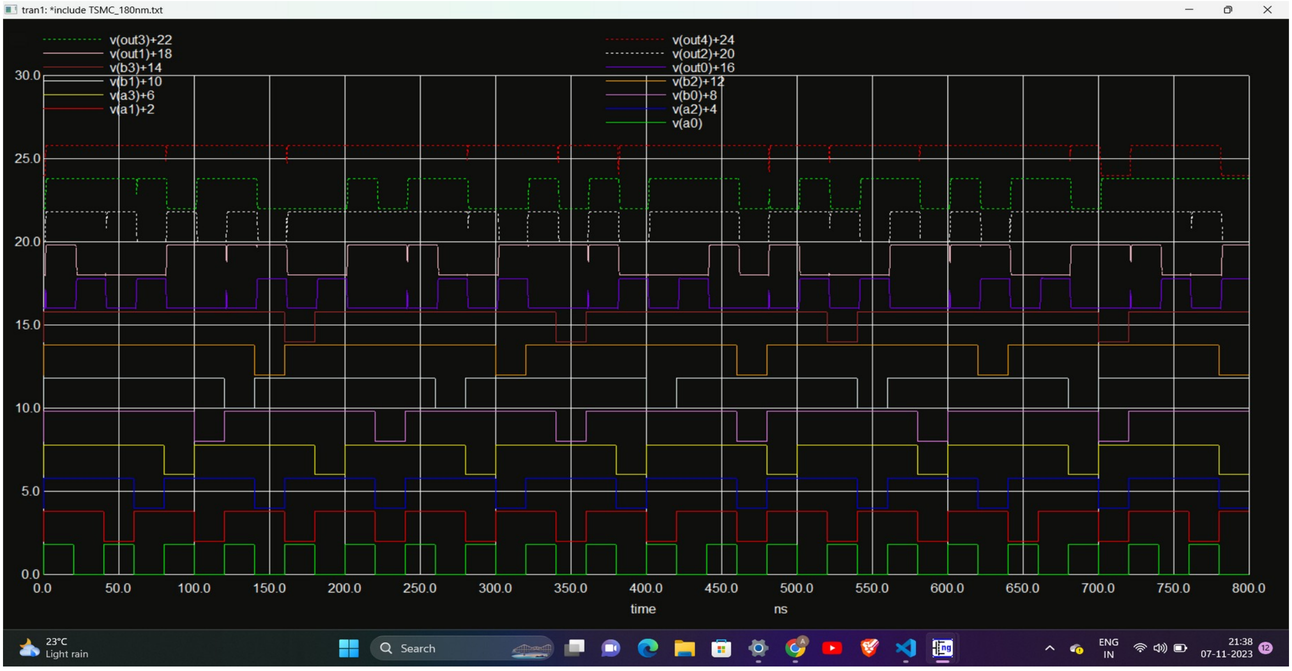


```
`include "full_adder.v"

module four_bit_adder_sub(S,Cout, A, B, Cin);
    input [3:0] A, B;
    input Cin;
    output [3:0] S;
    output Cout;

    wire [3:0] c;
    wire cout;

    full_adder fa0(S[0], c[0], A[0], B[0], Cin);
    full_adder fa1(S[1], c[1], A[1], B[1], c[0]);
    full_adder fa2(S[2], c[2], A[2], B[2], c[1]);
    full_adder fa3(S[3], c[3], A[3], B[3], c[2]);

    assign Cout = c[3];
endmodule
```

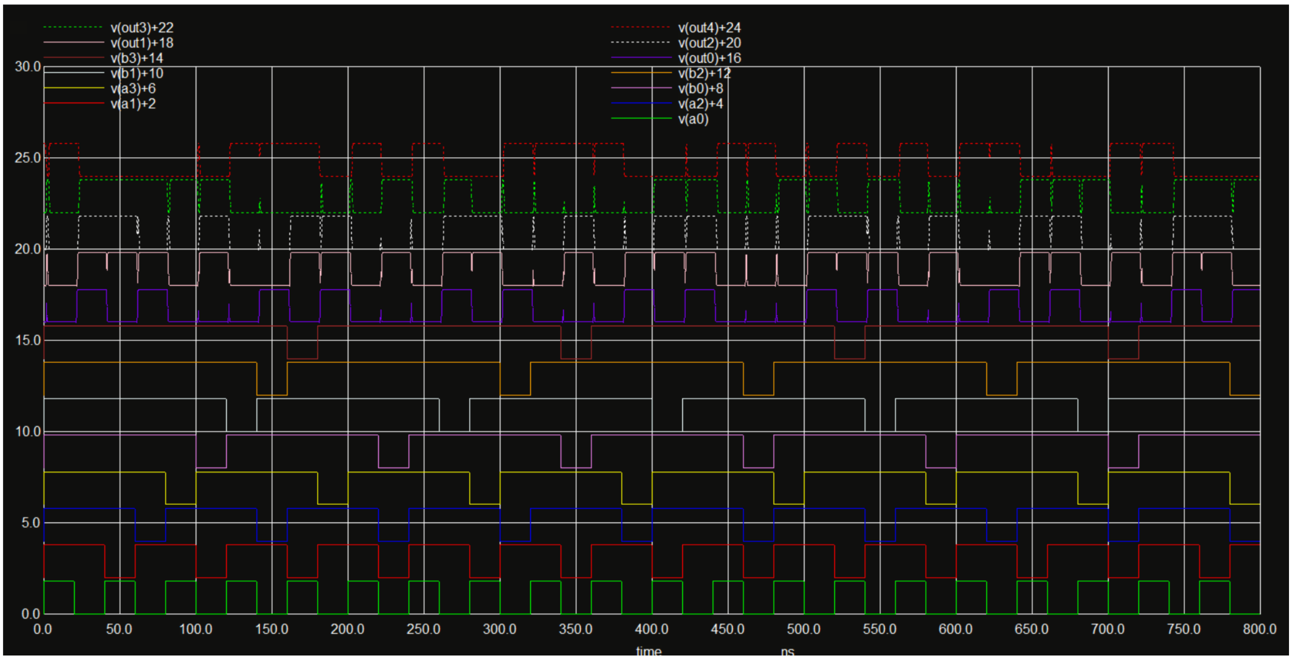
In this we include the fulladder code and wrote the adder code.

NGSPICE PLOT:

ADDER:

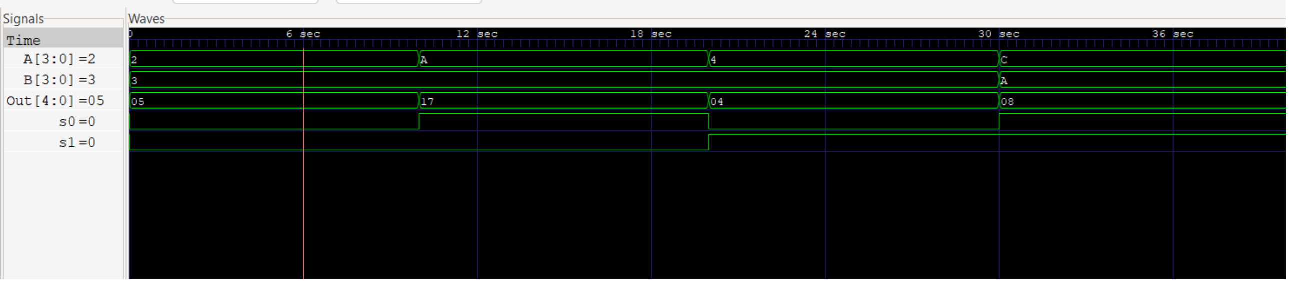


SUBTRACTOR:

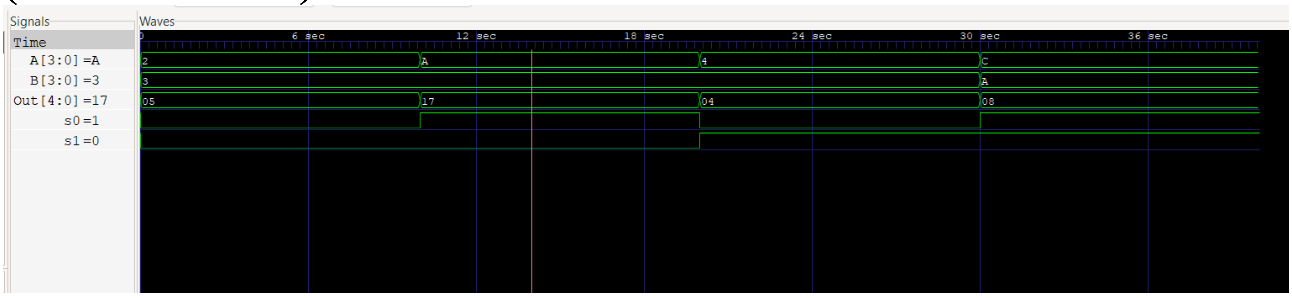


GTKwaves Plot:

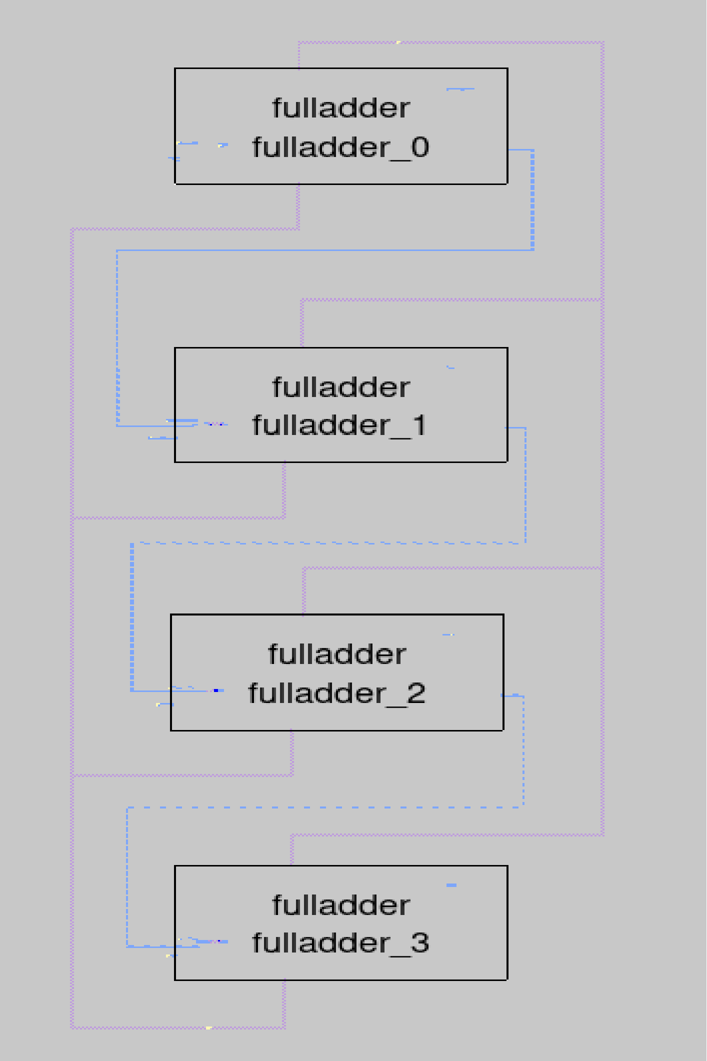
(ADDER)



(SUBTRACTOR)



MAGIC LAYOUT:

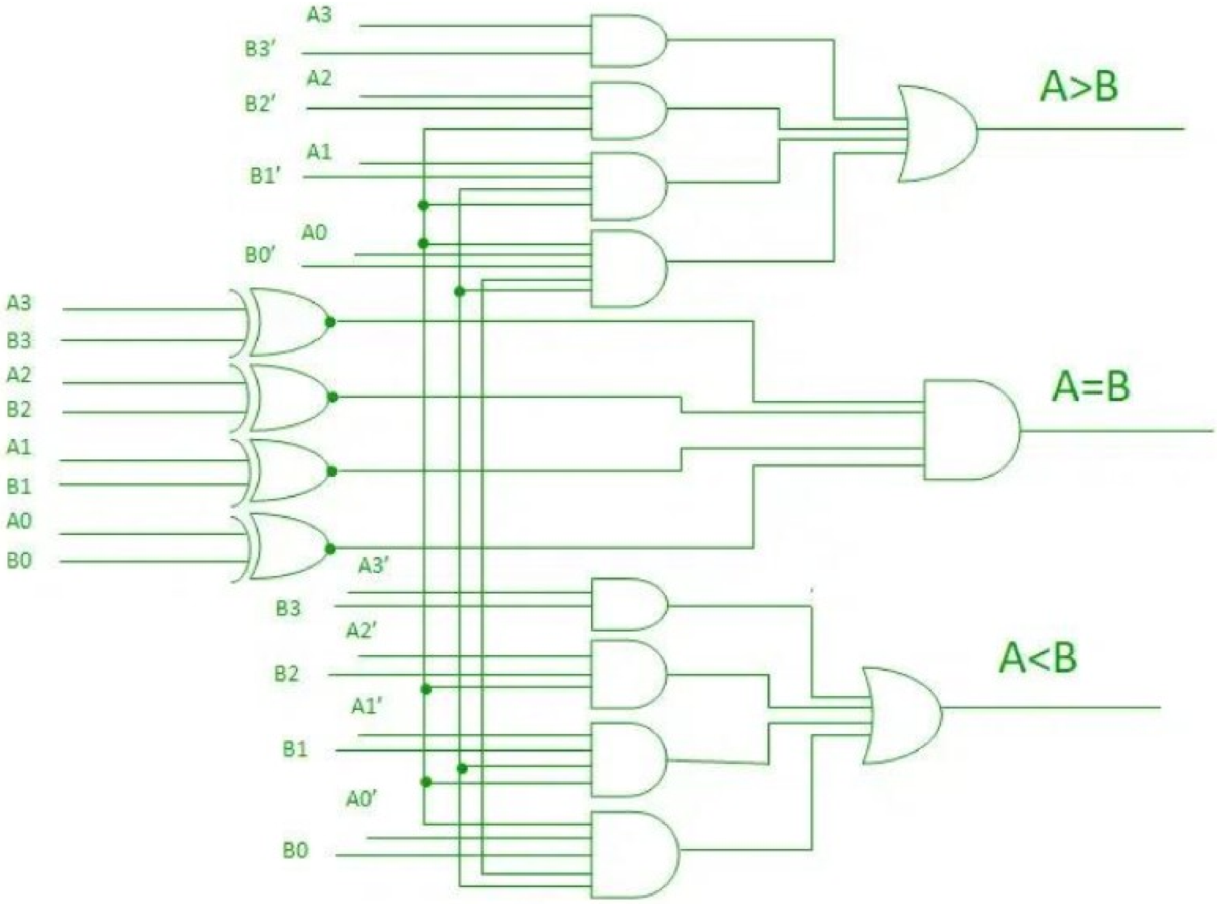


In this we use getcell to use fulladder and in the main alu we use the XOR gates to change the functionality to adder and subtractor.

3) when S0=1 &S0 =0:

COMPARATOR:

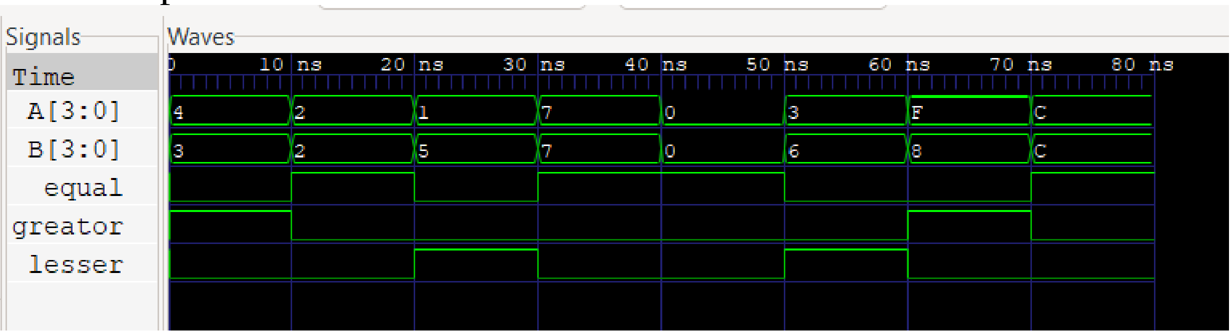
This block would compare our 4-Bit number and give result whether A3A2A1A1 is greater than or less than or equal to B3B2B1B0.



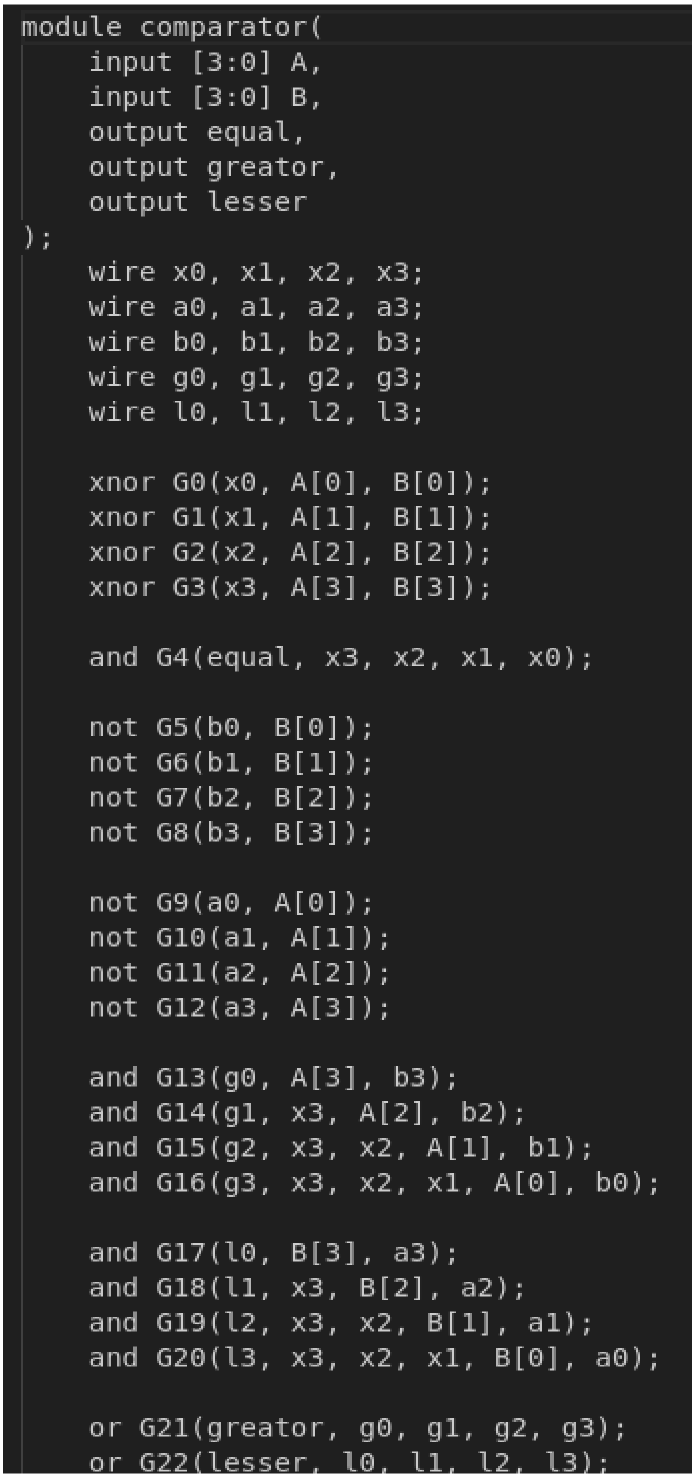
Here instead of using these circuit for simplicity, we use the formula,

for(A>B), G=A3.B3'+X3A2B2'+X3X2A1B1'+X3X2X1A0B0'
for(A<B), L=A3'B3+X3A2'B2+X3X2A1'B1+X3X2X1A0'B0
for(A=B), E=X3X2X1X0
where x3,x2,x1,x0 are XNOR if Ai and Bi.

GTKwave plot:

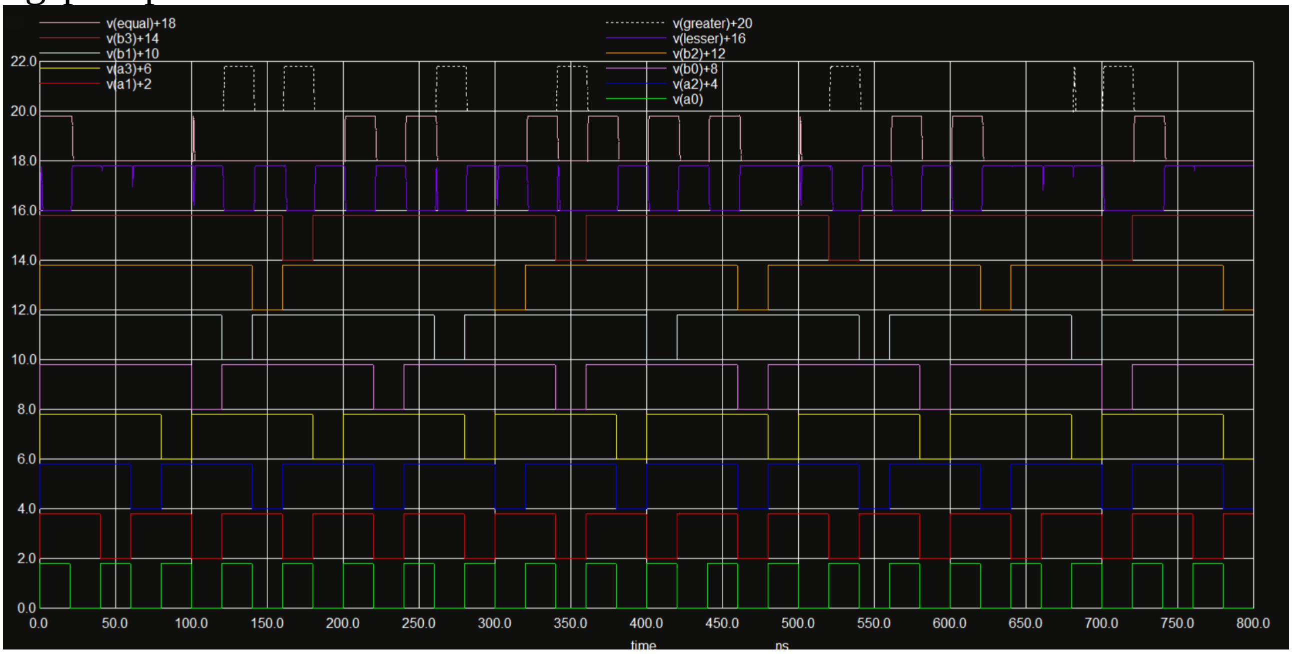


Verilog Code:

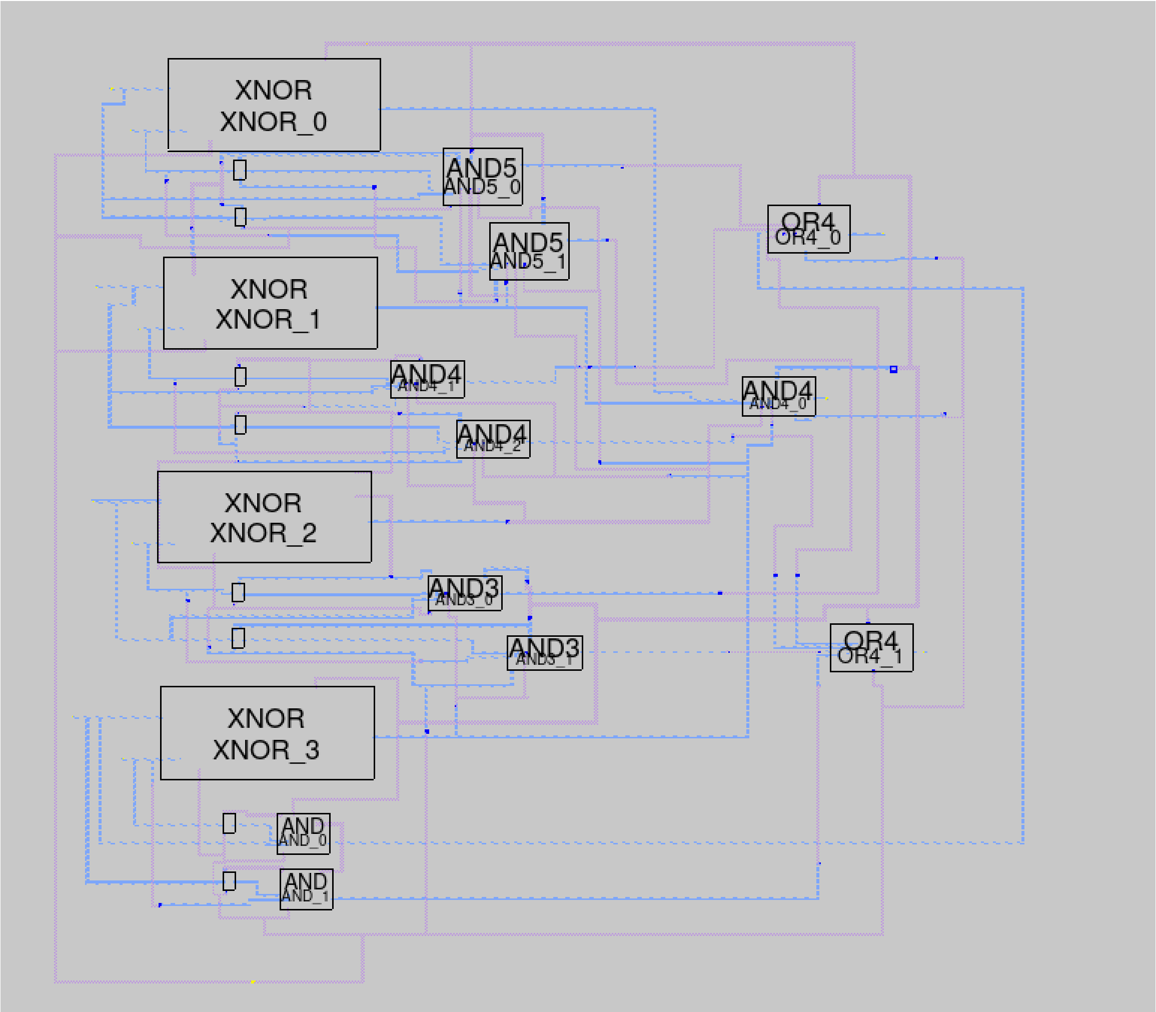


```
module comparator(
    input [3:0] A,
    input [3:0] B,
    output equal,
    output greator,
    output lesser
);
    wire x0, x1, x2, x3;
    wire a0, a1, a2, a3;
    wire b0, b1, b2, b3;
    wire g0, g1, g2, g3;
    wire l0, l1, l2, l3;

    xnor G0(x0, A[0], B[0]);
    xnor G1(x1, A[1], B[1]);
    xnor G2(x2, A[2], B[2]);
    xnor G3(x3, A[3], B[3]);

    and G4(equal, x3, x2, x1, x0);

    not G5(b0, B[0]);
    not G6(b1, B[1]);
    not G7(b2, B[2]);
    not G8(b3, B[3]);

    not G9(a0, A[0]);
    not G10(a1, A[1]);
    not G11(a2, A[2]);
    not G12(a3, A[3]);

    and G13(g0, A[3], b3);
    and G14(g1, x3, A[2], b2);
    and G15(g2, x3, x2, A[1], b1);
    and G16(g3, x3, x2, x1, A[0], b0);

    and G17(l0, B[3], a3);
    and G18(l1, x3, B[2], a2);
    and G19(l2, x3, x2, B[1], a1);
    and G20(l3, x3, x2, x1, B[0], a0);

    or G21(greator, g0, g1, g2, g3);
    or G22(lesser, l0, l1, l2, l3);
```

ngspice plot:



MAGIC Layout:



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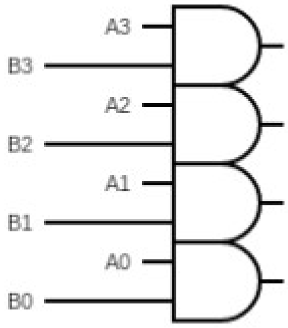
4)4-BIT Adder:

This block Performs AND operation on A3&B3; A0&B0; A1&B1; A0&B0.



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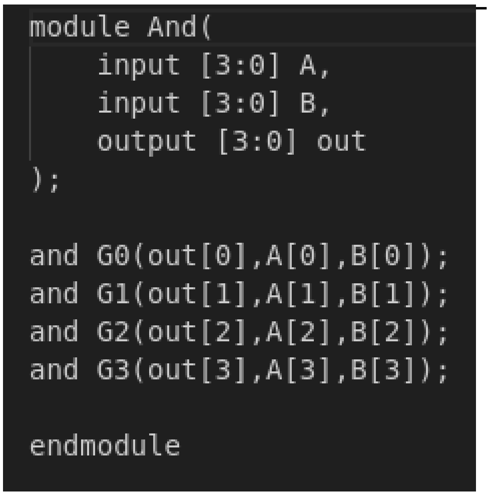
verilog code:

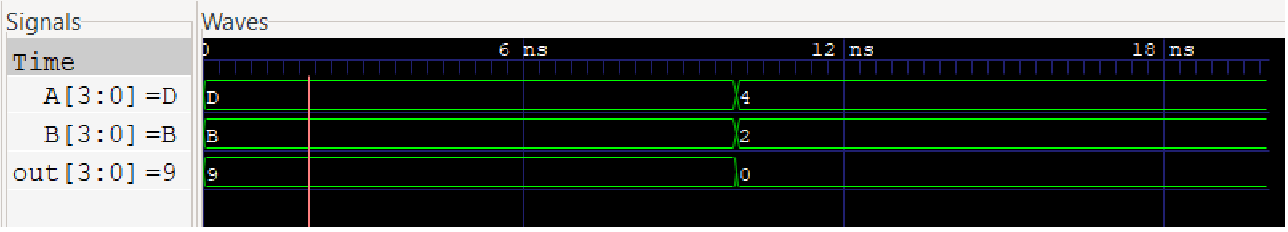


```
module And(
    input [3:0] A,
    input [3:0] B,
    output [3:0] out
);

and G0(out[0],A[0],B[0]);
and G1(out[1],A[1],B[1]);
and G2(out[2],A[2],B[2]);
and G3(out[3],A[3],B[3]);

endmodule
```

GTKwave plot:



```
Time
  A[3:0] =D
  B[3:0] =B
out[3:0] =9
```

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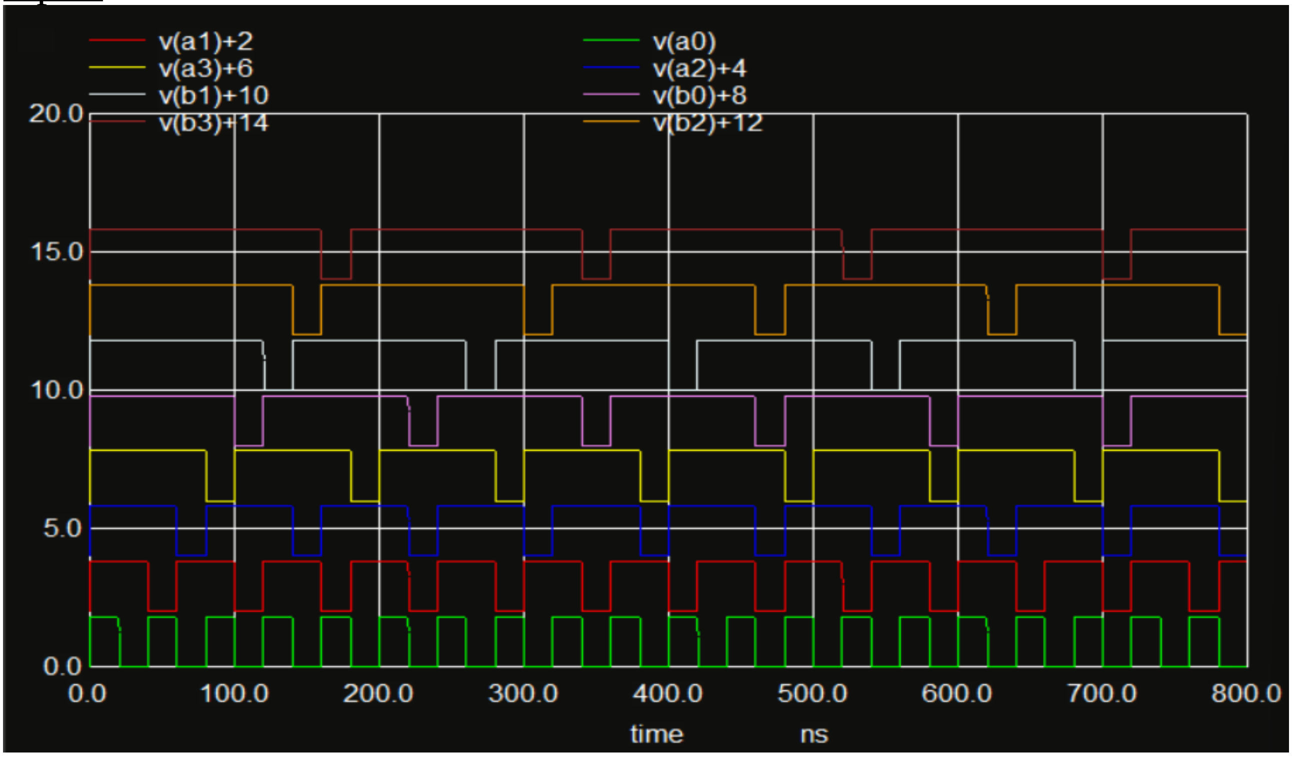
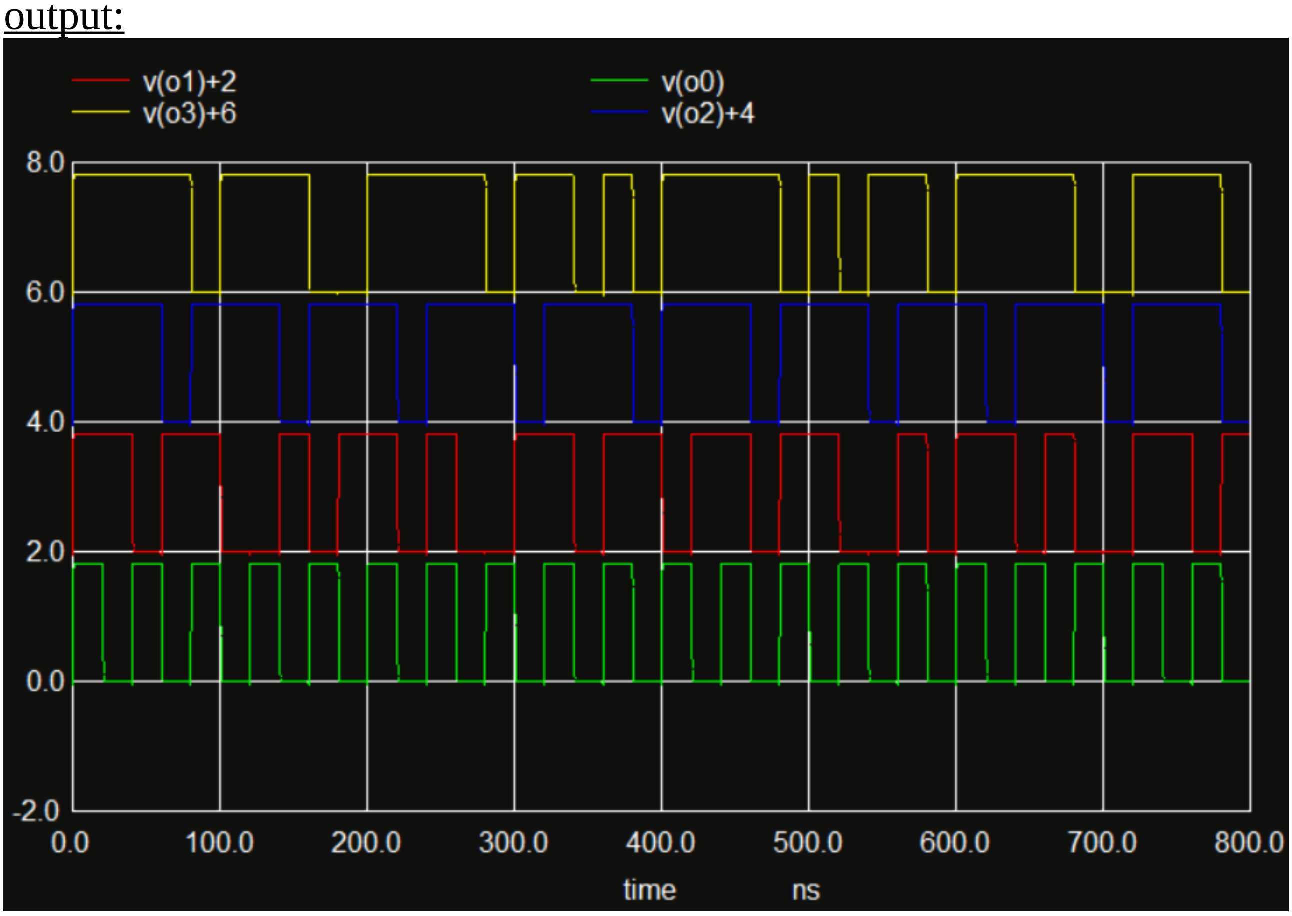
NGSPICE Plot:

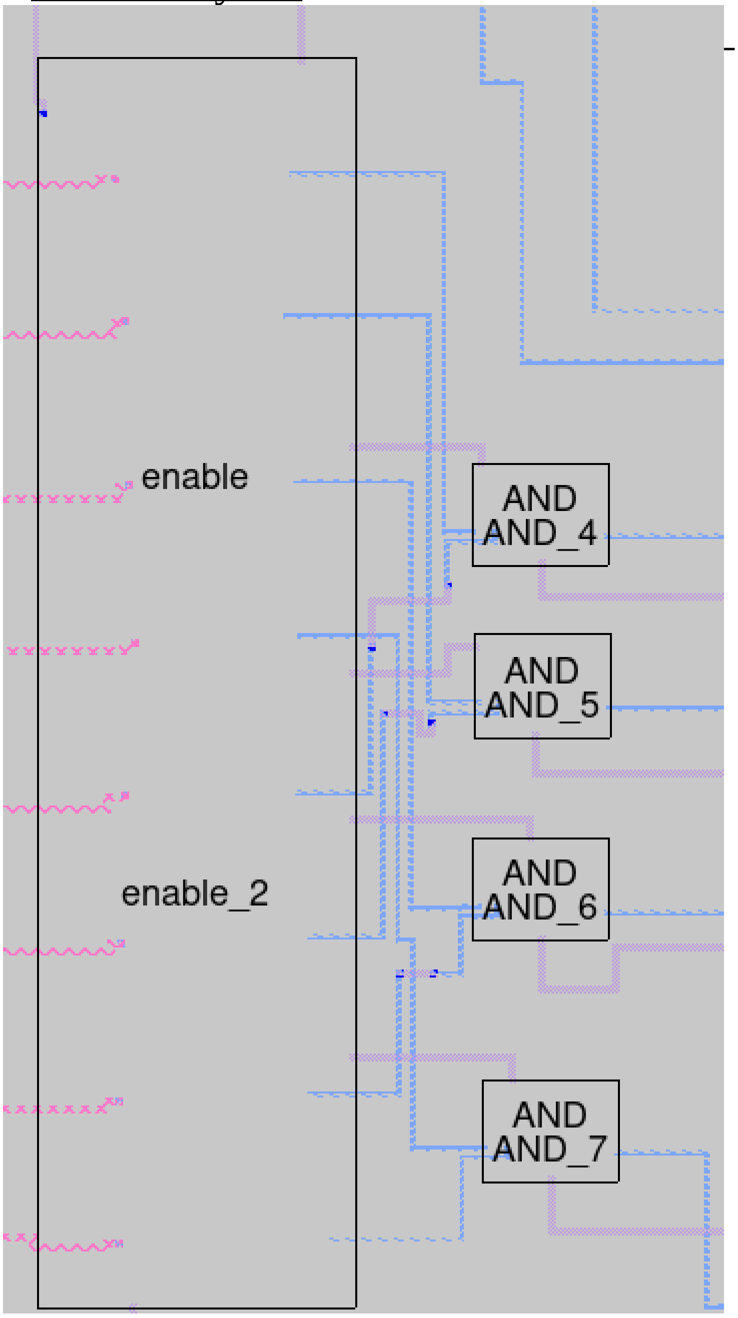
input:



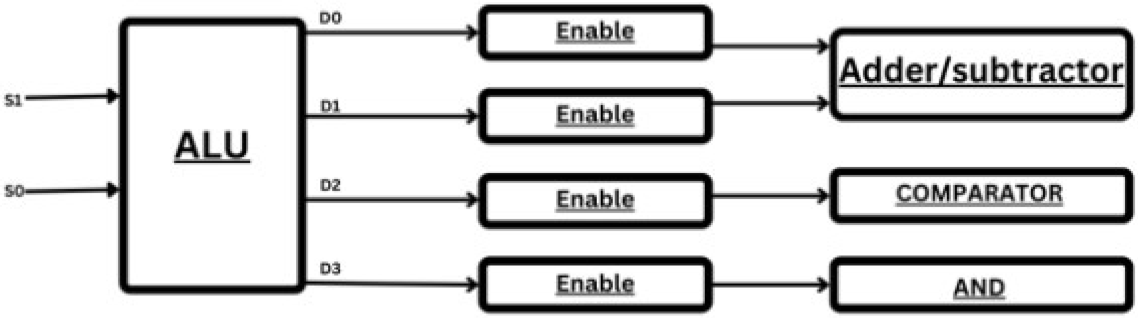
output:



MAGIC layout:



Combined circuit of 4-bit ALU:



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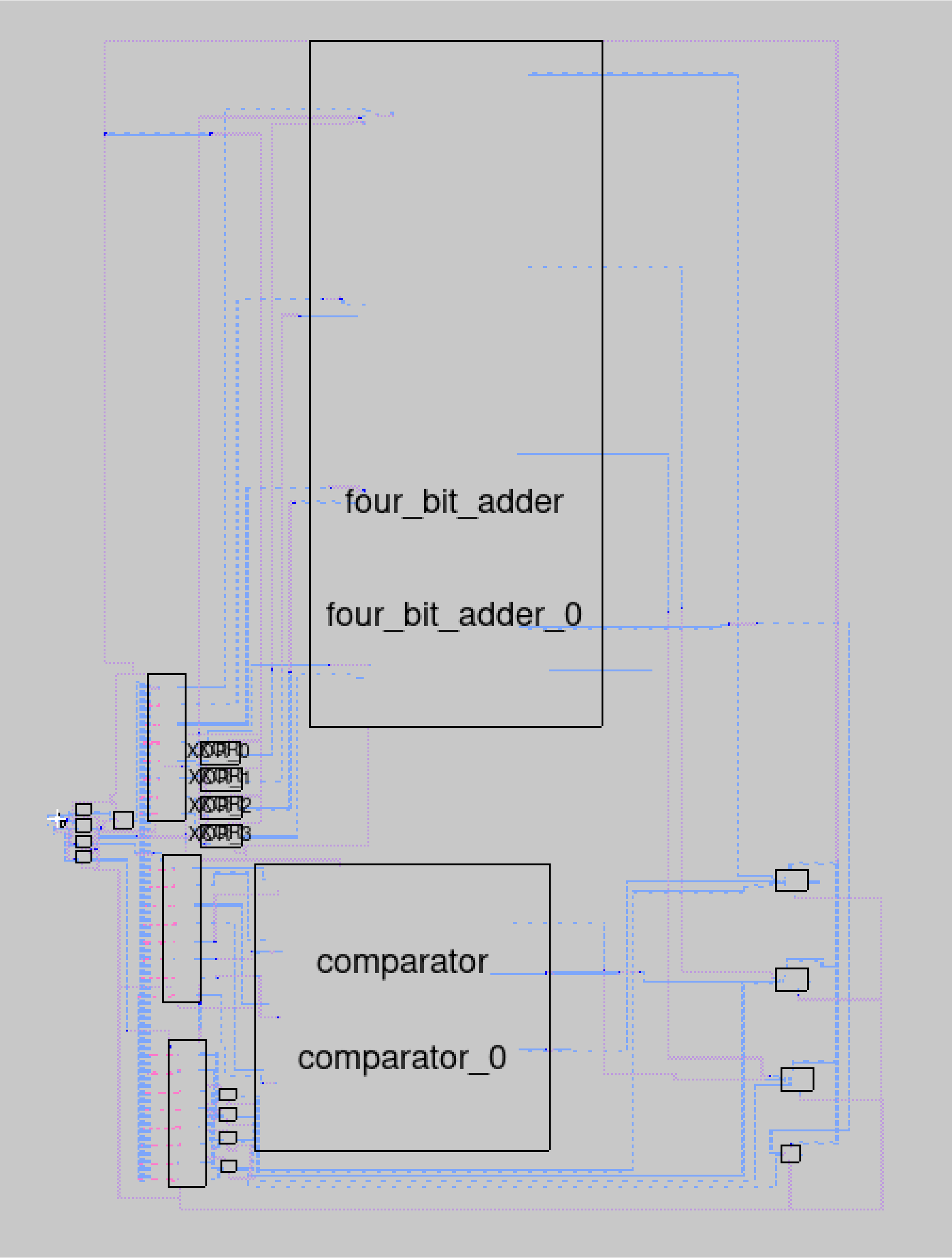
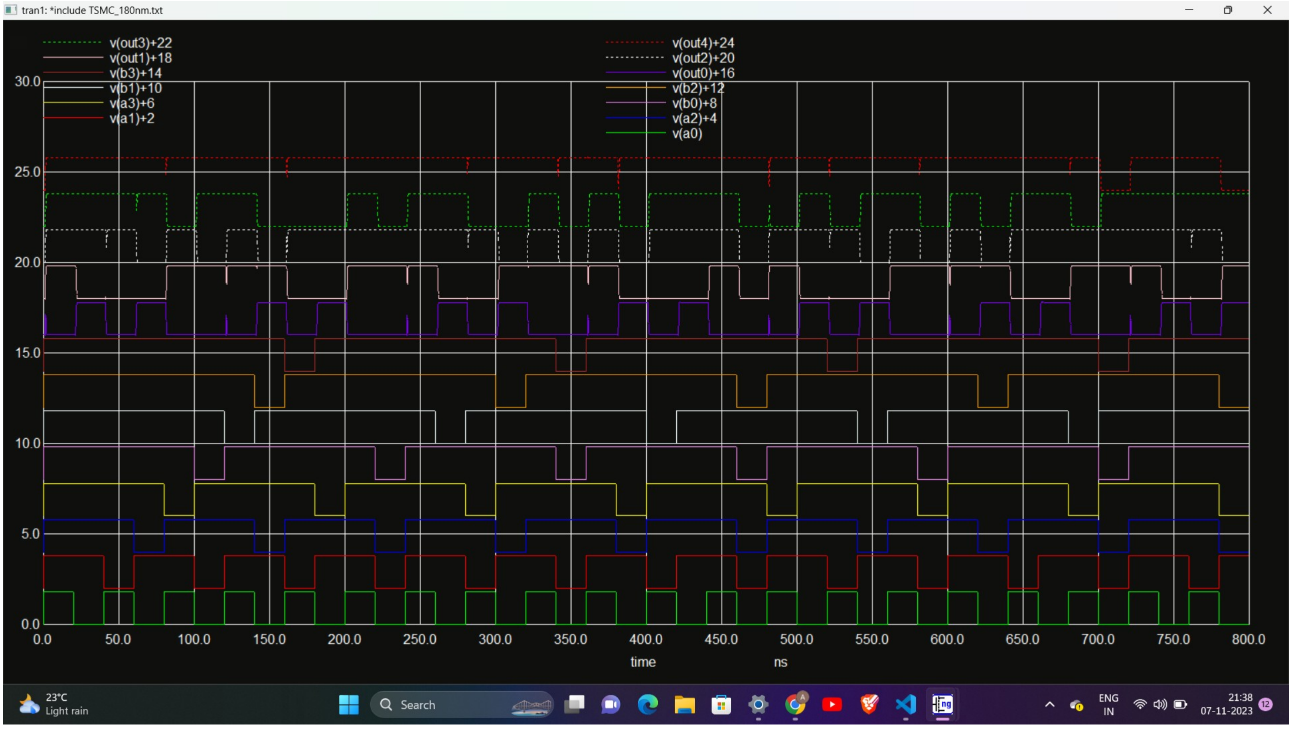
MAGIC layout for ALU:



NGSPICE plots:

1)ADDER:



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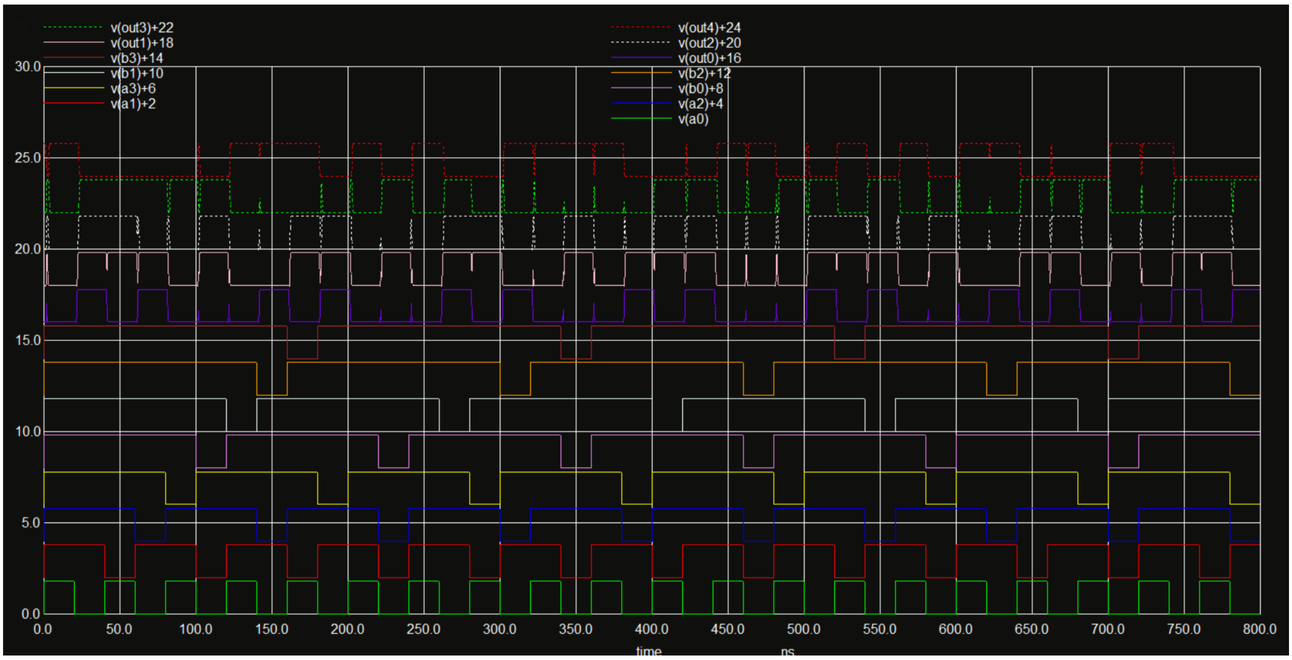
2)SUBTRACTOR:



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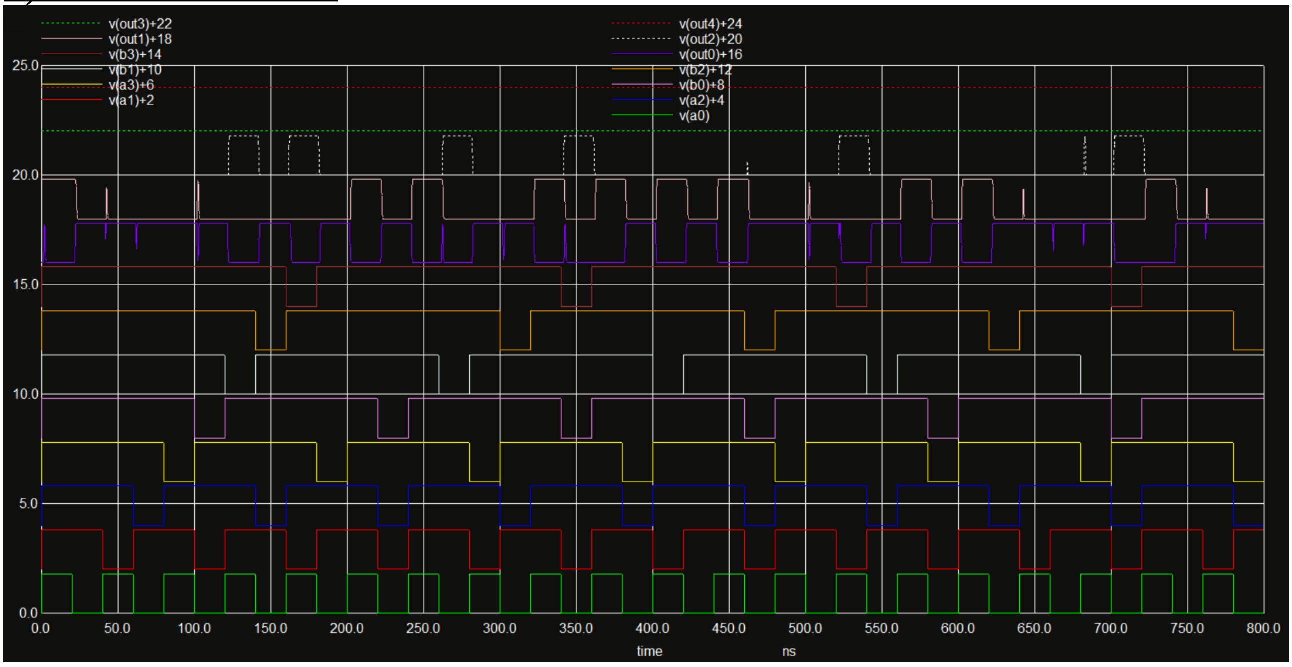
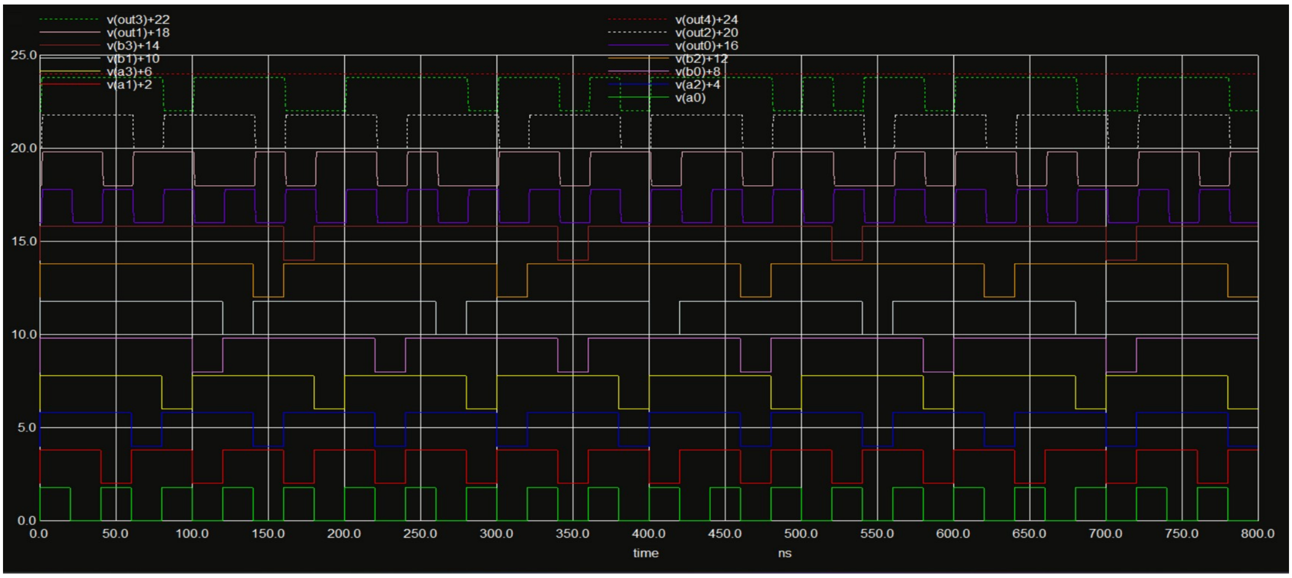
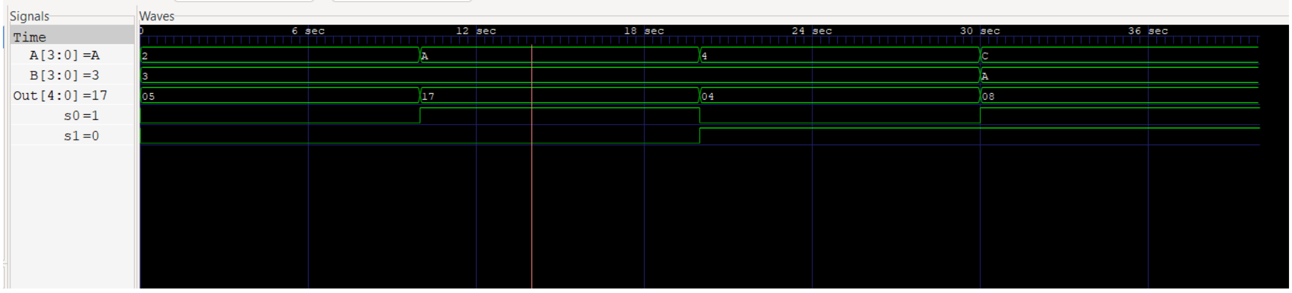
3)COMPARATOR:



4) AND



Verification by GTKwave Plot:



```
Signals
Time
   A[3:0] =A
   B[3:0] =3
Out[4:0] =17
      s0 =1
      s1 =0
```

Problems and challenges faced:

1) While doing verilog, i found it a bit hard at starting since we had to define intermediate values which after getting familiar it turns out to be quite simple.
2) While writing Ngspice code, i got few errors at starting since, i didn’t know that it was case-insensitive like naming different variables as A0 & a0 but both of them were sames.
3) In magic, we are not able to edit or change the position or delete any cell that we import using getcell, also i faced problems due to using m3 metal which gave errors.
4)Magic Layout Errors:

- Solution: Check the magic layout for DRC (Design Rule Check) errors. Address any spacing, width, or other layout violations. Magic usually provides detailed error messages to guide you.

5) Even with the help od DRC we only know about the error but the place is still unkown which was very tideous to find.

P.T.O.

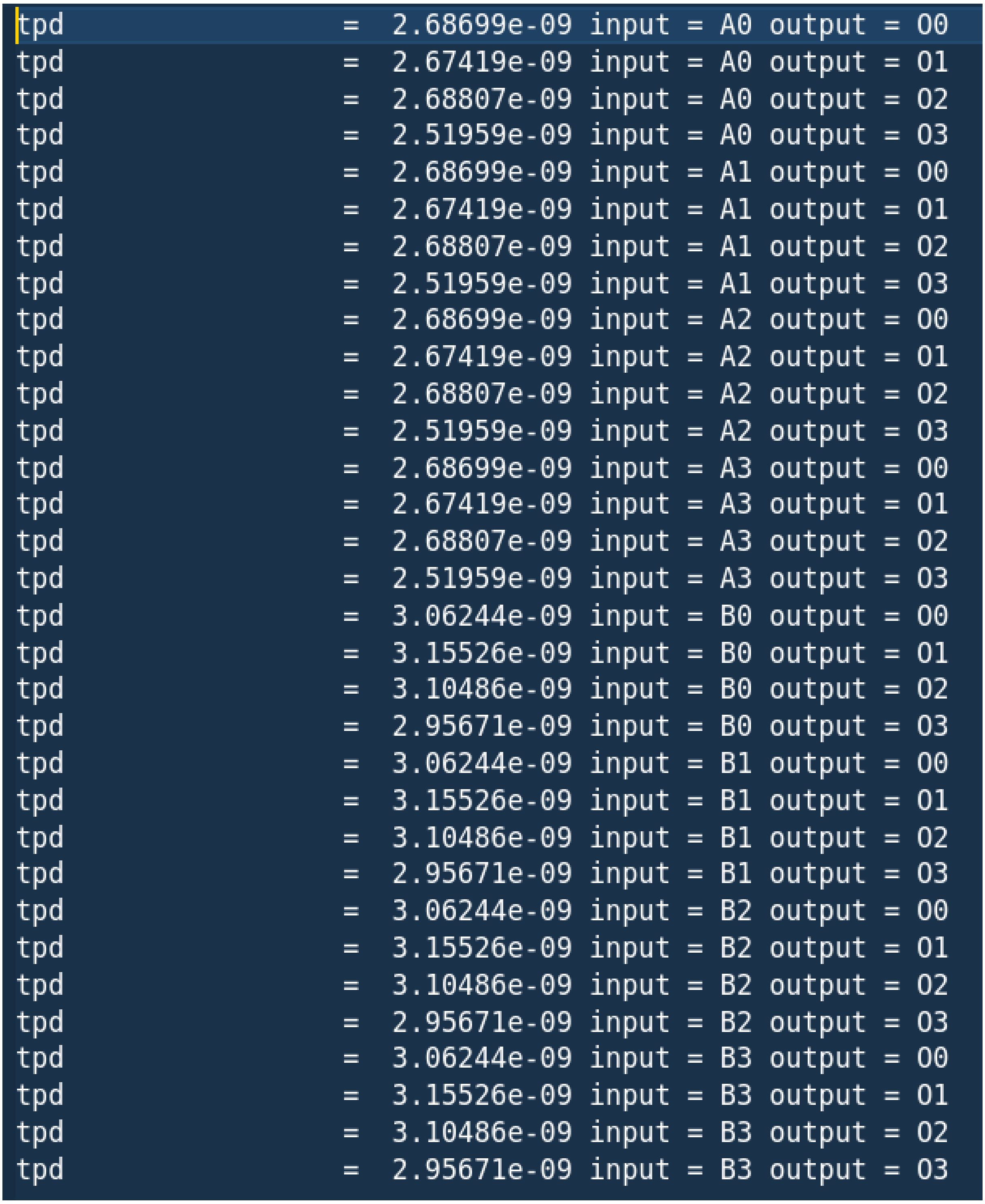
P.T.O.

DELAY_ANALYSIS:

In order to calculate Delay, i wrote 4 delay scripts to find the delay of all operations in the 4 modules.

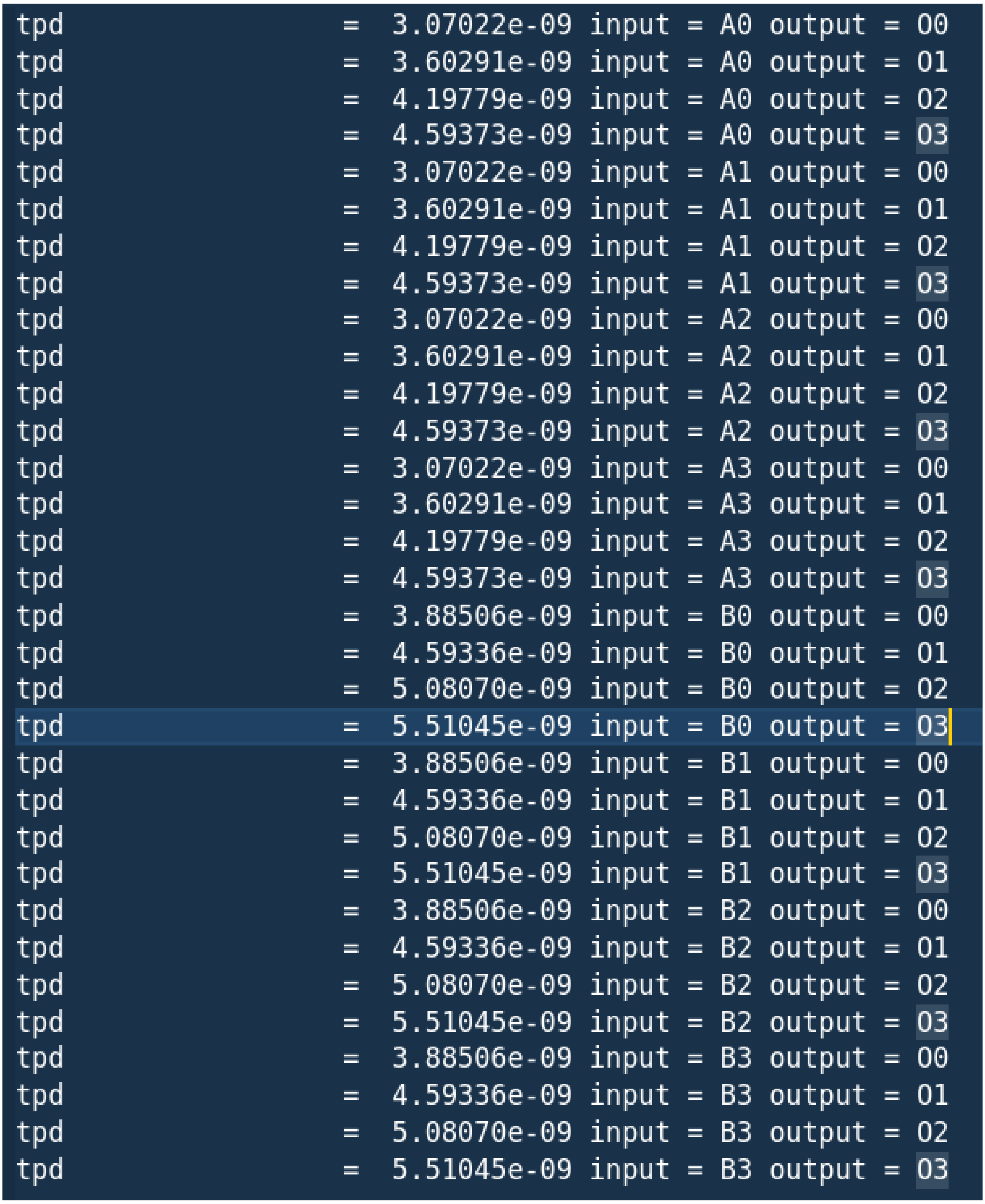
Delay results:

In case of ADDER:



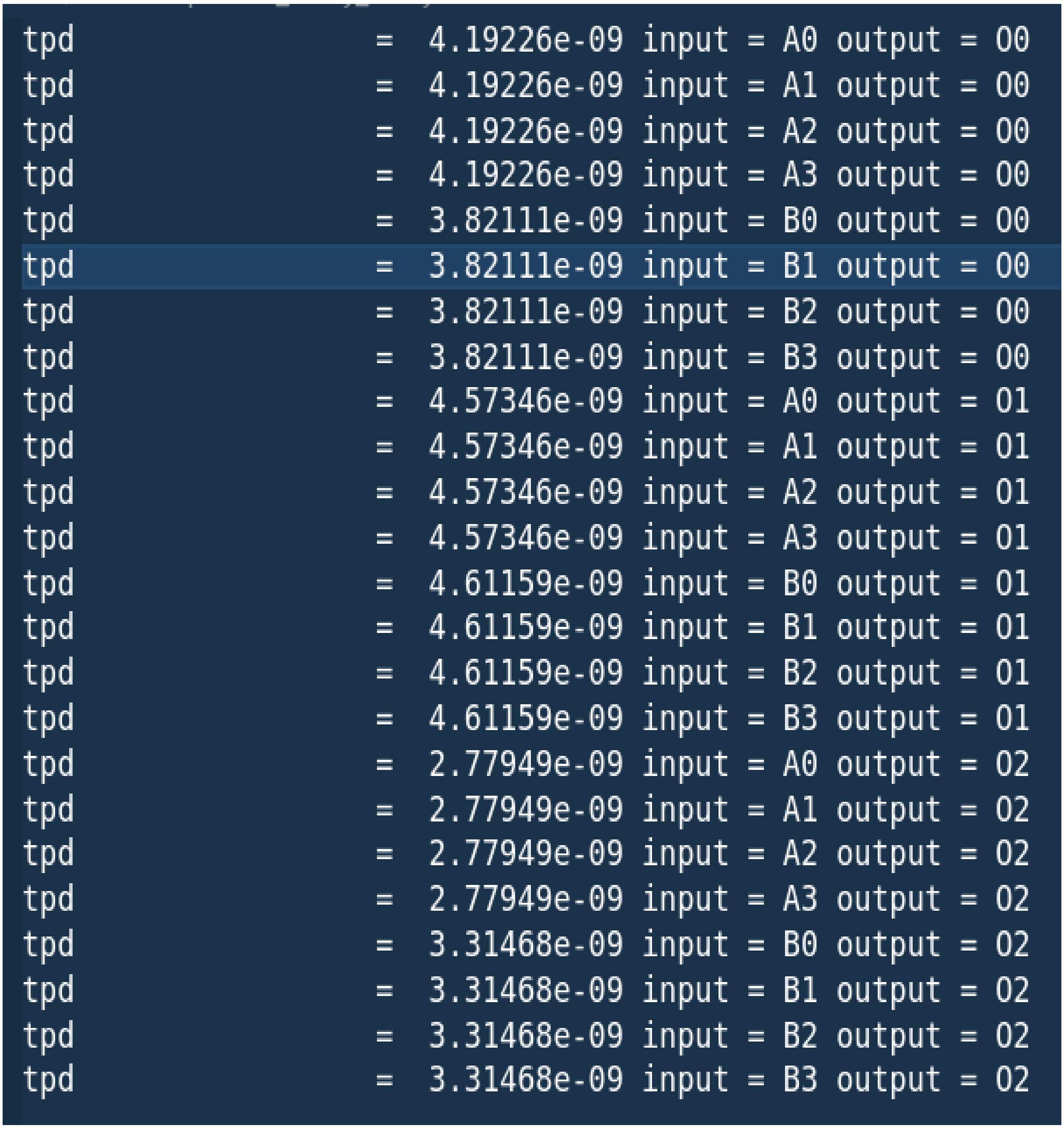
```
tpd                    =  2.68699e-09 input = A0 output = O0
tpd                    =  2.67419e-09 input = A0 output = O1
tpd                    =  2.68807e-09 input = A0 output = O2
tpd                    =  2.51959e-09 input = A0 output = O3
tpd                    =  2.68699e-09 input = A1 output = O0
tpd                    =  2.67419e-09 input = A1 output = O1
tpd                    =  2.68807e-09 input = A1 output = O2
tpd                    =  2.51959e-09 input = A1 output = O3
tpd                    =  2.68699e-09 input = A2 output = O0
tpd                    =  2.67419e-09 input = A2 output = O1
tpd                    =  2.68807e-09 input = A2 output = O2
tpd                    =  2.51959e-09 input = A2 output = O3
tpd                    =  2.68699e-09 input = A3 output = O0
tpd                    =  2.67419e-09 input = A3 output = O1
tpd                    =  2.68807e-09 input = A3 output = O2
tpd                    =  2.51959e-09 input = A3 output = O3
tpd                    =  3.06244e-09 input = B0 output = O0
tpd                    =  3.15526e-09 input = B0 output = O1
tpd                    =  3.10486e-09 input = B0 output = O2
tpd                    =  2.95671e-09 input = B0 output = O3
tpd                    =  3.06244e-09 input = B1 output = O0
tpd                    =  3.15526e-09 input = B1 output = O1
tpd                    =  3.10486e-09 input = B1 output = O2
tpd                    =  2.95671e-09 input = B1 output = O3
tpd                    =  3.06244e-09 input = B2 output = O0
tpd                    =  3.15526e-09 input = B2 output = O1
tpd                    =  3.10486e-09 input = B2 output = O2
tpd                    =  2.95671e-09 input = B2 output = O3
tpd                    =  3.06244e-09 input = B3 output = O0
tpd                    =  3.15526e-09 input = B3 output = O1
tpd                    =  3.10486e-09 input = B3 output = O2
tpd                    =  2.95671e-09 input = B3 output = O3
```

In case of subtractor:



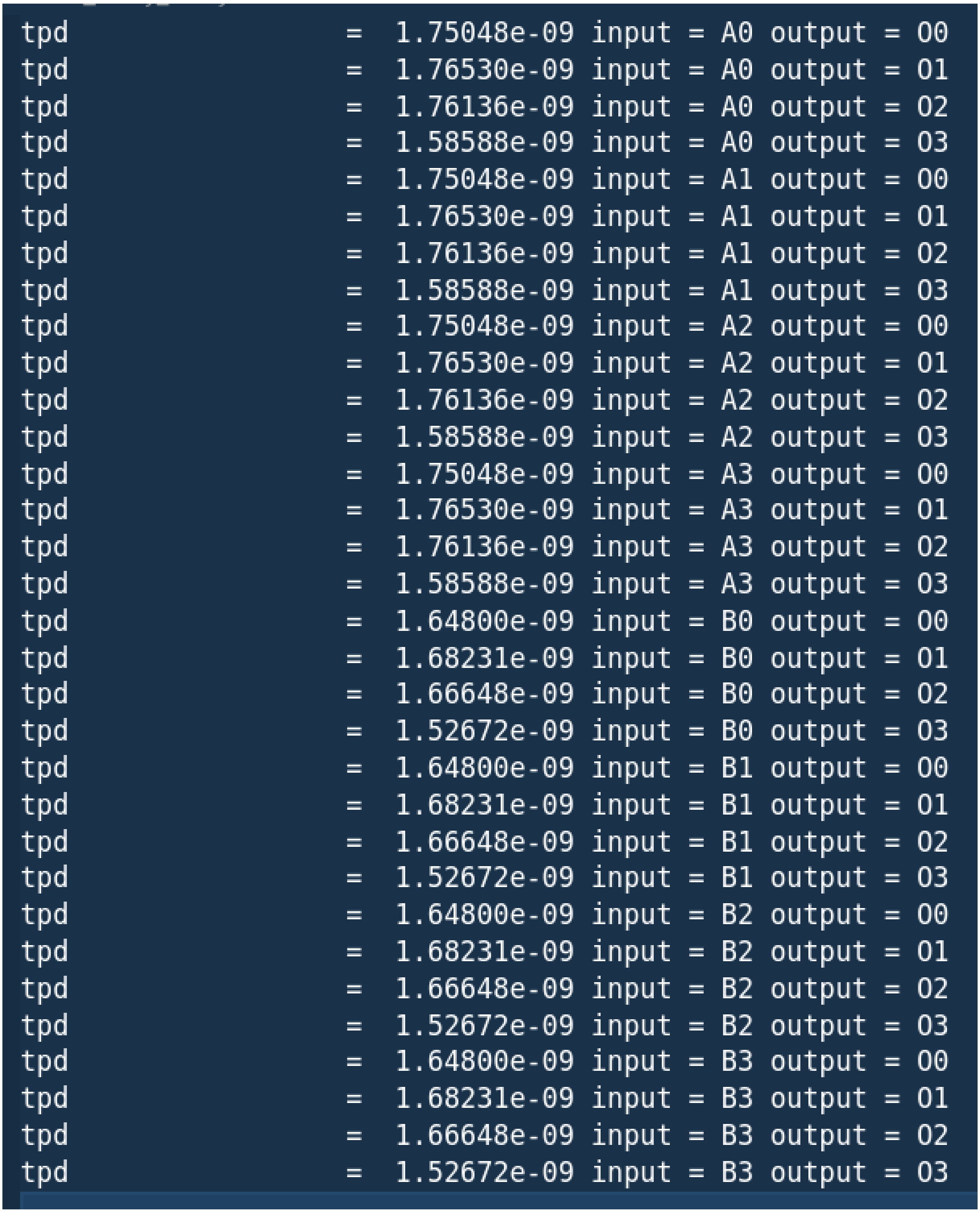
```
tpd                    =  3.07022e-09 input = A0 output = O0
tpd                    =  3.60291e-09 input = A0 output = O1
tpd                    =  4.19779e-09 input = A0 output = O2
tpd                    =  4.59373e-09 input = A0 output = O3
tpd                    =  3.07022e-09 input = A1 output = O0
tpd                    =  3.60291e-09 input = A1 output = O1
tpd                    =  4.19779e-09 input = A1 output = O2
tpd                    =  4.59373e-09 input = A1 output = O3
tpd                    =  3.07022e-09 input = A2 output = O0
tpd                    =  3.60291e-09 input = A2 output = O1
tpd                    =  4.19779e-09 input = A2 output = O2
tpd                    =  4.59373e-09 input = A2 output = O3
tpd                    =  3.07022e-09 input = A3 output = O0
tpd                    =  3.60291e-09 input = A3 output = O1
tpd                    =  4.19779e-09 input = A3 output = O2
tpd                    =  4.59373e-09 input = A3 output = O3
tpd                    =  3.88506e-09 input = B0 output = O0
tpd                    =  4.59336e-09 input = B0 output = O1
tpd                    =  5.08070e-09 input = B0 output = O2
tpd                    =  5.51045e-09 input = B0 output = O3
tpd                    =  3.88506e-09 input = B1 output = O0
tpd                    =  4.59336e-09 input = B1 output = O1
tpd                    =  5.08070e-09 input = B1 output = O2
tpd                    =  5.51045e-09 input = B1 output = O3
tpd                    =  3.88506e-09 input = B2 output = O0
tpd                    =  4.59336e-09 input = B2 output = O1
tpd                    =  5.08070e-09 input = B2 output = O2
tpd                    =  5.51045e-09 input = B2 output = O3
tpd                    =  3.88506e-09 input = B3 output = O0
tpd                    =  4.59336e-09 input = B3 output = O1
tpd                    =  5.08070e-09 input = B3 output = O2
tpd                    =  5.51045e-09 input = B3 output = O3
```

In case of Comparator:



```
tpd                        =  4.19226e-09 input = A0 output = O0
tpd                        =  4.19226e-09 input = A1 output = O0
tpd                        =  4.19226e-09 input = A2 output = O0
tpd                        =  4.19226e-09 input = A3 output = O0
tpd                        =  3.82111e-09 input = B0 output = O0
tpd                        =  3.82111e-09 input = B1 output = O0
tpd                        =  3.82111e-09 input = B2 output = O0
tpd                        =  3.82111e-09 input = B3 output = O0
tpd                        =  4.57346e-09 input = A0 output = O1
tpd                        =  4.57346e-09 input = A1 output = O1
tpd                        =  4.57346e-09 input = A2 output = O1
tpd                        =  4.57346e-09 input = A3 output = O1
tpd                        =  4.61159e-09 input = B0 output = O1
tpd                        =  4.61159e-09 input = B1 output = O1
tpd                        =  4.61159e-09 input = B2 output = O1
tpd                        =  4.61159e-09 input = B3 output = O1
tpd                        =  2.77949e-09 input = A0 output = O2
tpd                        =  2.77949e-09 input = A1 output = O2
tpd                        =  2.77949e-09 input = A2 output = O2
tpd                        =  2.77949e-09 input = A3 output = O2
tpd                        =  3.31468e-09 input = B0 output = O2
tpd                        =  3.31468e-09 input = B1 output = O2
tpd                        =  3.31468e-09 input = B2 output = O2
tpd                        =  3.31468e-09 input = B3 output = O2
```

p.t.o.
in case of AND:



```
tpd                  =  1.75048e-09 input = A0 output = O0
tpd                  =  1.76530e-09 input = A0 output = O1
tpd                  =  1.76136e-09 input = A0 output = O2
tpd                  =  1.58588e-09 input = A0 output = O3
tpd                  =  1.75048e-09 input = A1 output = O0
tpd                  =  1.76530e-09 input = A1 output = O1
tpd                  =  1.76136e-09 input = A1 output = O2
tpd                  =  1.58588e-09 input = A1 output = O3
tpd                  =  1.75048e-09 input = A2 output = O0
tpd                  =  1.76530e-09 input = A2 output = O1
tpd                  =  1.76136e-09 input = A2 output = O2
tpd                  =  1.58588e-09 input = A2 output = O3
tpd                  =  1.75048e-09 input = A3 output = O0
tpd                  =  1.76530e-09 input = A3 output = O1
tpd                  =  1.76136e-09 input = A3 output = O2
tpd                  =  1.58588e-09 input = A3 output = O3
tpd                  =  1.64800e-09 input = B0 output = O0
tpd                  =  1.68231e-09 input = B0 output = O1
tpd                  =  1.66648e-09 input = B0 output = O2
tpd                  =  1.52672e-09 input = B0 output = O3
tpd                  =  1.64800e-09 input = B1 output = O0
tpd                  =  1.68231e-09 input = B1 output = O1
tpd                  =  1.66648e-09 input = B1 output = O2
tpd                  =  1.52672e-09 input = B1 output = O3
tpd                  =  1.64800e-09 input = B2 output = O0
tpd                  =  1.68231e-09 input = B2 output = O1
tpd                  =  1.66648e-09 input = B2 output = O2
tpd                  =  1.52672e-09 input = B2 output = O3
tpd                  =  1.64800e-09 input = B3 output = O0
tpd                  =  1.68231e-09 input = B3 output = O1
tpd                  =  1.66648e-09 input = B3 output = O2
tpd                  =  1.52672e-09 input = B3 output = O3
```

OBSERVATION & CONCLUSION:

We notice from the above result that maximum delay is present in subtractor.
Therefore, that is the critical path.

Since, Critical Path is the path in which we get maximum delay.
So, Subtractor B0-O3 is the critical path.

THANK YOU