ELL201 LAB PROJECT
SERIAL GENERATOR

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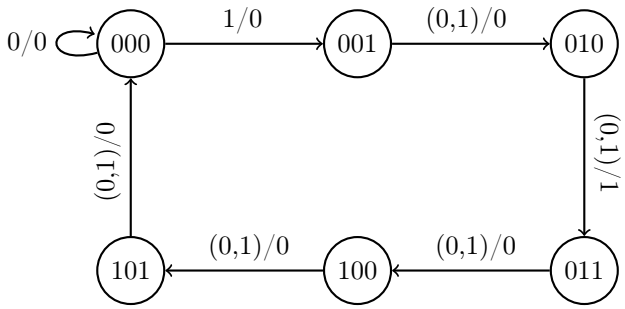
Contents

1 Aim

To design a sequence generator that generates the serial sequence:
$X_3 = 9 \Rightarrow X_3 \ \% \ 8 = 1$
$X_4 = 8, \Rightarrow X_4 \ \% \ 8 = 0$
$\therefore$ Serial Sequence : {0,0,1,0,0,0}

2 State Diagram



State diagram of Mealy FSM after reduction

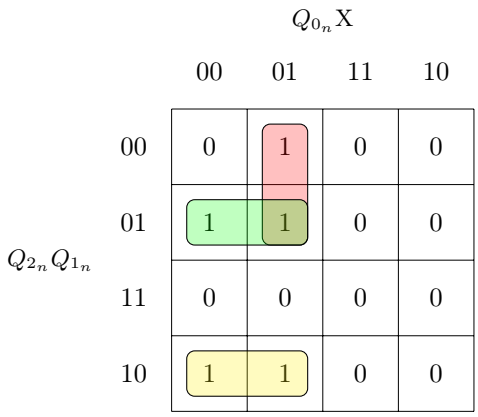
Here, 000 is the idle state. Since there are 6 states after reduction, we will need $\geq \ log_2 6$, i.e., 3 flip-flops for the generator.

3 State Table

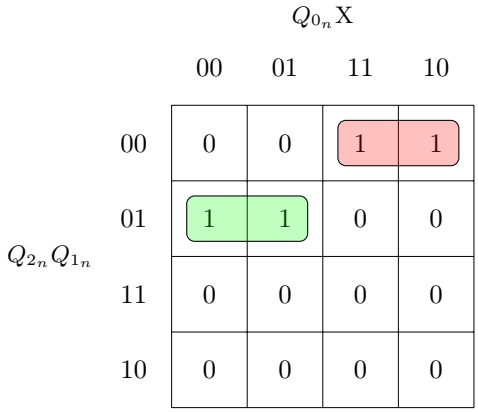
Current State			Input	Output	Next State			D Flip-Flop		
Q_{2_n}	Q_{1_n}	Q_{0_n}	X	Y	$Q_{2_{n+1}}$	$Q_{1_{n+1}}$	$Q_{0_{n+1}}$	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	1	0	0	1	0
0	1	0	0	1	0	1	1	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	1	0	0	1	0	0
0	1	1	1	0	1	0	0	1	0	0
1	0	0	0	0	1	0	1	1	0	1
1	0	0	1	0	1	0	1	1	0	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

4 Karnaugh Maps

K-Map for D_0



K-Map for D_1



K-Map for D_2

$Q_2{}_nQ_1{}_n$ \ $Q_0{}_n$X	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	0
10	1	1	0	0

K-Map for Y

$Q_2{}_nQ_1{}_n$ \ $Q_0{}_n$X	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

Here, Q_0 is the LSB and Q_2 is the MSB. The states are represented by $Q_2Q_1Q_0$.
Here, D_0 is the LSB and D_2 is the MSB.
$D_0 = Q_2Q_1'Q_0' + Q_2'Q_1Q_0' + Q_2'Q_0'$X
$D_1 = Q_2'Q_1'Q_0 + Q_2'Q_1Q_0'$
$D_2 = Q_2'Q_1Q_0 + Q_2Q_1'Q_0'$
Y $= Q_2'Q_1Q_0'$

‘

5 Verilog Code

```
module OIO(input d,input clk,output reg out);

always@(posedge clk)
begin
if (d==0) begin
out<=0;
end else if (d==1) begin
out<=1;
end
end
endmodule
```

Figure 1: Positive edge triggered D Flip-Flop

```
module fsm;
reg clk;
reg dc,db,da,x;
wire [2:0] q;
wire out;
  assign out = ~q[2] & q[1] & ~q[0];
  OIO df1(dc,clk,q[2]);
  OIO df2(db,clk,q[1]);
  OIO df3(da,clk,q[0]);
  always @(posedge clk) begin
    dc = (((q[2])&&(~q[0]))||((q[1])&&(q[0])));
    db = (((q[1])&&(~q[0]))||((~q[2])&&(~q[1])&&(q[0])));
    da = ((~q[0])&&(x||q[2]||q[1]));
end
initial begin
 $dumpfile("fsm.vcd");
 $dumpvars(0,fsm);
 $monitor($time," %b Input = %b Output = %b State = %b
 %b %b",clk,x,out,q[2],q[1],q[0]);
 x = 0;
 dc = 0;
 db = 0;
 da = 0;
 clk = 1;
 #7
 x = 1;
 #8
 x = 0;
 #20
 x = 1;
 #8
 x = 0;
 #20
 $finish;
end
always #2 clk = ~clk;
endmodule
```

Figure 2: Mealy Implementation using 3 D Flip-Flops

```
# KERNEL:                0 1 Input = 0 Output = 0 State = 0 0 0
# KERNEL:                2 0 Input = 0 Output = 0 State = 0 0 0
# KERNEL:                4 1 Input = 0 Output = 0 State = 0 0 0
# KERNEL:                6 0 Input = 0 Output = 0 State = 0 0 0
# KERNEL:                7 0 Input = 1 Output = 0 State = 0 0 0
# KERNEL:                8 1 Input = 1 Output = 0 State = 0 0 0
# KERNEL:               10 0 Input = 1 Output = 0 State = 0 0 0
# KERNEL:               12 1 Input = 1 Output = 0 State = 0 0 1
# KERNEL:               14 0 Input = 1 Output = 0 State = 0 0 1
# KERNEL:               15 0 Input = 0 Output = 0 State = 0 0 1
# KERNEL:               16 1 Input = 0 Output = 0 State = 0 0 1
# KERNEL:               18 0 Input = 0 Output = 0 State = 0 0 1
# KERNEL:               20 1 Input = 0 Output = 1 State = 0 1 0
# KERNEL:               22 0 Input = 0 Output = 1 State = 0 1 0
# KERNEL:               24 1 Input = 0 Output = 1 State = 0 1 0
# KERNEL:               26 0 Input = 0 Output = 1 State = 0 1 0
# KERNEL:               28 1 Input = 0 Output = 0 State = 0 1 1
# KERNEL:               30 0 Input = 0 Output = 0 State = 0 1 1
# KERNEL:               32 1 Input = 0 Output = 0 State = 0 1 1
# KERNEL:               34 0 Input = 0 Output = 0 State = 0 1 1
# KERNEL:               35 0 Input = 1 Output = 0 State = 0 1 1
# KERNEL:               36 1 Input = 1 Output = 0 State = 1 0 0
# KERNEL:               38 0 Input = 1 Output = 0 State = 1 0 0
# KERNEL:               40 1 Input = 1 Output = 0 State = 1 0 0
# KERNEL:               42 0 Input = 1 Output = 0 State = 1 0 0
# KERNEL:               43 0 Input = 0 Output = 0 State = 1 0 0
# KERNEL:               44 1 Input = 0 Output = 0 State = 1 0 1
# KERNEL:               46 0 Input = 0 Output = 0 State = 1 0 1
# KERNEL:               48 1 Input = 0 Output = 0 State = 1 0 1
# KERNEL:               50 0 Input = 0 Output = 0 State = 1 0 1
# KERNEL:               52 1 Input = 0 Output = 0 State = 0 0 0
```

Figure 3: Output

6 Test Bench Waveforms

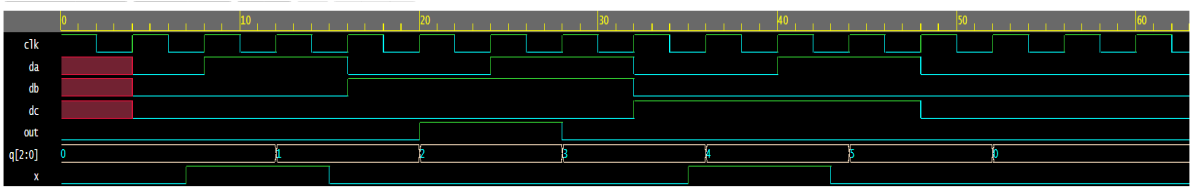


Figure 4: Generated Waveform