Time Constant of a Capacitor and Step Response in RLC Circuits
ELP100
Lab Report 3

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Contents

1 Time Constant in RC Circuit

1.1 Aim

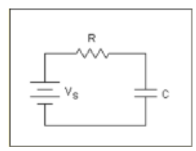
To observe and trace the complete response to step input and to determine the time constant and check with the theoretically calculated value.

1.2 Apparatus

1. Variable resistor and Multimeter
2. Function Generator (0 – 3 MHz)
3. Breadboard and Jumpers
4. Capacitor of capacitance – 0.22 µF
5. Digital Storage Oscilloscope (DSO1052B)

1.3 Theory

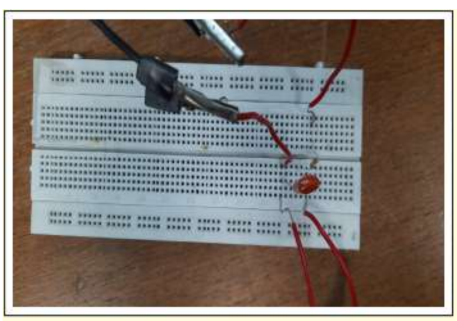
To determine the total response of an RC Series Circuit, we add the zero input response (Natural Response) and the zero state response (Forced Response).



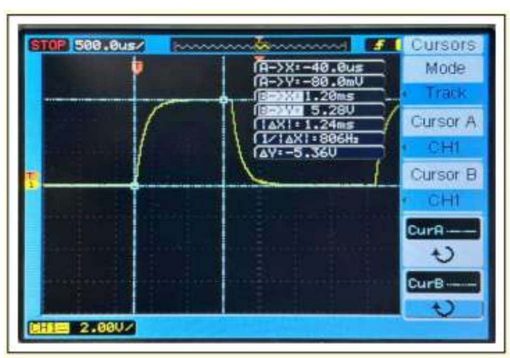
$$C\frac{dV_C}{dt} + \frac{V_C}{R} = 0 \tag{1}$$

In case of Charging, the solution is $V_C = V_0(1 \;\; e^{-\frac{Rt}{L}})$, where RC is known as Time Constant.
In case of Discharging, the solution is $V_C = V_0 e^{-\frac{Rt}{L}}$, where RC is known as Time Constant.

1.4 Breadboard Setup



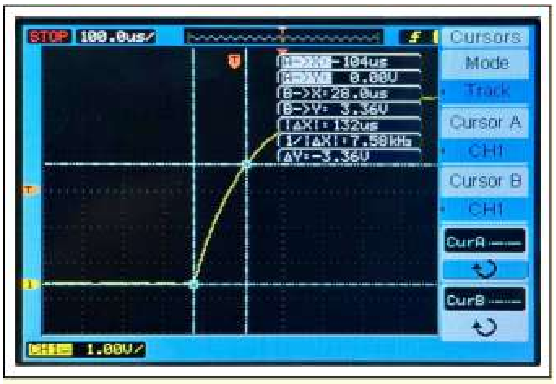
Circuit with $R = 470\Omega$ and $C = 0.23\mu F$



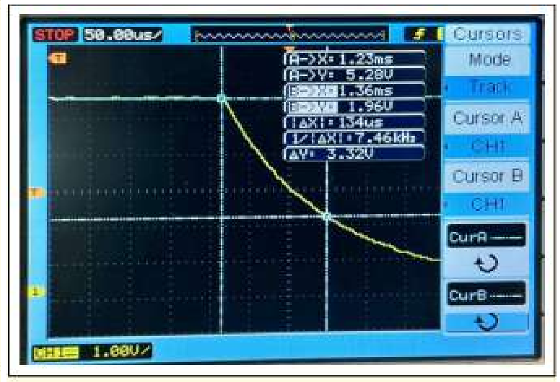
Peak Voltage is 5.28V

1.5 Observation

Status	Voltage(V)	Time Constant(τ)
Charging	63% of 5.28 = 3.33	132µs
Discharging	37% of 5.28 = 1.94	134µs



Charging



Discharging

1.6 Calculation

Theoretical Time Constant (τ) = R $\times$ C = 470 $\times$ 0.23 $\times$ 10^{-6}s=108.1 µs.
Calculated Time Constant $\approx$ 133 µs

1.7 Error Analysis

Error= 133µs - 108.1µs = 24.9 µs
Percentage Error= $\frac{24.9}{133}$ $\times$ 100 = 18.7%

1.8 Conclusion

Consequently, we were able to measure, within experimental error, the time constant of the series RC circuit using a DSO instrument.

2 Step Response in RLC Circuit

2.1 Aim

To observe and trace the complete response to step input in RLC Circuit.

2.2 Apparatus

1. Variable resistor and Multimeter
2. Function Generator (0 – 3 MHz)
3. Breadboard and Jumpers
4. Capacitor of capacitance – 0.22 µF and Inductance of 2H
5. Digital Storage Oscilloscope (DSO1052B)

2.3 Theory

The general Solution of Voltage in Series RLC Circuit is of the form:

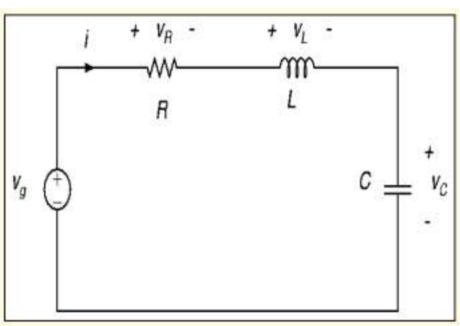
$$\text{V(t)}=A_1e^{-s_1t} + A_2e^{-s_2t}$$

where s_1 and s_2 are solutions of the quadratic equation:

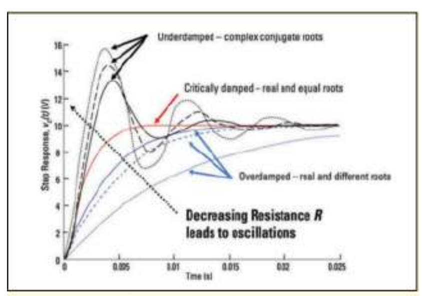
$$s^2 + 2\alpha\text{s} + \omega_0^2 = 0, \text{ where } \alpha = \frac{R}{2L} \text{ and } \omega_0^2 = \frac{1}{LC}$$

Now we have 3 cases depending on the roots of the Quadratic:

1. If $\alpha = \omega_0$ then roots are real and equal and circuit is Critically Damped
2. If $\alpha > \omega_0$ then roots are real and distinct and circuit is Over Damped
3. If $\alpha < \omega_0$ then roots are complex conjugates and circuit is Under Damped

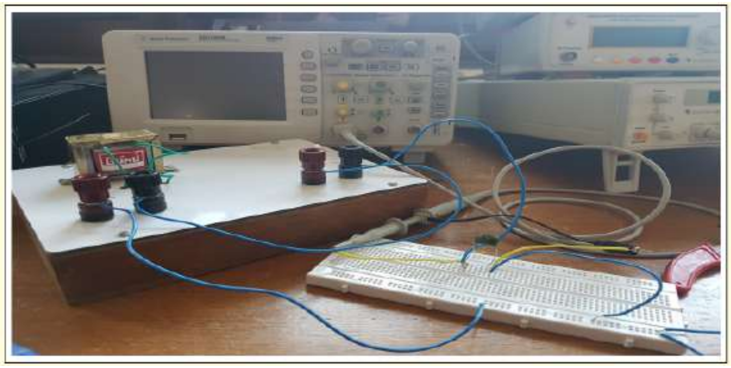


RLC Series Circuit



Effect of Changing Resistance on damping

2.4 Breadboard



2.5 Observation

Resistance(Ω)	α	ω_0
500	125	1507.55
5800	1450	1507.55
10000	2500	1507.55

2.6 Calculation

For Critically Damped Case, $\alpha = \omega_0$.
Thus, R=2Lω_0. or R $= 2 \times 2 \times 1507.55 = 6030.2\Omega$

2.7 Error Analysis

Calculated Value of R for Critical Damping= 6.03 kΩ
Measured Value of R for Critical Damping= 5.80 kΩ
Thus, Error= 0.23 kΩ
Error Percentage= $\frac{0.23}{6.03} \times 100 = 3.8\%$

2.8 Time Domains

2.8.1 Under Damped Circuit

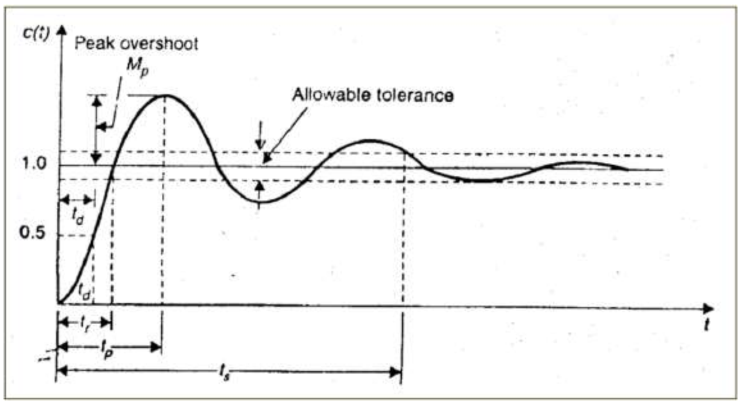
1. $\Delta V = 4.32V$ (Step Voltage)
2. $t_d = 800\mu s$ (Time till it reaches half the Step Voltage)
3. $t_r = 1.16ms$ (Time till it reaches Step Voltage First time)
4. $t_p = 2.12ms$ (Time till Overshoot Voltage)
5. $t_s = 11.7ms$ (Time till deflection from step voltage is $\leqslant 2\%$)

2.8.2 Critically Damped Circuit

1. t_d = 1ms (Time till it reaches half the Step Voltage)
2. t_r = 2.4ms (Time till it reaches Step Voltage First time)

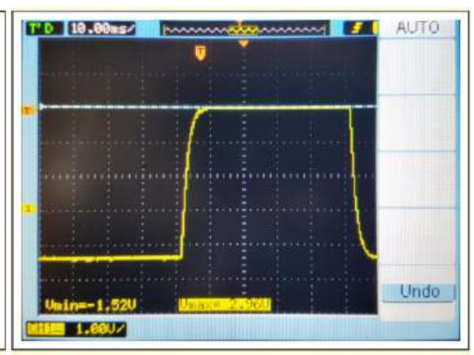
2.8.3 Over Damped Circuit

1. t_d = 1.62ms (Time till it reaches half the Step Voltage)
2. t_r = 5.2ms (Time till it reaches Step Voltage First time)

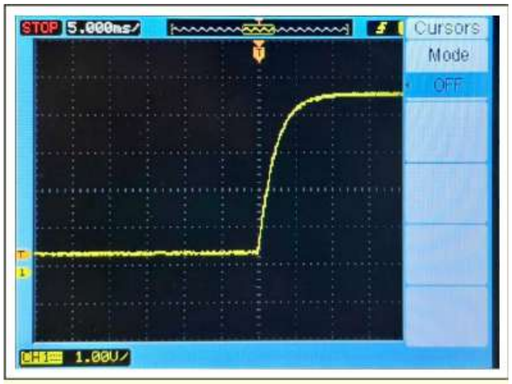


2.9 DSO Images

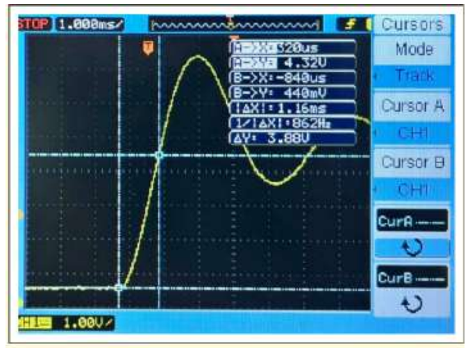
Under Damped R=500Ω



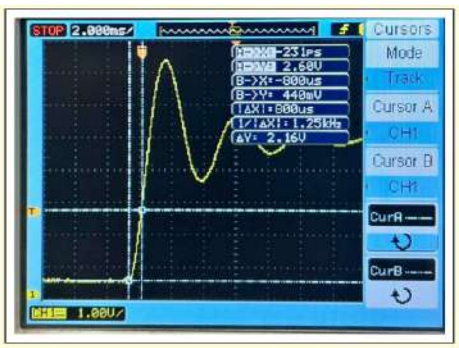
Critically Damped R=5.8kΩ



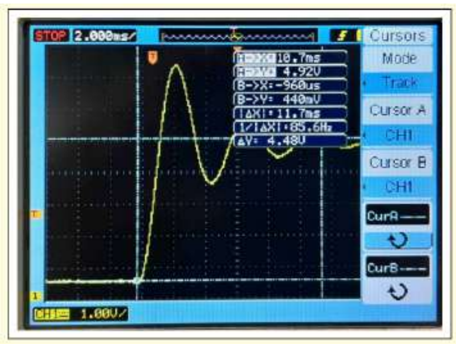
Over Damped R=$10k\Omega$



Measurement of Step Voltage in Under Damped Condition



Measurement of t_d in Under Damped Condition



Measurement of t_s in Under Damped Condition

2.10 Conclusion

Consequently, we were able to observe various damping conditions in the step response of a series RLC circuit and measure the various time domain specifications using a DSO device.

3 Sources of Error

1. Deviations due to tolerance in values.
2. Resistance in wires and change due to temperature.
3. Connections changed while circuit is powered.
4. Loose connections.
5. Difference in actual resistance, capacitance or inductance from measured value.

4 Precautions

1. Electric wires (jumpers) should be properly snipped.
2. Circuit should not be left powered for long time.
3. Proper shoes should be worn.
4. Insulated tools should be used

5 Concluding Remarks

In this experiment, the concept of step response in series RC and LCR circuits was demonstrated. In the initial phase of the experiment, the value of the time constant was derived from the graph displayed on the DSO screen. With a deflection of nearly 18.7 percent, the values were roughly equivalent to the theoretical values. This is within the experimental margin of error. In the second part of the experiment, we learned how to observe various types of damping in a series LCR circuit. In addition, we demonstrated that these cases are valid under under damped, over damped, and critically damped conditions. With a deflection of nearly 4 percent, we also confirmed that the resistance value for achieving a critically damped case came close to the theoretical value. Using the graphs obtained from the DSO display, we determined the various time domain specifications.